

4096K NV SRAM with Phantom Clock**FEATURES**

- Real time clock keeps tracks of hundredths of seconds, minutes, hours, days, date of the months, and years.
- Watch function is transparent to RAM operation.
- Data Retention over 10 years in absence of power.
- 512K x 8 NV SRAM directly replaces volatile static RAM or EEPROM.
- Embedded lithium energy cell maintains calendar operation and retains RAM data.
- Standard 32 pin DIP JEDEC Pinout.
- Month and year determine the number of days in each month
- Full $\pm 10\%$ operating range.
- Operating temperature range 0°C to 70°C.
- Available in 120 ns access time.

Functional Description

The IM 1251Y 4096K NV SRAM with Phantom Clock is a fully static nonvolatile RAM organized as 512K words by 8 bits with a built-in real time clock.

This 'NV SRAM' has all the normal characteristics of a CMOS static RAM with an important benefit of data being retained in the absence of power. Data retention current is so small that a miniature lithium cell contained within the package provides an energy source to preserve data. Protection against data loss has also been incorporated to maintain data integrity during power on/off conditions.

The Phantom Clock provides timekeeping information including hundredths of seconds, seconds, minutes, hours, day, date, month and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The Phantom Clock operates in either 24-hour or 12-hour format with an AM/PM indicator.

Pin configuration

| | | | |
|---------|----|----|-----------------|
| A18/RST | 1 | 32 | VCC |
| A16 | 2 | 31 | A15 |
| A14 | 3 | 30 | A17 |
| A12 | 4 | 29 | \overline{WE} |
| A7 | 5 | 28 | A13 |
| A6 | 6 | 27 | A8 |
| A5 | 7 | 26 | A9 |
| A4 | 8 | 25 | A11 |
| A3 | 9 | 24 | \overline{OE} |
| A2 | 10 | 23 | A10 |
| A1 | 11 | 22 | \overline{CE} |
| A0 | 12 | 21 | I/O7 |
| I/O0 | 13 | 20 | I/O6 |
| I/O1 | 14 | 19 | I/O5 |
| I/O2 | 15 | 18 | I/O4 |
| Gnd | 16 | 17 | I/O3 |

PIN NAMES

| | |
|-----------------|----------------|
| A0-A18 | Address Inputs |
| \overline{CE} | Chip Enable |
| GND | Ground |
| I/O0-I/O-7 | Input/Output |
| Vcc | Power(+5V) |
| \overline{WE} | Write Enable |
| \overline{OE} | Output Enable |
| RST | Reset |

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READ MODE

The IM 1251Y performs a read cycle whenever \overline{WE} high and \overline{CE} low. The unique address specified by the 19 address inputs A0-A18 defines which of the 4,194,304 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within access time t_{ACC} after the last address input is stable, provided that \overline{CE} and \overline{OE} access times are satisfied. If \overline{OE} or \overline{CE} access times are not satisfied, data access will be measured from the limiting parameter (t_{CO} or t_{OE}), rather than address. The state of the eight data I/O lines is controlled by the \overline{OE} and \overline{CE} control signals. The data lines may be in an indeterminate state between t_{OH} and t_{AA} but the data lines will always have valid data at t_{AA} .

WRITE MODE

The IM 1251Y is in the write mode whenever \overline{CE} and \overline{WE} inputs are held low. The latter occurring falling edge of either \overline{CE} or \overline{WE} determines the start of a write cycle. A write is terminated by the earlier rising edge of \overline{CE} or \overline{WE} . The address must be held valid throughout the write cycle. \overline{WE} must return to the high state for a minimum recovery time (t_{WR}) before another Read or Write cycle can be initiated. \overline{CE} or \overline{WE} is high during power on to perfect memory after V_{CC} reaches $V_{CC}(\min)$ but before the processor stabilizes.

DATA RETENTION

The IM 1251Y provides full functional capability for V_{CC} greater than 4.75V and write protects at 4.5V. Data is retained in the absence of V_{CC} without any additional support circuitry. The SRAM constantly monitors V_{CC} . The moment V_{CC} decays, the RAM automatically write protects itself. All inputs to the RAM become “don’t care” and all outputs are in high impedance-state. As V_{CC} falls below approximately 3.0V the power switching circuit connects the lithium energy source to RAM to retain data. During power-on, when V_{CC} rises above approximately 3.0V the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} becomes greater than 4.5V.

Maximum Ratings

Operating Temperature.....0°C to 70°C
Storage Temperature.....0°C to 70°C
Soldering Temperature
And Time.....260°C for 10 sec
Supply Voltage.....-0.5V to 7.0V
Input Voltage.....-0.5V to 7.0V
Input/ Output Voltage.....-0.5V to
 $V_{CC} + 0.3V$
Power Dissipation.....1.0W

Recommended D.C. Operating Conditions

| Parameter | Symbol | Min. | Typ | Max. | Unit |
|----------------|----------|------|-----|----------------|------|
| Supply Voltage | V_{CC} | 4.5 | 5.0 | 5.5 | V |
| | Gnd | 0 | - | 0 | V |
| Input Voltage | V_{IH} | 2.2 | 3.5 | $V_{CC} + 0.3$ | V |
| | V_{IL} | 0 | - | 0.8 | V |

4096K NV SRAM with Phantom Clock**PHANTOM CLOCK OPERATION**

Communication with the Phantom Clock is established by pattern recognition on a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on I/O0. All access which occur prior to recognition of the 64-bit pattern are directed to memory.

After recognition is established, the next 64 read or write cycles either extract or update data in the Phantom Clock, and memory access is inhibited.

Initially, a read cycle to any memory location using the $\overline{\text{CE}}$ and $\overline{\text{OE}}$ control of the Phantom Clock starts the pattern recognition sequence by moving a pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{\text{CE}}$ and $\overline{\text{WE}}$ control of the SmartWatch. These 64 write cycles are used only to gain access to the Phantom Clock.

However, write cycle generated to gain access to the Phantom Cycle are also writing data to a location in the mated RAM. When the first write cycle is executed it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register have been matched. With a correct match for 64-bits the Phantom Clock is enabled and data transfer to or from the time-keeping register can proceed. The next 64-cycles will cause the Phantom Clock to either receive or transmit data on I/O0, depending the level of the OE pin or the WE.

PHANTOM CLOCK REGISTER INFORMATION

The Phantom Clock information is contained in 8 registers of 8 bits, each of which is sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the Phantom Clock registers, each register must be handled in - groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results.

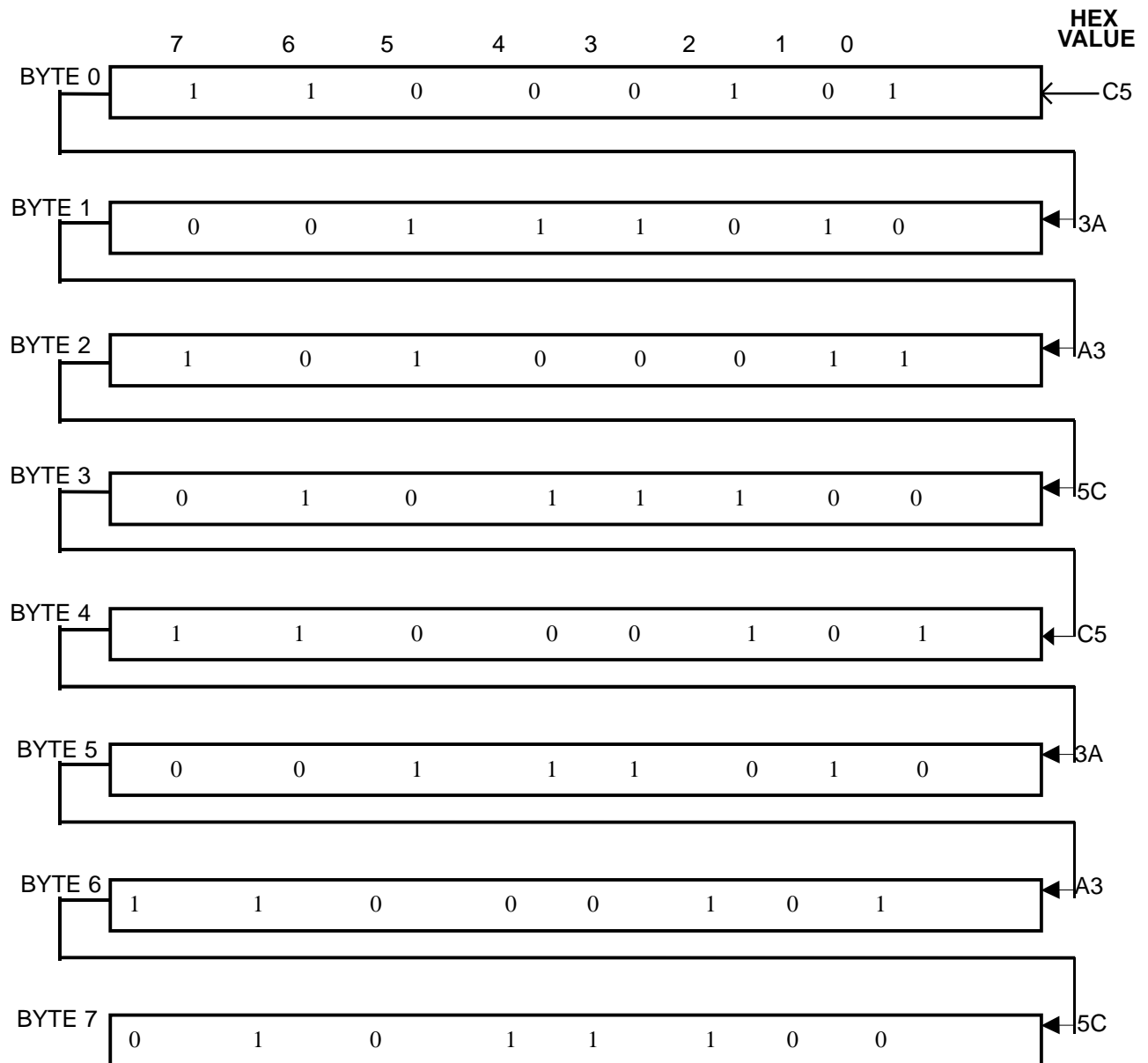
Data contained in the Phantom Clock register is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

AM/PM 12/24 MODE

Bit 7 of the hours register is defined as the 12-or-24 hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

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PHANTOM CLOCK REGISTER DEFINITION



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OSCILATTOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the RESET and oscillator functions. Bit 4 controls the RESET (pin 1). When the RESET bit is set to logic 1, the RESET input pin is ignored. When the RESET bit is set to logic 0, A low input on the RESET pin will cause the Phantom Clock to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. When set to logic 1, the oscillator is off. When set to logic 0, the oscillator turns on and the watch becomes operational. These bits are shipped from the factory set to a logic 1.

PHANTOM CLOCK REGISTER DEFINITION

| REGISTER | | | | | RANGE (BCD) |
|----------|---------|--------|-----------|-------------|----------------|
| 0 | 0.1 SEC | | 0.01 SEC | | 00-99 |
| 1 | 0 | 10 SEC | SECONDS | | 00-59 |
| 2 | 0 | 10 MIN | MINUTES | | 00-59 |
| 3 | 12/24 | 0 | 10 A/P | HR | 01-12 00-23 |
| 4 | 0 | 0 | OSC | RST | 01-07 |
| 5 | 0 | 0 | 10 DATE | DATE | 01-13 |
| 6 | 0 | 0 | 0 | 10 MONTH | 01-12 |
| 7 | 10YEAR | | YEAR | | 00-99 |

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DC ELECTRICAL CHARACTERISTICS (0°C TO 70°C; Vcc = 5V + 10%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|--|------------|------|-----|------|-------|
| Input Leakage Current | I_{IL} | -1.0 | | +1.0 | A |
| I/O Leakage Current $\overline{CE} > V_{IH} < V_{CC}$ | I_{IO} | -1.0 | | +1.0 | A |
| Output Current @ 2.4V | I_{OH} | -1.0 | | | mA |
| Output Current @ 0.4V | I_{OL} | 2.0 | | | mA |
| Standby Current $\overline{CE} = 2.25V$ | I_{CCS1} | | 5.0 | 10 | mA |
| Standby Current $\overline{CE} = V_{CC} - 0.5V$ | I_{CCS2} | | 3.0 | 5.0 | mA |
| Operating Current $t_{CYC} = 120ns$ | I_{CC01} | | | 85 | mA |

Notes

- Typical values are measured at Ta = 25°C and Vcc = 5V

Capacitance

| Parameter | Description | Test conditons | Min. | Typ | Max | Unit |
|-----------|-------------------|----------------|------|-----|-----|------|
| C_I | Input capacitance | $V_i = 0V$ | - | 5 | 10 | pF |
| C_{IO} | I/O capacitance | $V_{IO} = 0V$ | - | 5 | 10 | pF |

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Switching Characteristics over the operating range

| Parameter | Description | Min | Max | Unit |
|-----------|---------------------------------|-----|-------|------|
| t_{RC} | Read cycle time | 120 | | ns |
| t_{ACC} | Address access time | | 120 | ns |
| t_{OE} | Output enable access time | | 60 | ns |
| t_{CO} | CE to output valid | | 120 | ns |
| t_{COE} | OE or CE to output valid | 5 | | ns |
| t_{OD} | Output High Z from Deselection | | 40 | ns |
| t_{OH} | Output hold from address change | 5 | | ns |
| t_{WC} | Write cycle time | 120 | | ns |
| t_{AW} | Address setup time | 0 | | ns |
| t_{WP} | Write pulse-width | 90 | | ns |
| t_{WR} | Write recovery time | 20 | | ns |
| t_{ODW} | Output High Z from <u>WE</u> | | 40 ns | |
| t_{OEW} | Output Active from <u>WE</u> | 5 | | ns |
| t_{DS} | Input data setup time | 50 | | ns |
| t_{DH} | Input data hold time | 20 | | ns |

POWER DOWN/POWER UP TIMING

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|--|-----------|-----|-----|-----|---------|
| CE at VIH before power-down | t_{PD} | 0 | | | μ s |
| Vcc Slow from 4.5 V to 0V (CE at VIH) | t_F | 300 | | | μ s |
| Vcc Slow from 0V to 4.5 V (CE at VIH) | t_R | 0 | | | μ s |
| CE at VIH after Power-Up | t_{REC} | | | 2 | ms |

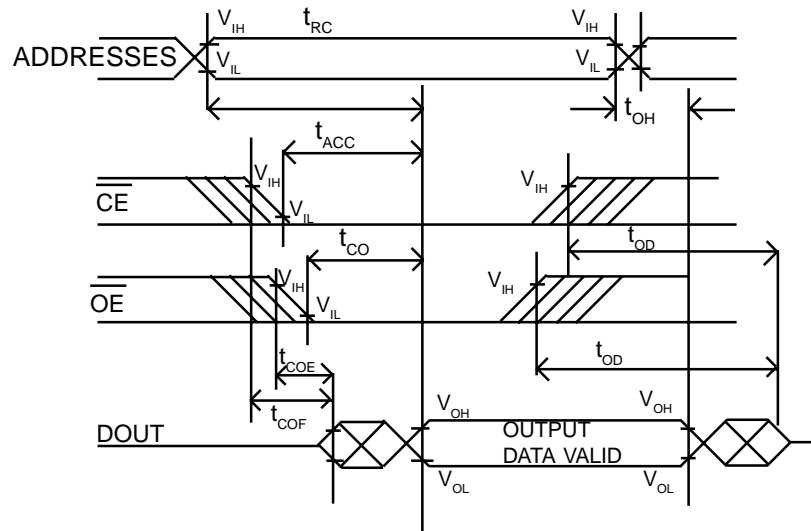
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PHANTOM CLOCK AC ELECTRICAL CHARACTERISTICS(0°C TO 70°C,V_{CC}= 4.5 TO 5.5V)

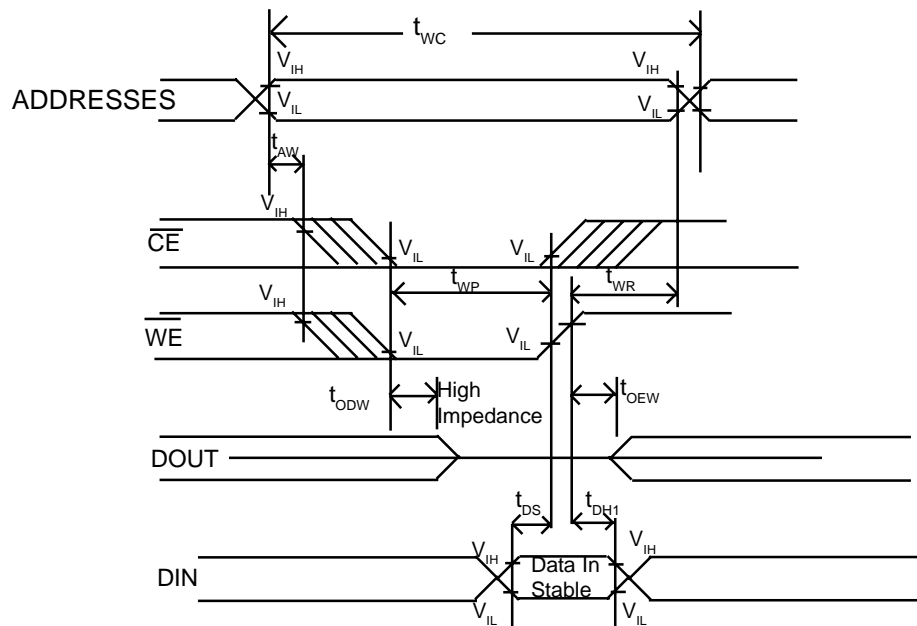
| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|-----------------------|-----------|-----|-----|-----|-------|
| Read Cycle Time | t_{RC} | 120 | | | ns |
| CE Access Time | t_{CO} | | | 100 | ns |
| OE Access Time | t_{OE} | | | 100 | ns |
| CE to Output Low Z | t_{COE} | 10 | | | ns |
| OE to Output Low Z | t_{OEE} | 10 | | | ns |
| CE to Output High Z | t_{OD} | | | 40 | ns |
| OE to Output High Z | t_{ODO} | | | 40 | ns |
| Read Recovery | t_{RR} | 20 | | | ns |
| Write Cycle Time | t_{WC} | 120 | | | ns |
| Write Pulse Width | t_{WP} | 100 | | | ns |
| Write Recovery | t_{WR} | 20 | | | ns |
| Data Setup Time | t_{DS} | 40 | | | ns |
| Data Hold Time | t_{DH} | 10 | | | ns |
| CE Pulse Width | t_{CW} | 100 | | | ns |
| RESET Pulse Width | t_{RST} | 200 | | | ns |
| CE High to Power-Fail | t_{PF} | | | 0 | ns |

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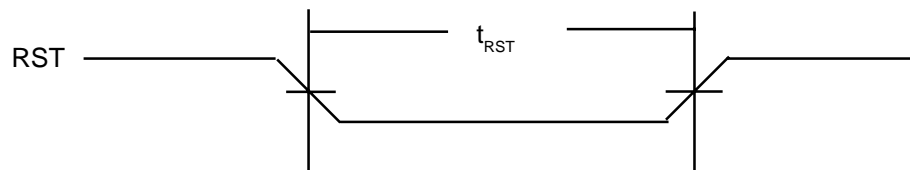
READ CYCLE



WRITE CYCLE 1

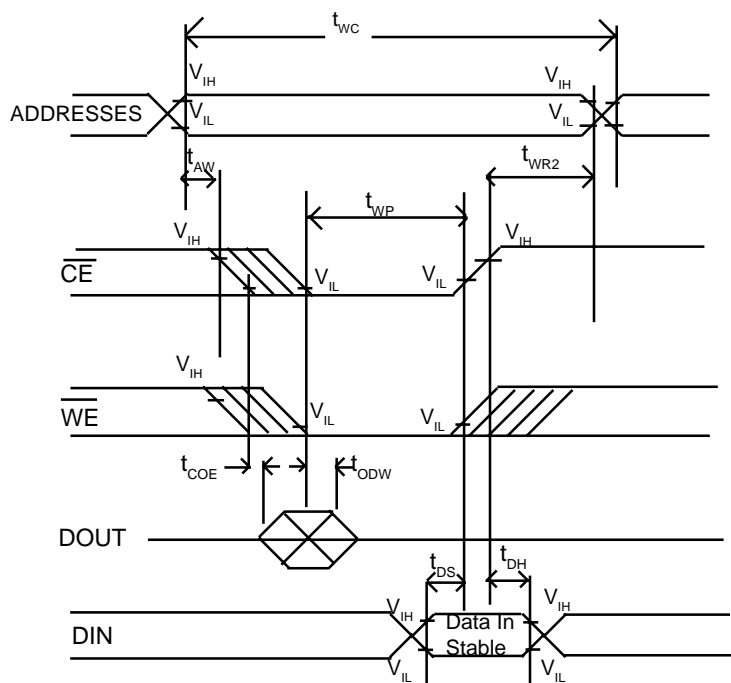


RESET FOR PHATOM CLOCK

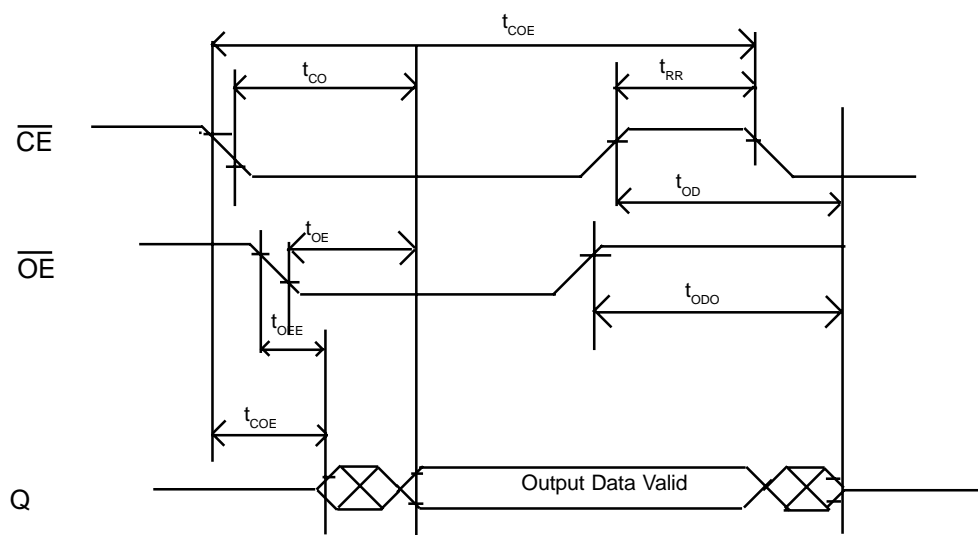


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WRITE CYCLE 2



Read cycle to Phantom Clock



4096K NV SRAM with Phantom Clock

Write Cycle to Phantom Clock

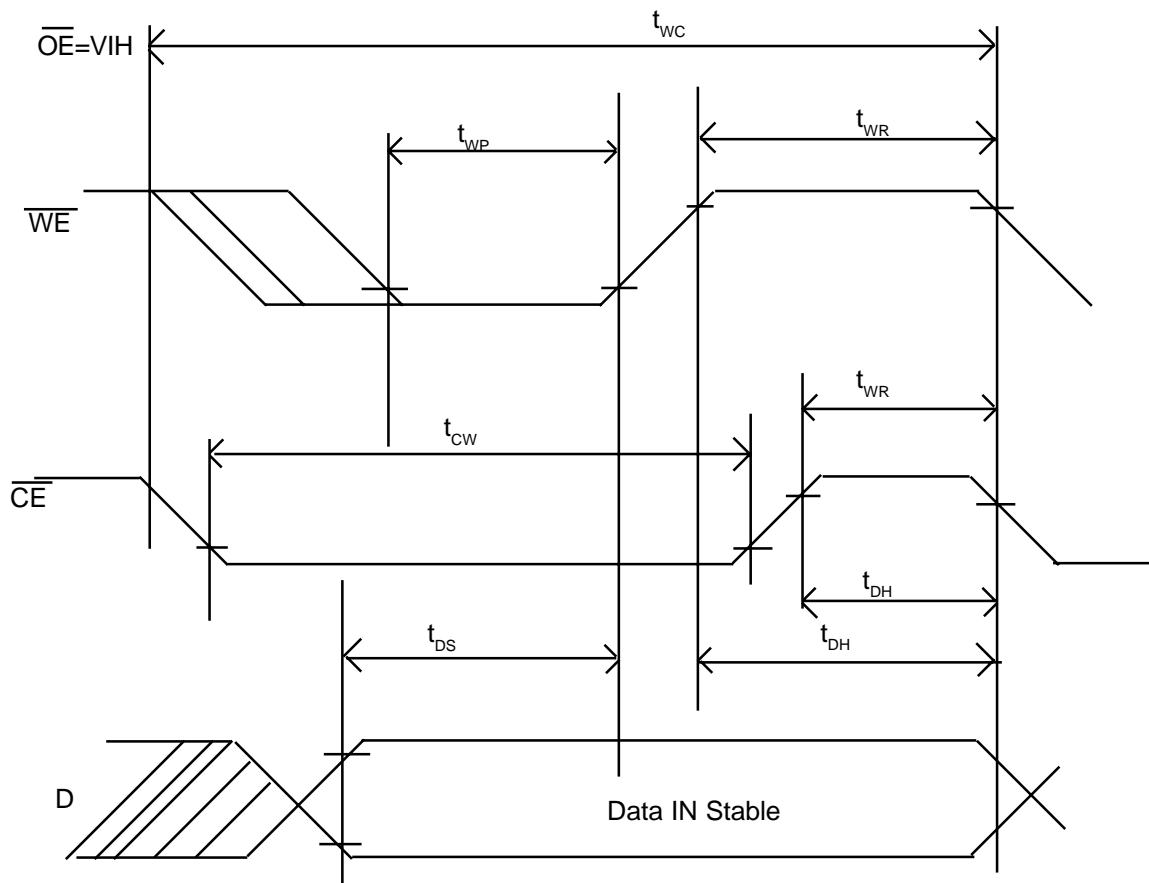
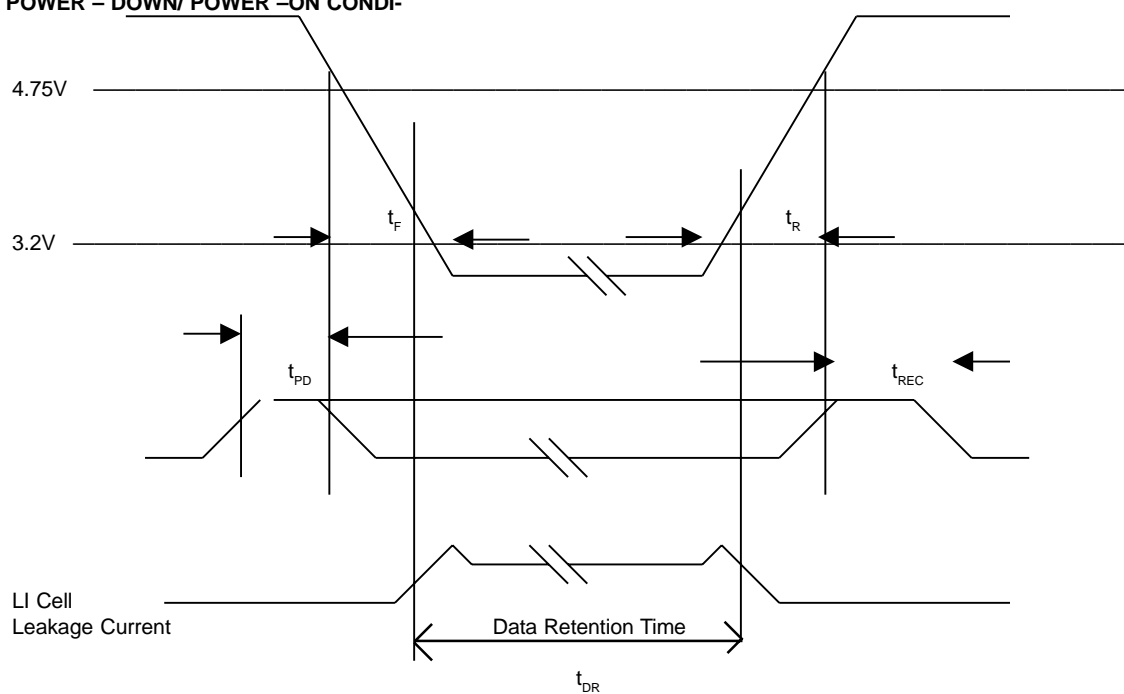
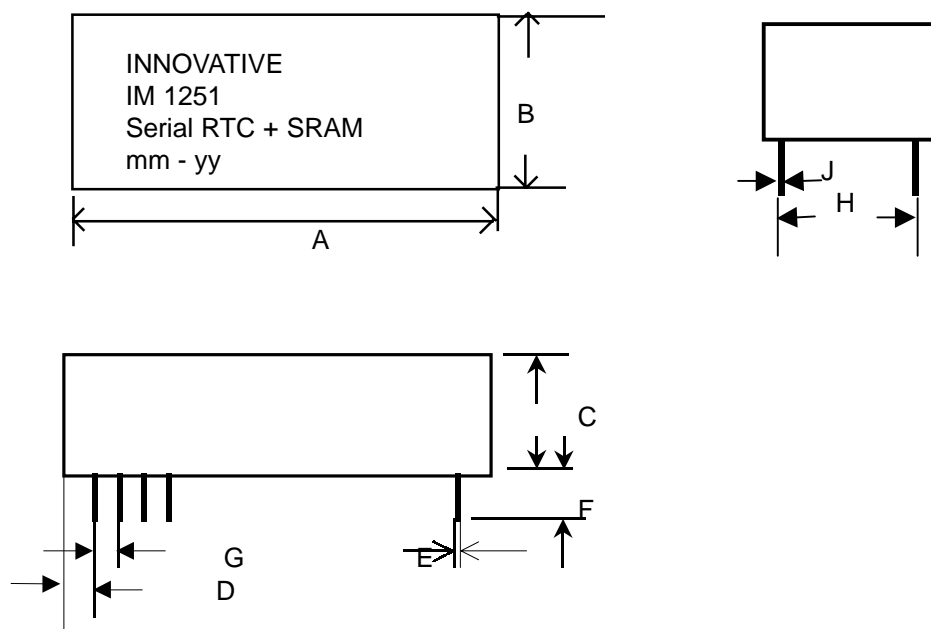


FIG. D POWER - DOWN/ POWER -ON CONDI-
TION



4096K NV SRAM with Phantom Clock



| DIM IN INCHES | MIN. | MAX. |
|---------------|-------|-------|
| A | 1.52 | 1.54 |
| B | 0.695 | 0.72 |
| C | 0.395 | 0.415 |
| D | 0.1 | 0.13 |
| E | 0.015 | 0.021 |
| F | 0.12 | 0.16 |
| G | 0.09 | 0.11 |
| H | 0.59 | 0.63 |
| J | 0.008 | 0.012 |