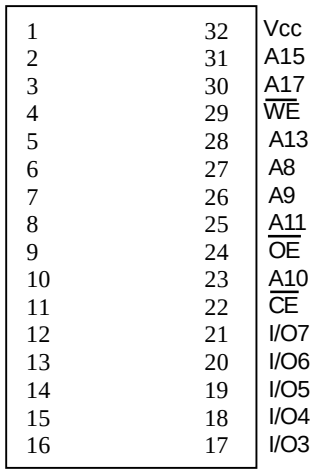
256K X 8 NO POWER SRAM

FEATURES

- Data Retention in the absence of power
- Automatic data protection during power failure
- Data Retention over 10 years
- Unlimited write cycles
- Conventional SRAM write cycles
- Low power CMOS
- Equal read/write cycle times
- +5Vonly read/write
- Operating voltage range ±10%
- Direct replacement for 256K X 8 SRAM or EPROM
- Standard 36 pin DIP JEDEC Pinout

PIN CONFIGURATION



PIN NAMES

NC	No Connection
OE	Output Enable
Gnd	Ground
I/O0 – I/O7	Data in/ Data Out
Vcc	Power Supply +5V
WE	Write Enable
A0 – A17	Address Inputs
CE	Chip Enable

Functional Description

The IM 1249Y–100 is a 2,097,152 bit, fully static NP RAM organized as 256K X 8 using CMOS and an internal lithium energy source.

This 'NO POWER' RAM has all the normal characteristics of a CMOS static RAM with an important benefit of data being retained in the absence of power. Data retention current is so small that a miniature lithium cell contained within the package provides an energy source to preserve data. Protection against data loss has also been incorporated to maintain data integrity during power on/off conditions.

The IM 1249Y–100 RAM can be directly used in place of existing static RAMs. There is no limit to the number of write cycles that can be executed and no additional support circuitry is required for interface to a microprocessor.

READ MODE

The IM 1249Y-100 performs a read cycle whenever $\overline{WE}$ high and $\overline{CE}$ low. The unique address specified by the 19 address inputs A0-A17 defines which of the 2,097,144 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within access time t_{ACC} after the last address input is stable, provided that $\overline{CE}$ and $\overline{OE}$ access times are satisfied. If $\overline{OE}$ or $\overline{CE}$ access times are not satisfied, data access will be measured from the limiting parameter (t_{CO} or t_{OE}), rather than address. The state of the eight data I/O lines is controlled by the $\overline{OE}$ and $\overline{CE}$ control signals. The data lines may be in an indeterminate state between t_{OH} and t_{AA} but the data lines will always have valid data at $t_{AA.}$

WRITE MODE

The IM 1249Y-100 is in the write mode whenever $\overline{CE}$ and $\overline{WE}$ inputs are held low. The latter occurring falling edge of either $\overline{CE}$ or $\overline{WE}$ determines the start of a write cycle. A write is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. The address must be held valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another Read or Write cycle can be initiated. $\overline{CE}$ or $\overline{WE}$ is high during power on to perfect memory after Vcc reaches Vcc (min) but before the processor stabilizes.

DATA RETENTION

The IM 1249Y-100 provides full functional capability for Vcc greater than 4.5V and write protects at 4.25V. Data is retained in the absence of Vcc without any additional support circuitry. The SRAM constantly monitors Vcc. The moment Vcc decays, the RAM automatically write protects itself. All inputs to the RAM become “don’t care” and all outputs re in high impedance-state. As Vcc falls below approximately 3.0V the power switching circuit connects the lithium energy source to RAM to retain data. During power-on, when Vcc rises above approximately 3.0V the power switching circuit connects external Vcc to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after Vcc becomes greater than 4.5V.

Maximum Ratings

Operating Temperature….0°C to 70°C

Storage Temperature……..0°C to 70°C

Soldering Temperature

And Time……..260°C for 10 sec

Supply Voltage…….. 0V to 7.0V

Input Voltage……-0.5V to 7.0V

Input/ Output Voltage…….-0.5V to Vcc + 0.3V

Power Dissipation……1.0W

Recommended D.C. Operating Conditions

Parameter	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
	Gnd	0	-	0	V
Input Voltage	V_{IH}	2.2	3.5	Vcc +0.3	V
	V_{IL}	0	-	0.8	V

FRESHNESS SEAL AND SHIPPING

The IM1250Y - 100 is shipped from INNOVATIVE MICROTECHONOLOGY INC. with the lithium energy source disconnected , guaranteeing full energy capacity. When Vcc is first applied at a level of greater than 4.15 volts, the lithium energy source is enabled for battery back-up operation.

Electrical Characeteristics

Parameter	Description	Test conditons	Min.	Typ	Max	Unit
I_{LI}	Input Leakage	$\underline{Vi}$ = 0 to Vcc	-1	-	1	µA
I_{OCA}	Average operating Current	$\overline{CE}$ = Vcc	-	45	80	µA
		$\overline{CE}$ = V_{IH},I_{IO} = 0mA	-	1	3	mA
I_{vcc}	Operating Supply current	$\overline{CE}$ = V_{IL},I_{IO} = 0mA	-	-	50	mA
I_{LO}	Output Leakage	$\overline{CE}$ = V_{IH} or Vcc Vi/o = Gnd to Vcc	-1		1	µA
V_{OH}	High level output voltage	I_{OH} = - 1.0 mA	2.4		Vcc - 0.1	V
V_{OL}	Low level output voltage	I_{OL} = 2.1 mA	-	0.2	0.4	V
V_{TP}	Write protection voltage	-	4.25	4.37	4.49	V

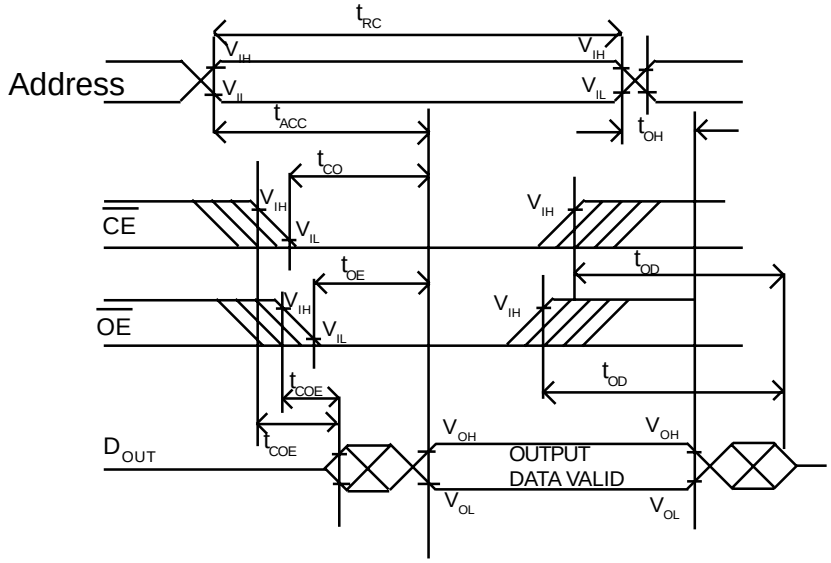
Capacitance

Parameter	Description	Test conditons	Min.	Typ	Max	Unit
C_{ADD}	Address capacitance	V_{ADD} = 0V	-	3	5	pF
C_I	Input capacitance	V_i =0V	-	5	6	pF
$C_{I/O}$	I/O capacitance	V_{IO} = 0V	-	6	7	pF

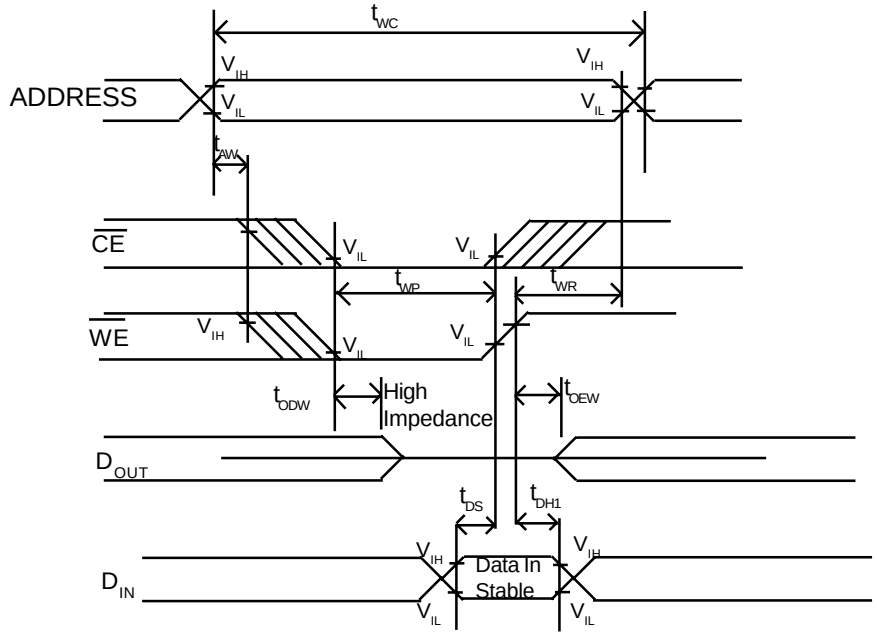
Switching Characteristics over the operating range

Parameter	Description	Min	Max	Unit
t_{RC}	Read cycle time	100	-	ns
t_{ACC}	Address access time	-	100	ns
t_{OE}	Output enable access time	-	50	ns
tCO	CE to output valid	-	100	ns
t_{COE}	OE or CE to output valid	5	-	ns
t_{OD}	Output High Z from Deselection	-	35	ns
t_{OH}	Output hold from adds change	5	-	ns
t_{WC}	Write cycle time	100	-	ns
t_{AW}	Address setup time	0	-	ns
t_{WP}	Write pulse-width	75	-	ns
t_{WR}	Write recovery time	5	-	ns
t_{ODW}	Output High Z from WE		35	ns
t_{OEW}	Output Active from WE	5	-	ns
t_{DS}	Input data setup time	40	-	ns
t_{DH1}	Input data hold time	15	-	ns

READ CYCLE



WRITE CYCLE 1



WRITE CYCLE 2

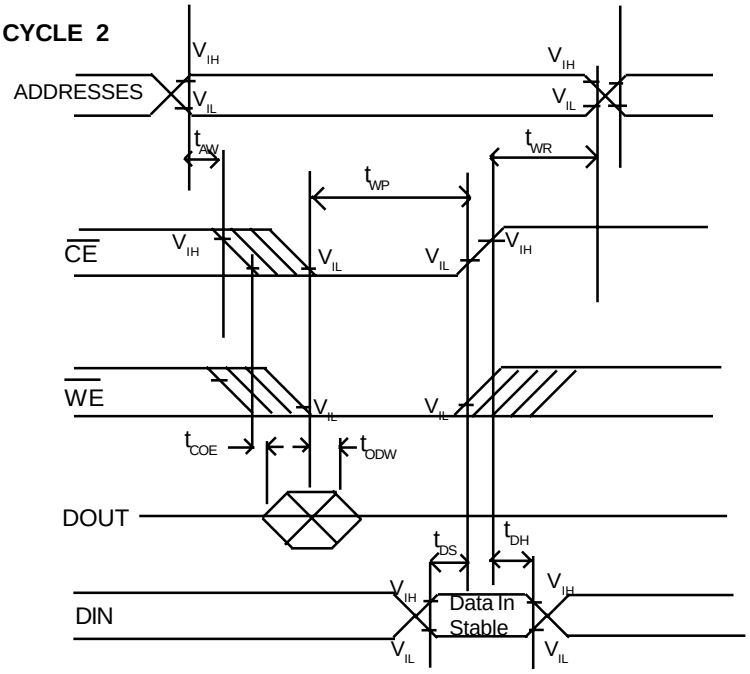
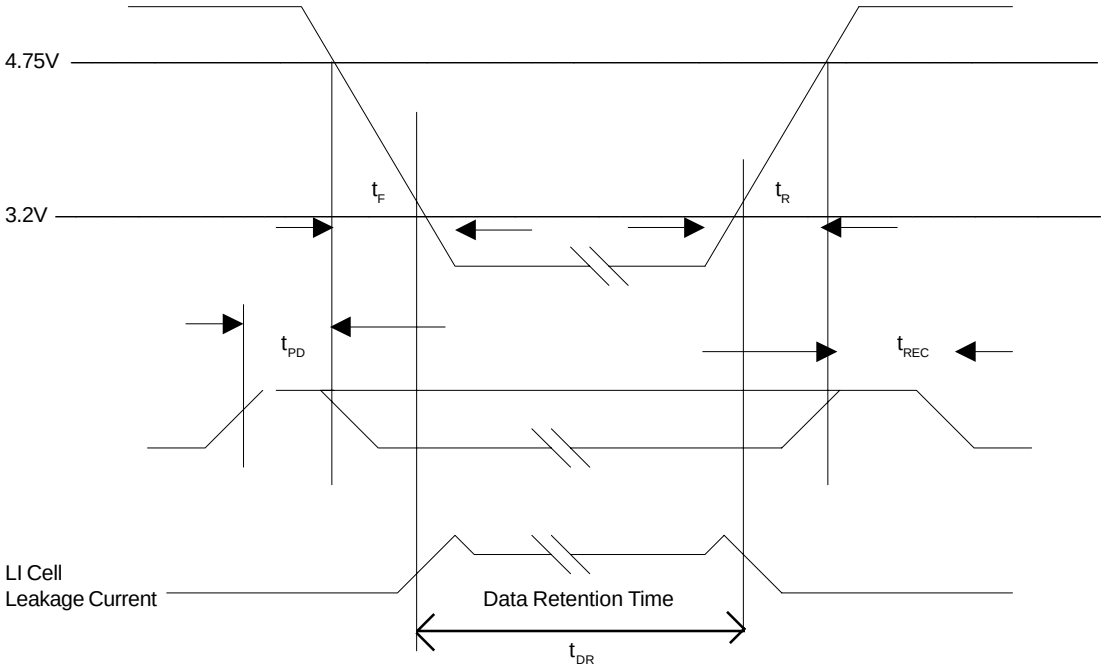
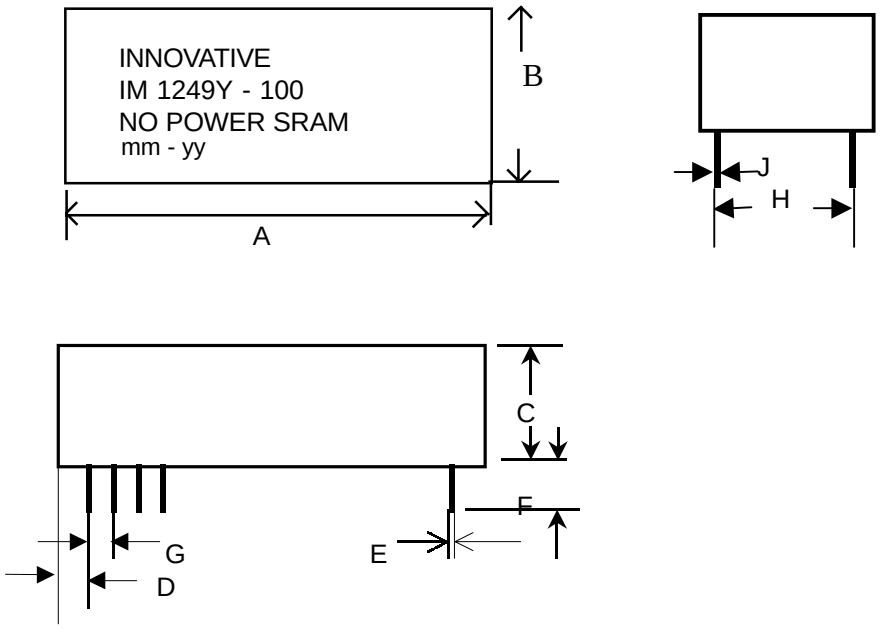


FIG. D POWER – DOWN/ POWER –ON CONDITION



Notes:

1. $\overline{WE}$ is to be high during read cycle.
2. During write cycle that is controlled by $\overline{CE}$, output buffer is in high impedance state irrespective of whether $\overline{OE}$ is high or low level.
3. During write cycle that is controlled by $\overline{WE}$, output buffer is in high impedance state if $\overline{OE}$ is high.



DIM IN INCHES	MIN.	MAX.
A	1.72	1.754
B	0.72	0.74
C	0.395	0.415
D	0.09	0.12
E	0.015	0.021
F	0.12	0.16
G	0.09	0.11
H	0.59	0.63
J	0.008	0.012