



IDT74LVCHR16543A

FEATURES:

- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP
and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- CMOS power levels (0.4μW typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVCHR16543A:

- Balanced Output Drivers: ± 12 mA
- Low switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

DESCRIPTION:

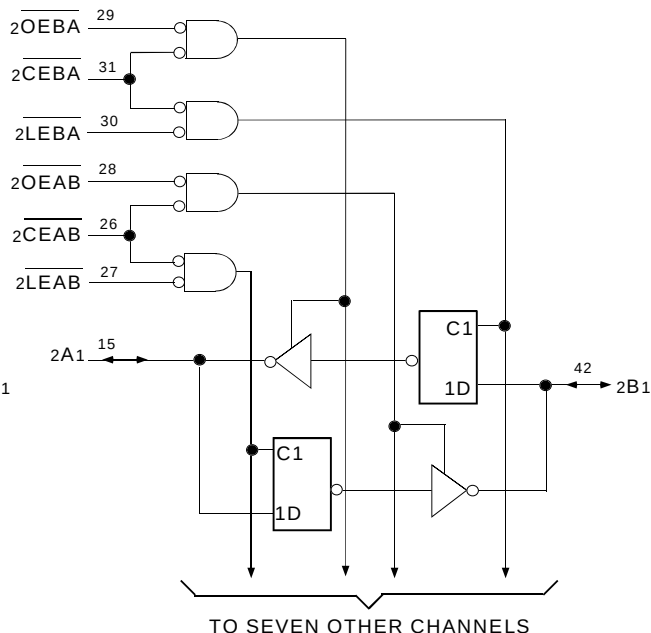
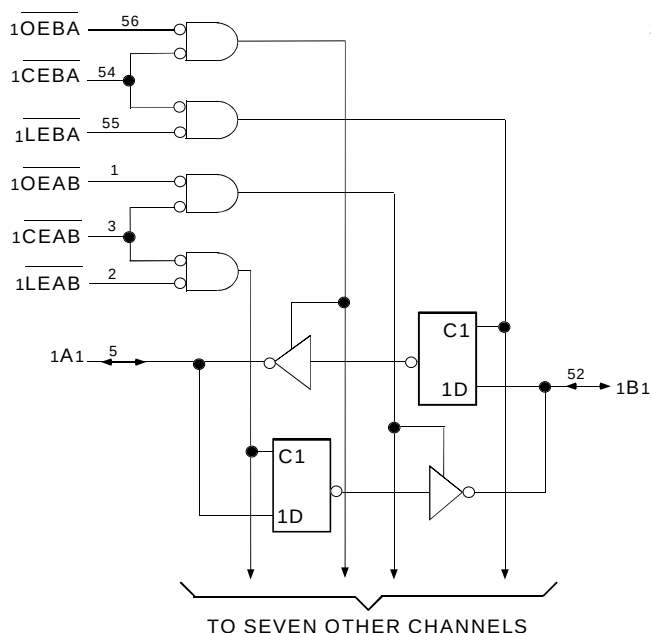
The LVCHR16543A 16-bit registered transceiver is built using advanced dual metal CMOS technology. The LVCHR16543A device can be used as two independent 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ($\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$) and output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) inputs are provided for each register to permit independent control in either direction of data flow. The A-to-B Enable ($\overline{\text{CEAB}}$) must be low in order to enter data from A or to output data from B. If $\overline{\text{CEAB}}$ is low and $\overline{\text{LEAB}}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{\text{LEAB}}$ puts the A latches in the storage mode. With $\overline{\text{CEAB}}$ and $\overline{\text{OEAB}}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$ inputs. To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current sinking capability of the driver.

The LVCHR16543A has series resistors in the device output structure which will significantly reduce line noise when used with light loads. The driver has been designed to drive $\pm 12\text{mA}$ at the designated threshold levels.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVCHR16543A has “bus-hold” which retains the input's last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

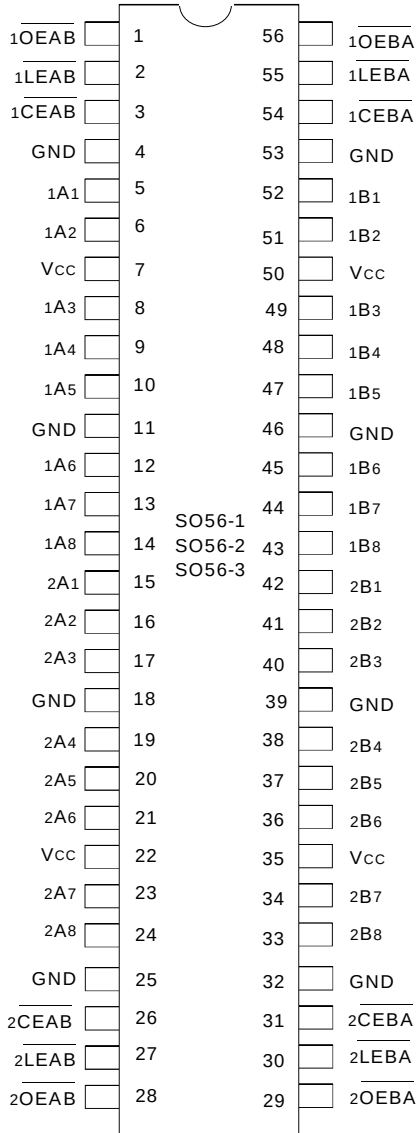
FUNCTIONAL BLOCK DIAGRAM



EXTENDED COMMERCIAL TEMPERATURE RANGE

OCTOBER 1999

PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{xOEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{xOEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{xCEAB}$	A-to-B Enable Input (Active LOW)
$\overline{xCEBA}$	B-to-A Enable Input (Active LOW)
$\overline{xLEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{xLEBA}$	B-to-A Latch Enable Input (Active LOW)
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs ⁽¹⁾
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs ⁽¹⁾

NOTE:

- These pins have "Bus-hold". All other pins are standard inputs, outputs, or I/Os.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	- 0.5 to +6.5	V
T_{STG}	Storage Temperature	- 65 to +150	°C
I_{OUT}	DC Output Current	- 50 to +50	mA
I_{IK} I_{OK}	Continuous Clamp Current, $V_I < 0$ or $V_O < 0$	- 50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	± 100	mA

LVC Link

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4.5	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	6.5	8	pF
$C_{I/O}$	I/O Port Capacitance	$V_{IN} = 0V$	6.5	8	pF

LVC Link

NOTE:

- As applicable to the device type.

FUNCTION TABLE (each 8-bit section) (1, 2)

Inputs				Outputs
$\overline{xCEAB}$	$\overline{xLEAB}$	$\overline{xOEAB}$	xAx	xBx
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	$B_0^{(3)}$
L	L	L	L	L
L	L	L	H	H

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
- A-to-B data flow is shown; B-to-A flow control is the same except using $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
- Before $\overline{LEAB}$ LOW-to-HIGH Transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to 5.5V	—	—	± 5	μA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = 0$ to 5.5V	—	—	± 10	μA
I_{OFF}	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}$, V_{IN} or $V_O \leq 5.5\text{V}$		—	—	± 50	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$	$V_{IN} = \text{GND}$ or V_{CC}	—	—	10	μA
			$3.6 \leq V_{IN} \leq 5.5\text{V}^{(2)}$	—	—	10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$ other inputs at V_{CC} or GND		—	—	500	μA

LVC Link

NOTES:

- Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.
- This applies in the disabled state only.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
I_{BHH} I_{BHL}	Bus-Hold Input Sustain Current	$V_{CC} = 3.0\text{V}$	$V_I = 2.0\text{V}$	-75	—	—	μA
			$V_I = 0.8\text{V}$	75	—	—	
I_{BHH} I_{BHL}	Bus-Hold Input Sustain Current	$V_{CC} = 2.3\text{V}$	$V_I = 1.7\text{V}$	—	—	—	μA
			$V_I = 0.7\text{V}$	—	—	—	
I_{BHHO} I_{BHLO}	Bus-Hold Input Overdrive Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to 3.6V	—	—	± 500	μA

LVC Link

NOTES:

- Pins with Bus-hold are identified in the pin description.
- Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = -0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	IOH = -4mA	1.9	—	
			IOH = -6mA	1.7	—	
		VCC = 2.7V	IOH = -4mA	2.2	—	
			IOH = -8mA	2	—	
		VCC = 3.0V	IOH = -6mA	2.4	—	
			IOH = -12mA	2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 4mA	—	0.4	
			IOL = 6mA	—	0.55	
		VCC = 2.7V	IOL = 4mA	—	0.4	
			IOL = 8mA	—	0.6	
		VCC = 3.0V	IOL = 6mA	—	0.55	
			IOL = 12mA	—	0.8	

LVC Link

NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = -40°C to +85°C.

OPERATING CHARACTERISTICS, VCC = 3.3V ± 0.3V, TA = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per transceiver Outputs enabled	CL = 0pF, f = 10Mhz		pF
CPD	Power Dissipation Capacitance per transceiver Outputs disabled			pF

SWITCHING CHARACTERISTICS ⁽¹⁾

Symbol	Parameter	V _{CC} = 2.7V		V _{CC} = 3.3V±0.3V		Unit
		Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay x _A to x _B or x _B to x _A	1.5	7	1.5	6	ns
t _{PLH} t _{PHL}	Propagation Delay x _{LEB} to x _A , x _{LEAB} to x _B	1.5	8	1.5	7	ns
t _{PZH} t _{PZL}	Output Enable Time x _{CEB} or x _{CEAB} to x _A or x _B	1.5	9	1.5	8	ns
t _{PZH} t _{PZL}	Output Enable Time x _{OEBA} or x _{OEAB} to x _A or x _B	1.5	9	1.5	8	ns
t _{PHZ} t _{PLZ}	Output Disable Time x _{CEBA} or x _{CEAB} to x _A or x _B	1.5	7.5	1.5	6.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time x _{OEBA} or x _{OEAB} to x _A or x _B	1.5	7.5	1.5	6.5	ns
t _{SU}	Set-up Time, data before $\overline{CE} \uparrow$	2	—	2	—	ns
t _{SU}	Set-up Time, data before $\overline{LE} \uparrow$, $\overline{CE}$ LOW	2	—	2	—	ns
t _H	Hold Time, data after $\overline{CE} \uparrow$	2	—	2	—	ns
t _H	Hold Time, data after $\overline{LE} \uparrow$, $\overline{CE}$ LOW	2	—	2	—	ns
t _W	Pulse Duration x _{LEAB} or x _{LEBA} , x _{CEAB} or x _{CEBA} LOW	5	—	5	—	ns
t _{SK(0)}	Output Skew ⁽²⁾	—	—	—	500	ps

NOTES:

1. See test circuits and waveforms. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

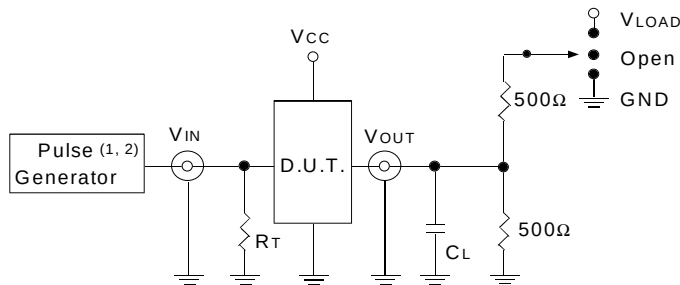
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} (1)= 3.3V ±0.3V	V _{CC} (1)= 2.7V	V _{CC} (2)= 2.5V ±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

LVC Link

TEST CIRCUITS FOR ALL OUTPUTS



LVC Link

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

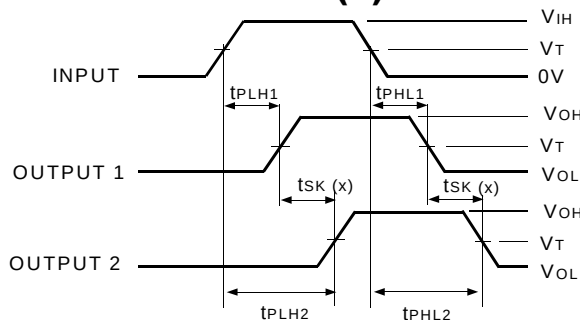
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

LVC Link

OUTPUT SKEW - t_{sk} (x)



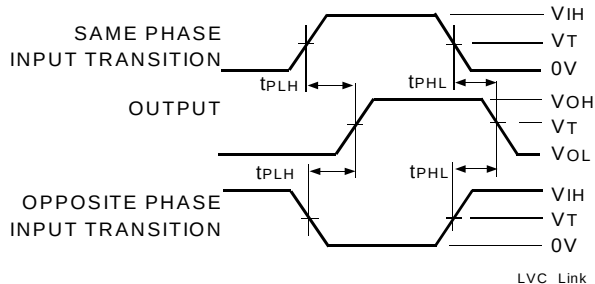
$$tsk(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

LVC Link

NOTES:

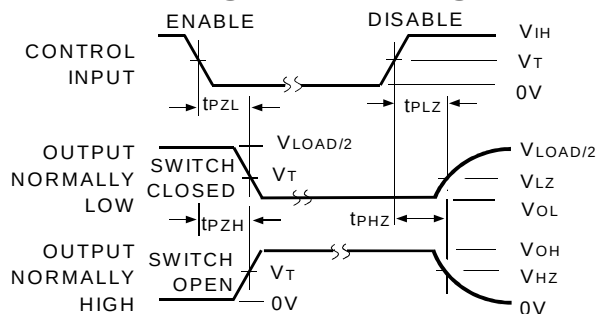
1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



LVC Link

ENABLE AND DISABLE TIMES

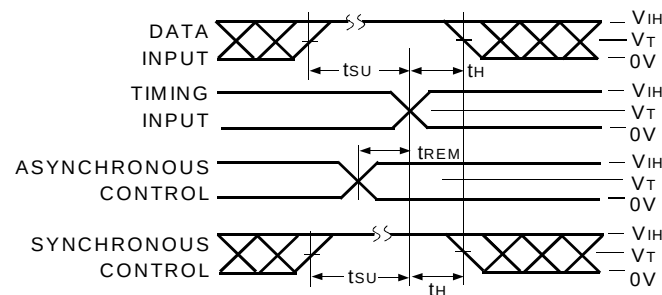


LVC Link

NOTE:

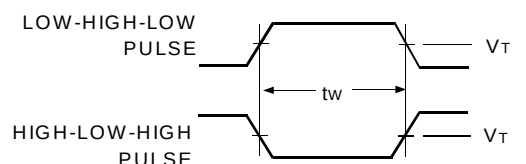
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



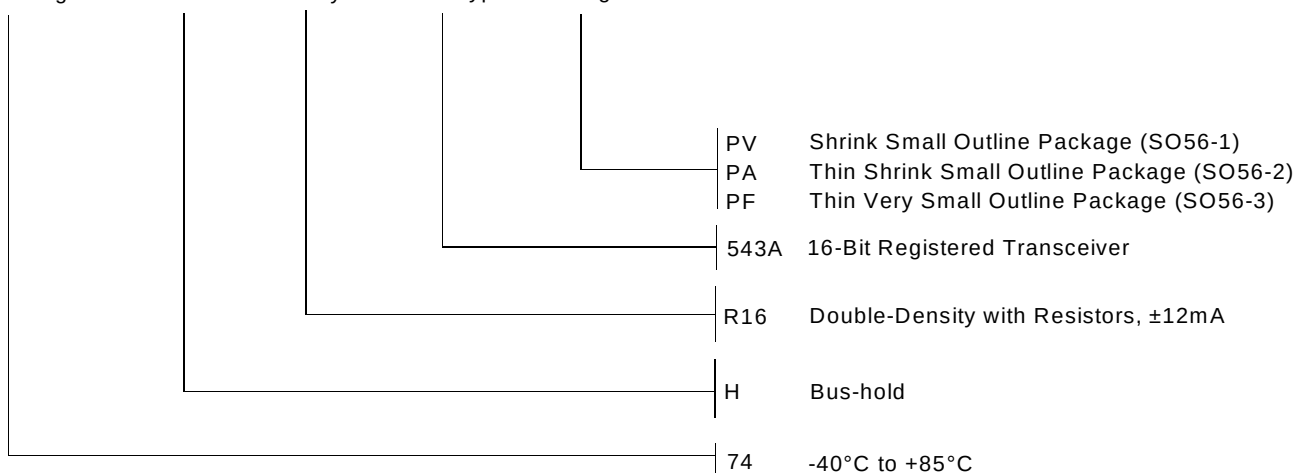
LVC Link

PULSE WIDTH



LVC Link

IDT XX LVC X XX XXXX XX
Temp. Range Bus-Hold Family Device Type Package



for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.jdt.com*

**To search for sales office near you, please click the sales button found on our home page or dial the 800# above and press 2.*