



GENERAL DESCRIPTION

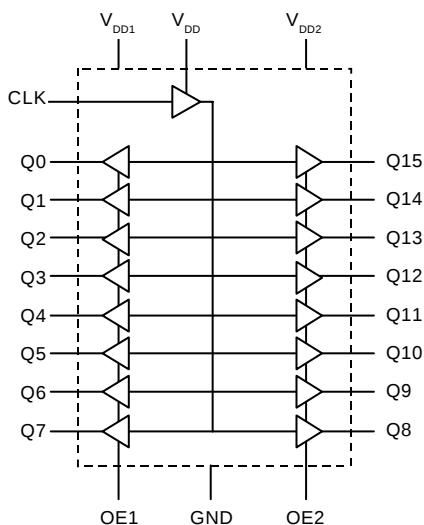


The ICS8343I is a low skew, 1-to-16 LVCMOS Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8343I is at 5.0V, 3.3V, 2.5V and mixed 3.3V input and 2.5V supply modes over the commercial temperature range. Guaranteed output and part-to-part skew characteristics make the ICS8343I ideal for those clock distribution applications demanding well defined performance and repeatability.

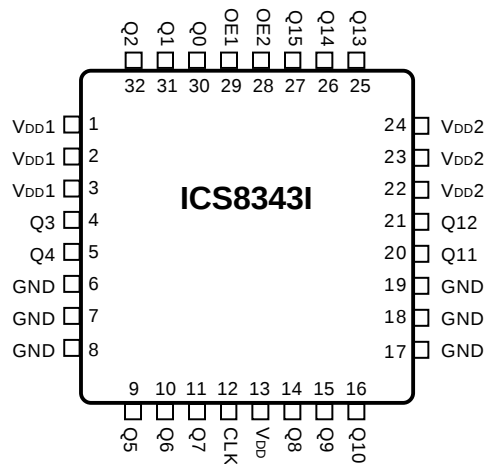
FEATURES

- 16 LVCMOS / LVTTTL outputs
- LVCMOS compatible clock input at 5V, LVTTTL and LVCMOS compatible at 3.3V and 2.5V
- Output frequency up to 200MHz
- Dual output enable inputs facilitates 1-to-16 or 1-to-8 input-to-output modes
- Output skew: 250ps (maximum)
- Part-to-part skew: 700ps (maximum)
- 5.0V, 3.3V, 2.5V or mixed 3.3V, 2.5V
- -40°C to 85°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP

7mm x 7mm x 1.4mm package body

Y package
(Top View)



TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2, 3	V _{DD1}	Power		Output Q0 thru Q7 power supply.
4, 5	Q3, Q4	Output		Clock outputs. 14Ω typical output impedance.
6, 7, 8, 17, 18, 19	GND	Power		Power supply ground.
9, 10, 11	Q5, Q6, Q7	Output		Clock outputs. 14Ω typical output impedance.
12	CLK	Input		Clock input. LVCMOS / LVTTTL interface levels.
13	V _{DD}	Power		Positive supply pin.
14, 15, 16	Q8, Q9, Q10	Output		Clock outputs. 14Ω typical output impedance.
20, 21	Q11, Q12	Output		Clock outputs. 14Ω typical output impedance.
22, 23, 24	V _{DD2}	Power		Output Q8 thru Q15 power supply.
25, 26, 27	Q13, Q14, Q15	Output		Clock outputs. 14Ω typical output impedance.
28	OE2	Input	Pullup	Output enable. When low forces outputs Q8 thru Q15 to HiZ state.
29	OE1	Input	Pullup	Output enable. When low forces outputs Q0 thru Q7 to HiZ state.
30, 31, 32	Q0, Q1, Q2	Output		Clock outputs. 14Ω typical output impedance.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance					pF
C _{PD}	Power Dissipation Capacitance (per output)	V _{DD1} , V _{DD2} = 5.25V		15		pF
		V _{DD1} , V _{DD2} = 3.47V		11		pF
		V _{DD1} , V _{DD2} = 2.63V		9.5		pF

TABLE 3. FUNCTION TABLE

Inputs		Outputs	
OE1	OE2	Q0:Q7	Q8:Q15
0	0	Hi Z	Hi Z
1	0	Active	Hi Z
0	1	Hi Z	Active
1	1	Active	Active



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	7V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, V_O	-0.5V to $V_{DDx} + 0.5V$
Ambient Operating Temperature	-40°C to 85°C
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DD1} = V_{DD2} = 3.3V \pm 5\%$, $T_A = -40^\circ$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DD1}, V_{DD2}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				100	μA

TABLE 4B. LVCMOS DC CHARACTERISTICS, $V_{DD} = V_{DD1} = V_{DD2} = 3.3V \pm 5\%$, $T_A = -40^\circ$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK	$V_{DD} = 3.465V$	2	$V_{DD} + 0.3$	V
		OEx	$V_{DD} = 3.465V$	2	$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	CLK	$V_{DD} = 3.135V$	-0.3	0.8	V
		OEx	$V_{DD} = 3.135V$	-0.3	0.8	V
I_{IH}	Input High Current	CLK	$V_{IN} = V_{DD}$		1	μA
		OEx	$V_{IN} = V_{DD}$		1	μA
I_{IL}	Input Low Current	CLK	$V_{IN} = 0V$	-15		μA
		OEx	$V_{IN} = 0V$	-15		μA
V_{OH}	Output High Voltage	$V_{DDx} = 3.135V, I_{OH} = -25mA$	2.4			V
V_{OL}	Output Low Voltage	$V_{DDx} = 3.135V, I_{OL} = 25mA$			0.8	V
I_{OZH}	High Impedance Leakage Current	OEx = 0V, $V_{OUT} = V_{DDx}$			1	μA
I_{OZL}	High Impedance Leakage Current	OEx = 0V, $V_{OUT} = 0V$	-1			μA



TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DD1} = V_{DD2} = 3.3V \pm 5\%$, $T_A = -40^\circ$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Input Frequency				200	MHz
tp_{LH}	Propagation Delay, Low-to-High;	$0 < f \leq 200MHz$	1	2.1	3.1	ns
tp_{HL}	Propagation Delay; High-to-Low;	$0 < f \leq 200MHz$	1.1	2	2.8	ns
$tsk(o)$	Output Skew; NOTE 3	Measured on rising edge @ $V_{DDX}/2$			250	ps
$tsk(pp)$	Part-to-Part Skew; NOTE 4	Measured on rising edge @ $V_{DDX}/2$			700	ps
t_R	Output Rise Time	$0 < f \leq 200MHz$		0.5	0.8	ns
t_F	Output Fall Time	$0 < f \leq 200MHz$		0.9	1.7	ns
t_{PW}	Output Pulse Width		$t_{CYCLE}/2 - 0.5$	$t_{CYCLE}/2$	$t_{CYCLE}/2 + 0.5$	ns

NOTE 1: All parameters measured at f_{MAX} unless noted otherwise.

NOTE 2: Outputs terminated with 50Ω resistor connected to $V_{DDX}/2$.

NOTE 3: Defined as skew across outputs at the same supply voltages and with equal load conditions.

NOTE 4: Defined as skew at different outputs on different devices operating at the same supply voltages and with equal load conditions.

TABLE 4C. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DD1} = V_{DD2} = 2.5V \pm 5\%$, $T_A = -40^\circ$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DD1}, V_{DD2}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				100	μA

TABLE 4D. LVCMOS DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DD1} = V_{DD2} = 2.5V \pm 5\%$, $T_A = -40^\circ$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK $V_{DD} = 3.465V$	2		$V_{DD} + 0.3$	V
		OEx $V_{DD} = 3.465V$	2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	CLK $V_{DD} = 3.135V$	-0.3		0.8	V
		OEx $V_{DD} = 3.135V$	-0.3		0.8	V
I_{IH}	Input High Current	CLK $V_{DD} = V_{IN}$			1	μA
		OEx $V_{DD} = V_{IN}$			1	μA
I_{IL}	Input Low Current	CLK $V_{IN} = 0V$	-15			μA
		OEx $V_{IN} = 0V$	-15			μA
V_{OH}	Output High Voltage	$V_{DDX} = 2.375V$, $I_{OH} = -25mA$	1.5			V
V_{OL}	Output Low Voltage	$V_{DDX} = 2.375V$, $I_{OL} = 25mA$			0.8	V
I_{OZH}	High Impedance Leakage Current	OEx = 0V, $V_{OUT} = V_{DDX}$			1	μA
I_{OZL}	High Impedance Leakage Current	OEx = 0V, $V_{OUT} = 0V$	-1			μA



TABLE 5B. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DD1} = V_{DD2} = 2.5V \pm 5\%$, $T_A = -40^\circ$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Input Frequency				200	MHz
tp_{LH}	Propagation Delay, Low-to-High;	$0 < f \leq 200MHz$	1	2.3	3.2	ns
tp_{HL}	Propagation Delay; High-to-Low;	$0 < f \leq 200MHz$	1.4	2.3	3.2	ns
$tsk(o)$	Output Skew; NOTE 3	Measured on rising edge @ $V_{DDX}/2$			250	ps
$tsk(pp)$	Part-to-Part Skew; NOTE 4	Measured on rising edge @ $V_{DDX}/2$			700	ps
t_R	Output Rise Time	$0 < f \leq 200MHz$		0.5	0.8	ns
t_F	Output Fall Time	$0 < f \leq 200MHz$		0.9	1.7	ns
t_{PW}	Output Pulse Width		$t_{CYCLE}/2 - 0.5$	$t_{CYCLE}/2$	$t_{CYCLE}/2 + 0.5$	ns

NOTE 1: All parameters measured at f_{MAX} unless noted otherwise.

NOTE 2: Outputs terminated with 50Ω resistor connected to $V_{DDX}/2$.

NOTE 3: Defined as skew across outputs at the same supply voltages and with equal load conditions.

NOTE 4: Defined as skew at different outputs on different devices operating at the same supply voltages and with equal load conditions.

TABLE 4E. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DD1} = V_{DD2} = 2.5V \pm 5\%$, $T_A = -40^\circ$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{DD1}, V_{DD2}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				100	μA

TABLE 4F. LVCMOS DC CHARACTERISTICS, $V_{DD} = V_{DD1} = V_{DD2} = 2.5V \pm 5\%$, $T_A = -40^\circ$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK $V_{DD} = 2.625V$	2		$V_{DD} + 0.3$	V
		OEx $V_{DD} = 2.625V$	2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	CLK $V_{DD} = 2.375V$	-0.3		0.8	V
		OEx $V_{DD} = 2.375V$	-0.3		0.8	V
I_{IH}	Input High Current	CLK $V_{DD} = V_{IN}$			1	μA
		OEx $V_{DD} = V_{IN}$			1	μA
I_{IL}	Input Low Current	CLK $V_{IN} = 0V$	-10			μA
		OEx $V_{IN} = 0V$	-10			μA
V_{OH}	Output High Voltage	$V_{DDX} = 2.375V$, $I_{OH} = -25mA$	1.5			V
V_{OL}	Output Low Voltage	$V_{DDX} = 2.375V$, $I_{OL} = 25mA$			0.8	V
I_{OZH}	High Impedance Leakage Current	OEx = 0V, $V_{OUT} = V_{DDX}$			1	μA
I_{OZL}	High Impedance Leakage Current	OEx = 0V, $V_{OUT} = 0V$	-1			μA



TABLE 5C. AC CHARACTERISTICS, $V_{DD} = V_{DD1} = V_{DD2} = 2.5V \pm 5\%$, $T_A = -40^\circ$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Input Frequency				133	MHz
t_{pLH}	Propagation Delay, Low-to-High;	$0 < f \leq 133\text{MHz}$	1	2.5	3.7	ns
t_{pHL}	Propagation Delay; High-to-Low;	$0 < f \leq 133\text{MHz}$	1.4	2.6	3.5	ns
$t_{sk(o)}$	Output Skew; NOTE 3	Measured on rising edge @ $V_{DDX}/2$			250	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 4	Measured on rising edge @ $V_{DDX}/2$			750	ps
t_R	Output Rise Time			0.5	0.8	ns
t_F	Output Fall Time			0.9	1.7	ns
t_{PW}	Output Pulse Width		$t_{CYCLE}/2 - 0.75$	$t_{CYCLE}/2$	$t_{CYCLE}/2 + 0.75$	ns

NOTE 1: All parameters measured at f_{MAX} unless noted otherwise.

NOTE 2: Outputs terminated with 50Ω resistor connected to $V_{DDX}/2$.

NOTE 3: Defined as skew across outputs at the same supply voltages and with equal load conditions.

NOTE 4: Defined as skew at different outputs on different devices operating at the same supply voltages and with equal load conditions.

TABLE 4G. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DD1} = V_{DD2} = 5V \pm 5\%$, $T_A = -40^\circ$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		4.75	5.0	5.25	V
V_{DD1}, V_{DD2}	Output Supply Voltage		4.75	5.0	5.25	V
I_{DD}	Power Supply Current				110	μA

TABLE 4H. LVCMOS DC CHARACTERISTICS, $V_{DD} = V_{DD1} = V_{DD2} = 5V \pm 5\%$, $T_A = -40^\circ$ TO $85^\circ C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK	$V_{DD} = 4.75V$	3.32		5.05	V
			$V_{DD} = 5.25V$	3.67		5.55	V
		OEx	$V_{DD} = 5.25V$	2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	CLK	$V_{DD} = 4.75V$	-0.3		1.42	V
			$V_{DD} = 5.25V$	-0.3		1.57	V
		OEx	$V_{DD} = 4.75V$	-0.3		0.8	V
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN} = 5.25V$			1	μA
		OEx	$V_{DD} = V_{IN} = 5.25$			1	μA
I_{IL}	Input Low Current	CLK	$V_{DD} = 5.25V, V_{IN} = 0V$	-40			μA
		OEx	$V_{DD} = 5.25V, V_{IN} = 0V$	-40			μA
V_{OH}	Output High Voltage		$V_{DDX} = 4.75V, I_{OH} = -25mA$	4			V
V_{OL}	Output Low Voltage		$V_{DDX} = 4.75V, I_{OL} = 25mA$			0.8	V
I_{OZH}	High Impedance Leakage Current		OEx = 0V, $V_{OUT} = V_{DDX}$			1	μA
I_{OZL}	High Impedance Leakage Current		OEx = 0V, $V_{OUT} = 0V$	-1			μA



TABLE 5D. AC CHARACTERISTICS, $V_{DD} = V_{DD1} = V_{DD2} = 5V \pm 5\%$, $T_A = -40^\circ$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Input Frequency				66	MHz
tp_{LH}	Propagation Delay, Low-to-High;	$0 < f \leq 66\text{MHz}$	0.9	1.4	1.8	ns
tp_{HL}	Propagation Delay; High-to-Low;	$0 < f \leq 66\text{MHz}$	0.9	1.4	1.9	ns
$t_{sk(o)}$	Output Skew; NOTE 3	Measured on rising edge @ $V_{DDX}/2$			350	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 4	Measured on rising edge @ $V_{DDX}/2$			700	ps
t_R	Output Rise Time	Measured from 0.8V to 2.0V		0.3	0.5	ns
t_F	Output Fall Time	Measured from 2.0V to 0.8V		0.3	0.4	ns
t_{PW}	Output Pulse Width		$t_{CYCLE}/2 - 0.75$	$t_{CYCLE}/2$	$t_{CYCLE}/2 + 0.75$	ns

NOTE 1: All parameters measured at f_{MAX} unless noted otherwise.

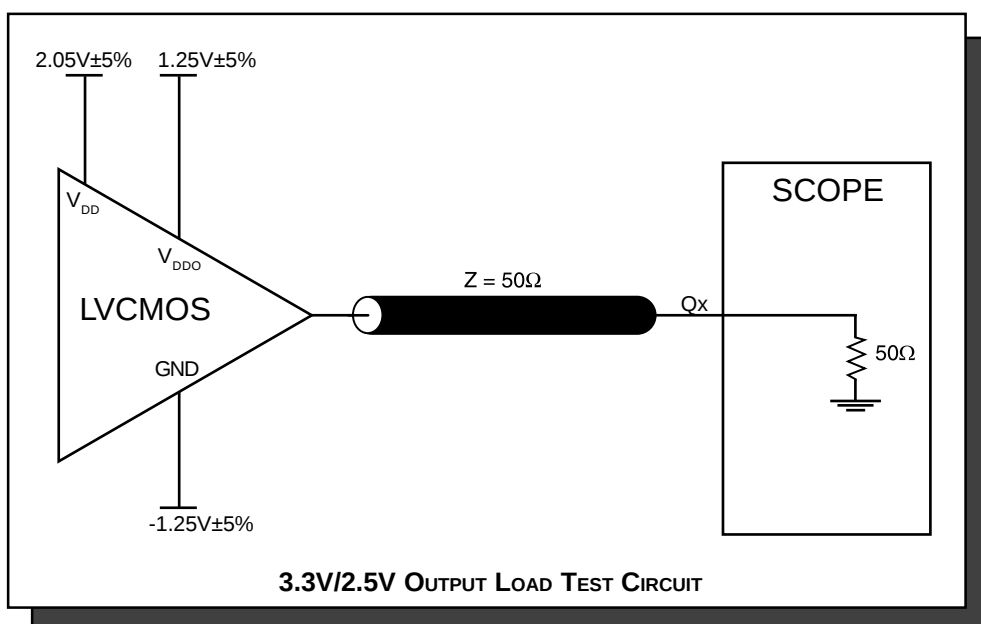
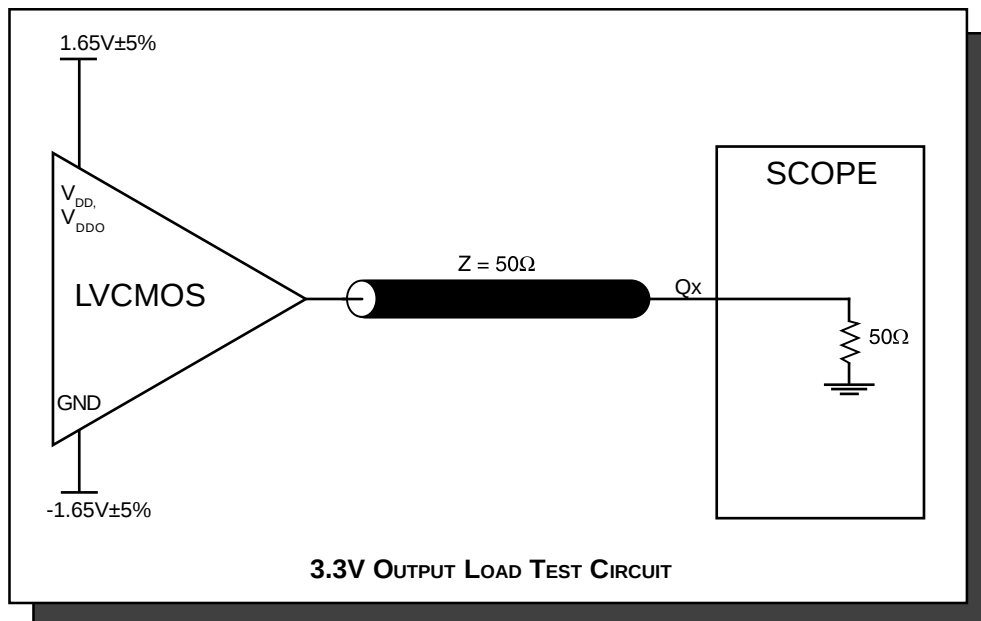
NOTE 2: Outputs terminated with 50Ω resistor connected to $V_{DDX}/2$.

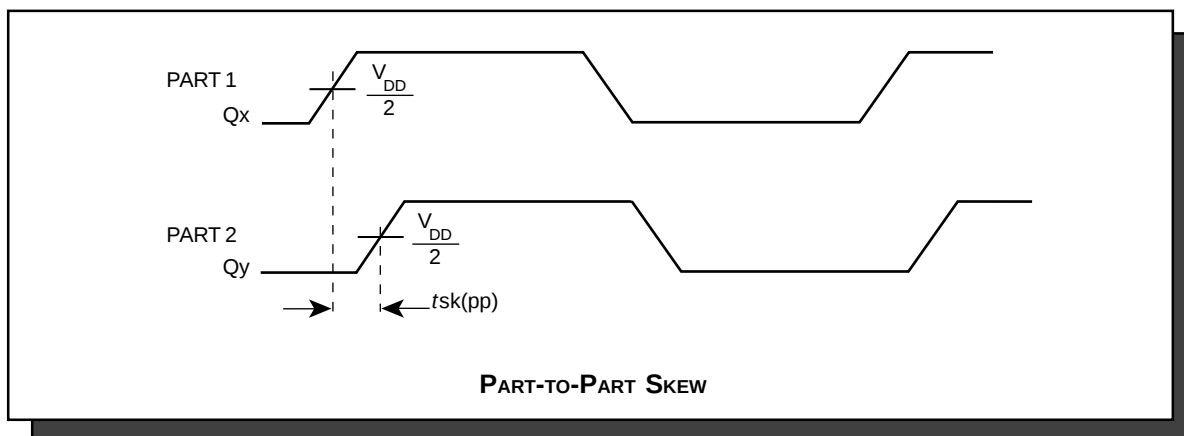
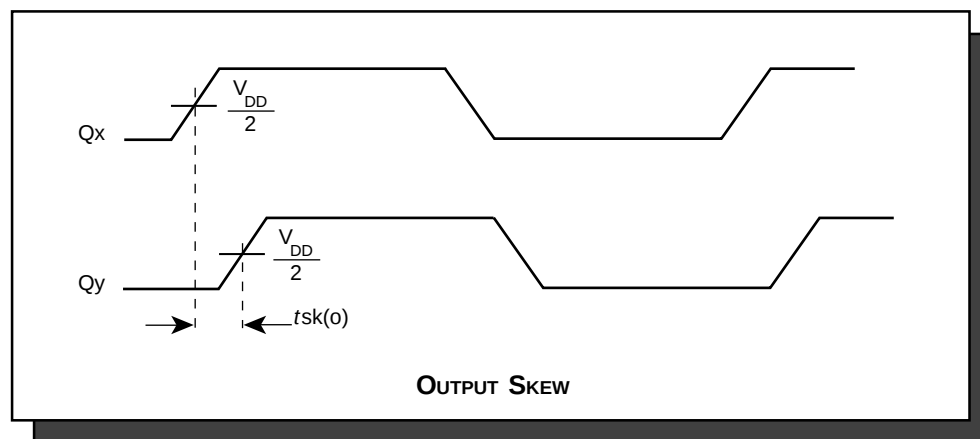
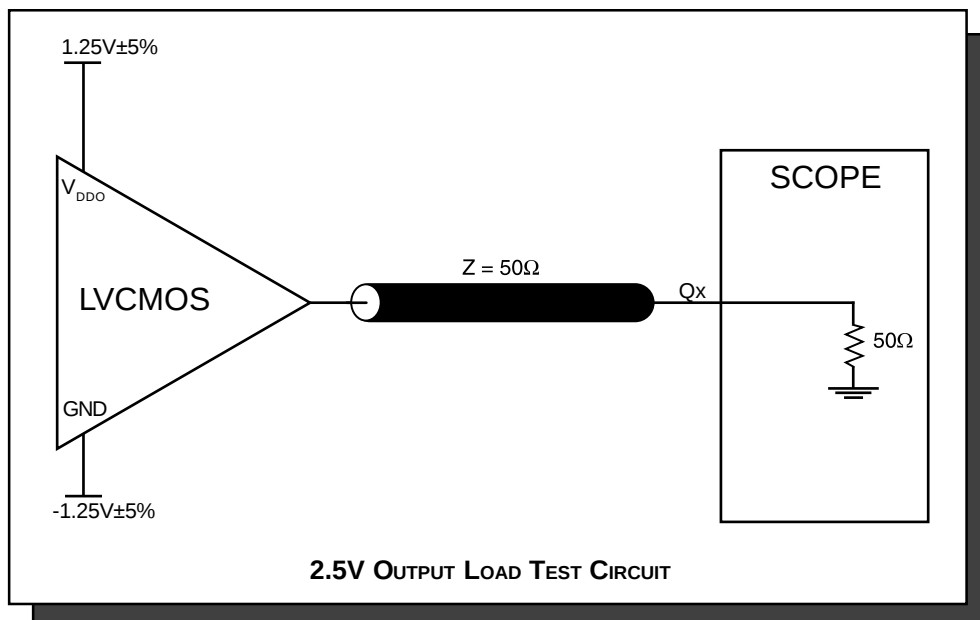
NOTE 3: Defined as skew across outputs at the same supply voltages and with equal load conditions.

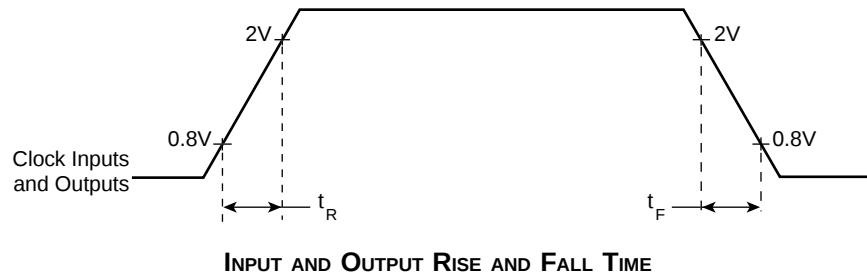
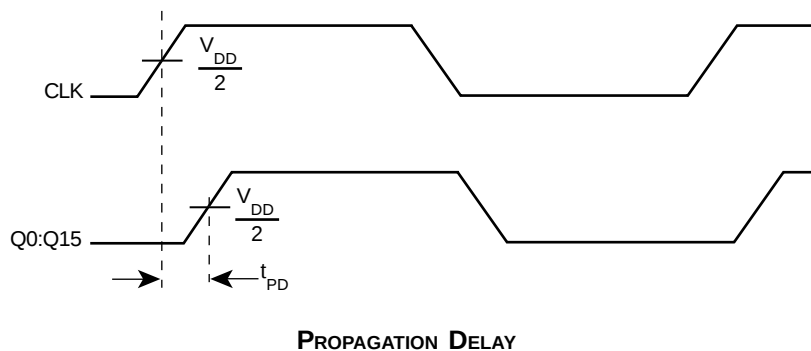
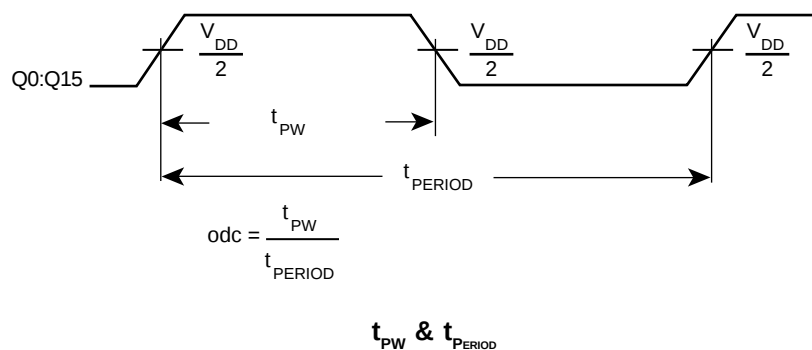
NOTE 4: Defined as skew at different outputs on different devices operating at the same supply voltages and with equal load conditions.



PARAMETER MEASUREMENT INFORMATION









RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

TRANSISTOR COUNT

The transistor count for ICS8343I is: 1939



PACKAGE OUTLINE - Y SUFFIX

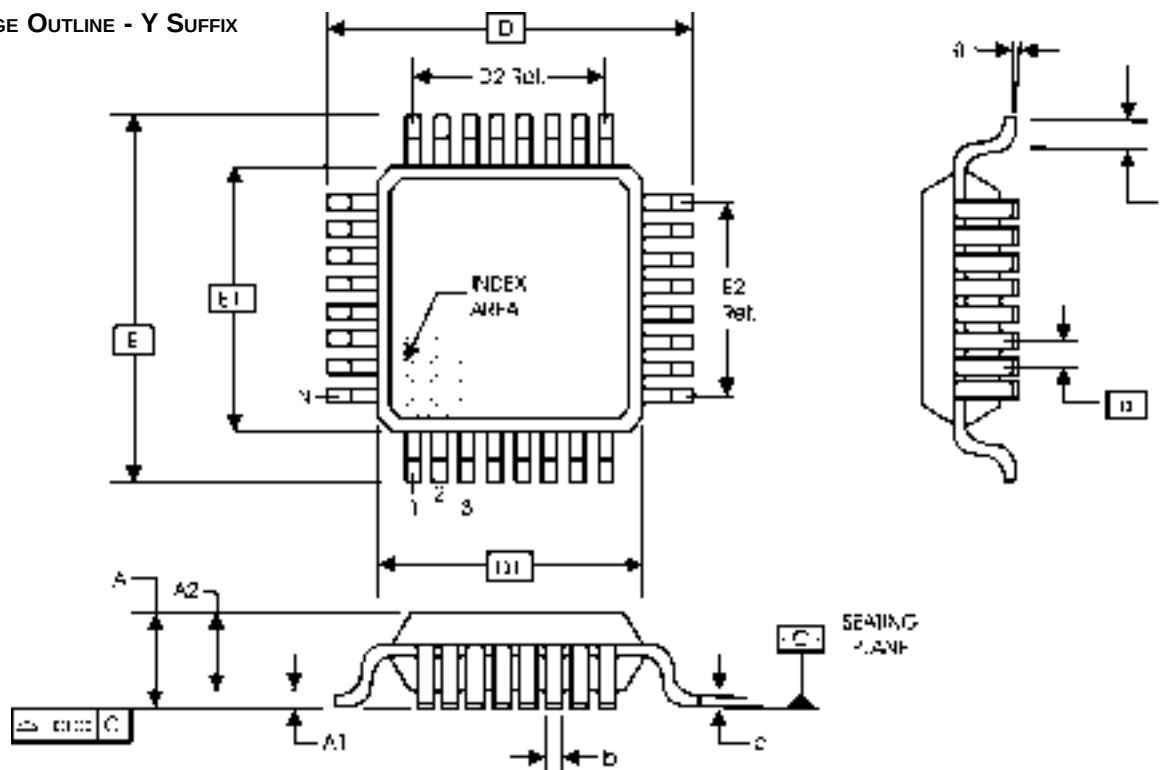


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.60 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.60 Ref.		
e	0.80 BASIC		
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026



Integrated
Circuit
Systems, Inc.

ICS8343I

LOW SKEW, 1-TO-16

LVCMOS FANOUT BUFFER

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8343YI	ICS8343YI	32 Lead LQFP	250 per tray	-40°C to 85°C
ICS8343YIT	ICS8343YI	32 Lead LQFP on Tape and Reel	2000	-40°C to 85°C

While the information presented herein has been checked for both accuracy and reliability, Integrated Circuit Systems, Incorporated (ICS) assumes no responsibility for either its use or for infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial and industrial applications. Any other applications such as those requiring high reliability, or other extraordinary environmental requirements are not recommended without additional processing by ICS. ICS reserves the right to change any circuitry or specifications without notice. ICS does not authorize or warrant any ICS product for use in life support devices or critical medical instruments.



Integrated
Circuit
Systems, Inc.

ICS8343I
LOW SKEW, 1-TO-16
LVCMOS FANOUT BUFFER

REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
D		8 - 10 11	Updated to new format. Added Parameter Measurement Information Section. Added Reliability Information Section.	05/08/02