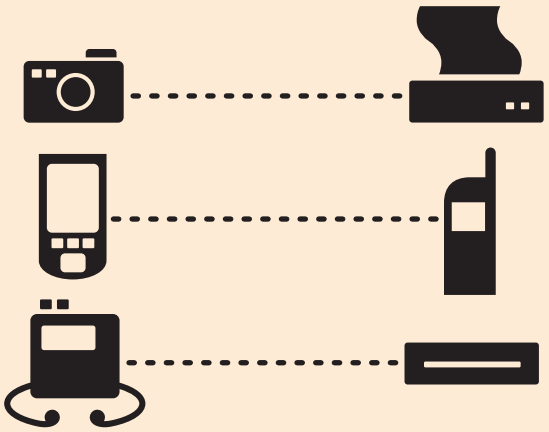
Single-chip USB OTG host and peripheral controller for point-to-point connectivity in embedded systems and peripherals

Philips ISP1362



FEATURES

- Incorporates OTG, host, and peripheral controller functionality on a single chip
- Fully compliant with USB Specification Rev. 2.0 (full speed and low speed) and the On-The-Go Supplement, Rev. 1.0
- Flexible hardware or software configuration of HNP and SRP for OTG dual-role devices
- USB host controller incorporates patent-pending architectural enhancements
  - requires minimal interrupts from CPU
  - enhanced control, bulk, interrupt, and isochronous data transfer performance maximizes transactions per frame, fully utilizing the 12 Mb/s USB full-speed bandwidth
- High-performance USB peripheral controller with integrated Serial Interface Engine, buffer memory, transceiver, and up to 14 programmable USB endpoints
- Dedicated physical buffer memories for host (4096 bytes) and peripheral (2462 bytes) controllers
- Two USB ports enable three application modes: OTG, host only (two ports), and simultaneous host and peripheral
- Efficient power management with support for suspend and remote wakeup
- High-speed, 16-bit PIO and DMA interface accommodates popular CPUs
- Uses 12-MHz or direct clock source with on-chip PLL for low EMI
- 3.3 V operating voltage with built-in charge pump for V_{BUS} generation
  - supports USB port voltage requirement of 4.0 to 5.5 V
  - optional support for external V_{BUS} source
  - output current adjustable with external capacitor
- Available in 64-pin LQFP or very-thin, 64-ball TFBGA packages for small form factor systems

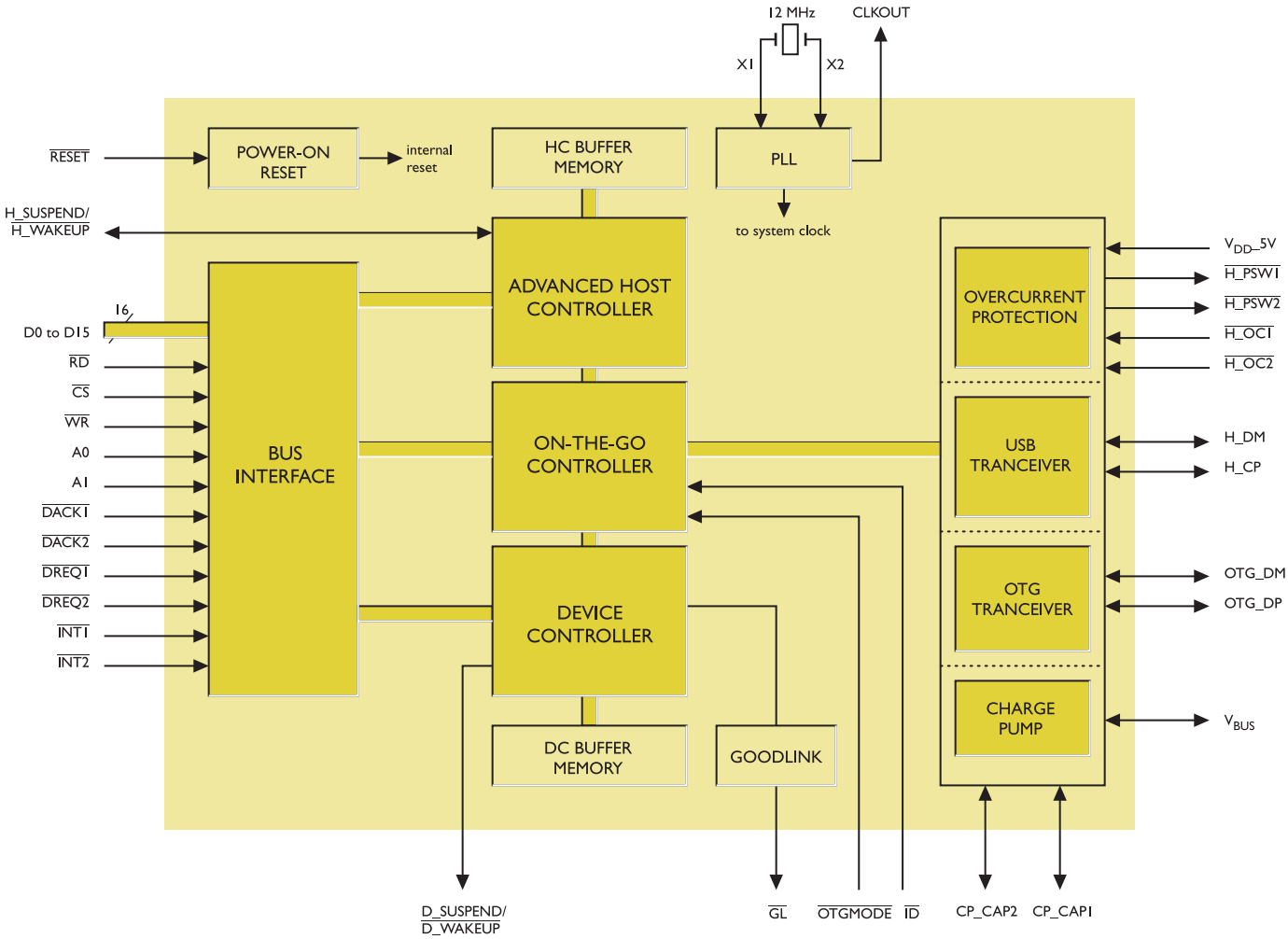
First in a family of Universal Serial Bus (USB) On-The-Go (OTG) solutions, the Philips ISP1362 integrates the functionality of an OTG controller, an advanced host controller and a Philips ISP1181-based peripheral controller onto a single chip. Fully compliant with the USB Specification Rev. 2.0 (full speed and low speed) and the On-The-Go Supplement, Rev. 1.0, the ISP1362 incorporates Philips patent-pending architectural enhancements to maximize utilization of the USB 2.0 specified 12 Mb/s full-speed bandwidth.

Using the ISP1362, developers can create OTG-compliant dual-role products capable of point-to-point communication, functioning as a host or traditional peripheral, and dynamically switching host/peripheral roles on demand. Its focus on power efficiency makes the ISP1362 ideal for small handheld devices for personal digital assistants (PDAs), digital cameras, MP3 digital audio players, mobile phones—any product where battery life and small, compact size are key.

USB ON-THE-GO

The recent extension of the USB 2.0 Specification to include On-The-Go functionality opens up many possibilities for more flexible, convenient use of small portable consumer devices. OTG gives traditional USB peripherals limited host capability, enabling them to communicate point-to-point with each other when a formal 'host' (commonly a PC) is not available. OTG products can also connect to traditional USB hosts or peripheral products, and some can switch host/peripheral roles on demand. For example, an OTG printer could switch from its traditional role as a peripheral to become a host for a digital camera so it can upload and print pictures.

OTG-compliant products hold the potential to increase productivity and simplify connectivity in a wide variety of everyday tasks such as file sharing, data synchronization, and uploading or downloading files. The OTG supplement also specifies power-saving features and new cabling options to promote acceptance in smaller battery-powered devices.



ISP1362 Architectural Block Diagram

FUNCTIONAL OVERVIEW

The ISP1362 comprises an OTG controller, a host controller and a peripheral controller connected to each other and to the external CPU through a data bus interface. Both host and peripheral controllers incorporate built-in memory to buffer USB traffic. An OTG transceiver, a charge pump for V_{BUS}, and pull-up and pull-down resistors are integrated on-chip to reduce the number and cost of external components.

USB OTG Controller—The ISP1362 OTG controller block provides all the control, monitoring, and switching functions required for OTG operations. It supports all functionality outlined by the OTG Supplement, Rev. 1.0.

When configured in OTG mode, the ISP1362 can function as either a host or a peripheral and supports the Host Negotiation Protocol (HNP) for switching between host and peripheral roles. It supports the Session Request Protocol (SRP) in both modes, enabling it to turn off V_{BUS} and respond to SRP when acting as host and initiate SRP to wakeup the host when acting as a peripheral. A set of OTG registers provides the control and status monitoring to support software HNP and SRP.

The ISP1362 supports use of both built-in and external voltage sources. For very low-power designs, an integrated charge pump eliminates the need for an external voltage source component. To support devices with higher power requirements, the ISP1362 also supports an external source for powering the USB bus.

Host controller optimized for embedded systems—The features and performance of embedded systems are often constrained by limited system resources, a compromise typically made for reasons of cost or size. The ISP1362 on-chip host controller takes advantage of many innovative architectural features to deliver robust system performance and highly optimized USB host functionality in embedded systems.

Enhancing the proven Philips ISP1161 controller, the ISP1362 uses a more robust and more advanced USB transfer data structure to fully utilize the USB bandwidth and deliver higher performance than its predecessor. It integrates four Kb of directly addressable on-chip buffer memory that can be updated on-the-fly. Patent-pending architectural features such as paired buffering for bulk transfer, multi-frame buffering for isochronous transfer, and an automatic interrupt polling rate for interrupt transfer enable the ISP1362 to achieve data transfer rates approaching the full 12 Mb/s bandwidth of the USB 2.0 full-speed standard.

Peripheral controller—The ISP1362 incorporates the market-proven Philips ISP1181 peripheral controller core. 2462 bytes of built-in buffer memory support the requirements of different applications. An efficient double buffering architecture maximizes data throughput.

As a peripheral controller, the ISP1362 supports two control endpoints and up to 14 endpoints that can be programmed to any of the four transfer types at both full speed and low speed.

Other on-chip components—In addition to the normal USB transceivers, the ISP1362 integrates the timers and analog components required for full OTG functionality. A 12- to 48-MHz clock multiplier phase-locked loop (PLL) enables use of a low-cost, 12-MHz crystal to minimize EMI due to low frequency operation. The ISP1362 also incorporates built-in overcurrent protection circuitry for use in non-OTG configurations (host and peripheral only). An on-chip 3.3 to 5 V charge pump adjusts the output current required to support a variety of different peripherals when the ISP1362 acts as a host.

Two ports/three operational USB modes—The ISP1362 provides two USB ports. Port 1 is software configurable and can function as a downstream, upstream, or OTG port. As an OTG port, port 1 can act in either host or peripheral modes and dynamically switch between roles through the HNP or when directed by a change in cabling. Port 2 is for downstream operation only.

MODE	PORT 1	PORT 2	APPLICATION
on-the-go	OTG	host	OTG application and a USB host as internal bus
host only	host	host	host only controller with two host ports
host/device	device	host	one host and one device (simultaneous operation supported)

EXTERNAL MICROPROCESSOR SUPPORT

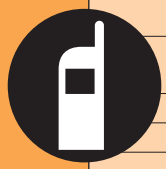
The ISP1362 supports a high-speed parallel interface to popular CPUs including Hitachi SH-3, Intel® StrongARM®, Philips XA, Fujitsu SPARCLite®, NEC and Toshiba MIPS, ARM7/9, Motorola DragonBall and PowerPC™ RISC. Support for both

USB OTG Applications

Connect a PDA to a . . .

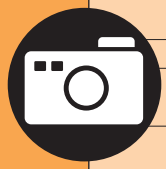
- **PDA** to exchange files
- **mobile phone** to surf the web, send e-mail
- **digital camera** to exchange pictures
- **keyboard** or **mouse** for user interface
- **printer** to print files or pictures
- **hard disk** to store data

Connect a mobile phone to a . . .



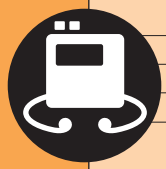
- **mobile phone** to exchange directories, messages, songs, applications, and more
- **PDA** to exchange files, surf the web
- **digital camera** to upload pictures
- **digital audio player** to exchange songs

Connect a digital camera to a . . .



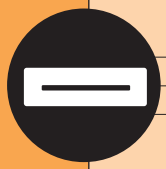
- **digital camera** to exchange pictures
- **mobile phone** to upload pictures to the web, send e-mail
- **printer** to print pictures

Connect a digital audio player to a . . .



- **digital audio player** to exchange songs
- **CD player** to upload songs
- **speakers** to play songs
- **hard disk** to store songs

Connect a portable hard disk to a . . .



- **digital audio player** to store songs
- **digital camera** to store pictures
- **digital camcorder** to store video clips

Connect a personal computer to a . . .

- **PDA** to synchronize data, transfer files
- **mobile phone** to synchronize data, use modem, transfer MP3 files
- **digital camera** to upload pictures
- **digital audio player** to upload/download songs
- **hard disk** to store data

PIO and DMA modes enables external CPU access to the ISP1362 internal buffer memories. Using PIO, an external CPU can also read or write to the ISP1362 internal control registers.

EFFICIENT POWER MANAGEMENT

When inactive, OTG devices normally power down their V_{BUS} and transceivers to conserve power, a desirable feature in small, portable products where power consumption or battery life is a key concern. To significantly reduce power consumption, the ISP1362 implements a power saving mode whenever the OTG device is not in a connected data-transfer session. In this mode, all controllers, the PLL, the oscillator, and the charge pump are placed in a suspend state. The ISP1362 LazyClock continues to run, however, allowing the device to respond to a wakeup event.

In accordance with the OTG specification, the ISP1362 fully supports the SRP. As a peripheral it can prompt the host to initiate bus activity; as a host it can respond to an SRP request. SRPs and other wakeup events can be individually enabled/disabled by programming bits and software registers.

OTG SOFTWARE SUPPORT

Philips Semiconductors offers a complete USB software solution for the ISP1362. The FlexiStack On-The-Go software suite combines the Philips FlexiStack USB host/peripheral stacks with On-The-Go control modules to support many popular real-time operating systems (RTOSs) such as VxWorks, pSOS, µITRON, WinCE, Linux, and DOS.

Optimized for Philips USB products, FlexiStack utilizes a modular approach that provides broad platform support and includes a complete library of class drivers for embedded systems. Written in the C programming language, Flexistack facilitates rapid porting to RTOSs and processors not already supported. The API of the On-The-Go controls can be used directly by the application program layers.

Philips also partners with third-party software companies to provide additional software stacks, fast porting services, and customization.

EVALUATION KITS AND REFERENCE DESIGNS

A variety of reference designs and evaluation kits are available. Visit *www.semiconductors.philips.com/buses/usb/products/otg/isp136x* for additional kit and ordering information.

> ISP1362 ISA/Linux On-The-Go Eval Kit

> ISP1362 ISA/DOS Mini Kit On-The-Go Eval Kit

> ISP1362 Cotulla/WinCE Reference Design

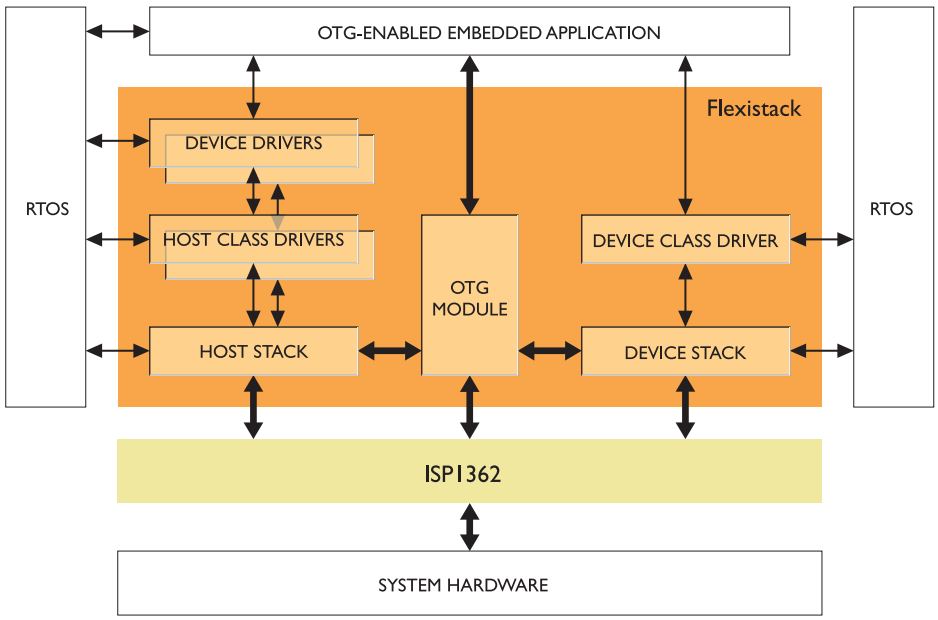
> ISP1362 Cotulla/PalmOS Reference Design

> ISP1362 Cotulla/Linux Reference Board

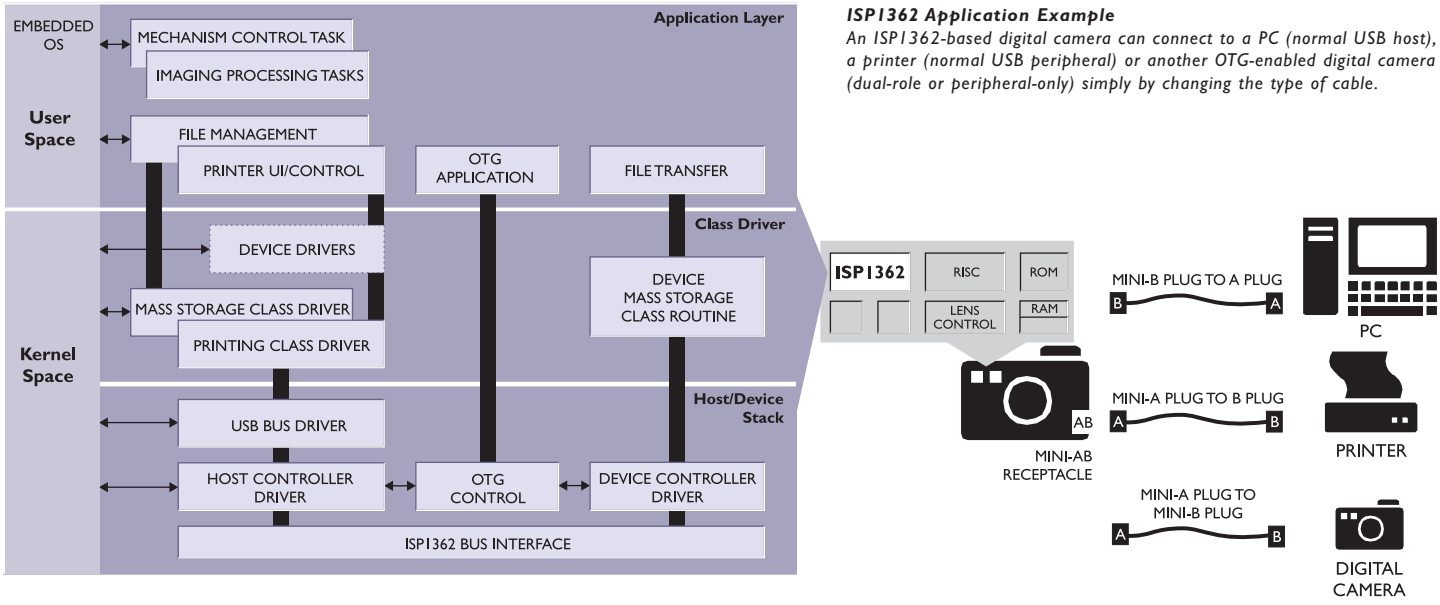
> ISP1362 PCI/Linux On-The-Go Eval Kit

> ISP1362 PCI/VxWorks On-The-Go Eval Kit

> ISP1362 PCI/µITRON On-The-Go Eval Kit



Philips FlexiStack On-The-Go Software Architecture



ISP1362 Application Example

An ISP1362-based digital camera can connect to a PC (normal USB host), a printer (normal USB peripheral) or another OTG-enabled digital camera (dual-role or peripheral-only) simply by changing the type of cable.

Philips ISP1362 Technical Specifications

STANDARDS COMPLIANCE

USB	Specification Rev. 2.0 (full-speed and low-speed)
OTG	On-The-Go Supplement, Rev 1.0

OTG CONTROLLER

Transfer modes	Control, bulk, interrupt and isochronous
OTG transceiver	Fully integrated; OTG compliant
HNP	Supported in hardware; status and control registers for software implementation
SRP	Supported in hardware; status and control registers for software implementation
Timers	Programmable high-resolution (0.01 ms to 80 sec)
Power	On-chip charge pump or external source

HOST CONTROLLER

Buffer memory	4096 bytes on-chip; directly addressable; updated on-the-fly
Patent-pending enhancements	Multi-frame buffering (isochronous transfer); automatic interrupt polling rate mechanism (interrupt transfer); paired buffering (bulk transfer) achieving up to 18 packets per frame for single bulk endpoint
Hub support	Standalone hubs

PERIPHERAL CONTROLLER

Buffer memory	2462 bytes on-chip; double buffered
Endpoints	Up to 14 programmable endpoints with double buffering; 2 fixed control I/O endpoints
Suspend support	Controllable LazyClock (110 ±50% kHz) output
GoodLink circuitry	Drives external LED for USB traffic indication
USB bus connection	Software-controlled pull-up resistor (SoftConnect™)

CHARGE PUMP

Output current	8 to 50 mA; adjustable by external capacitor

BUS INTERFACE AND USB PORTS

External CPU	High-speed, parallel interface with PIO and DMA Supports Hitachi SH-3, Intel® StrongARM®, Philips XA, Fujitsu SPARClite®, NEC and Toshiba MIPS, ARM7/9, Motorola DragonBall, PowerPC™ RISC and others
Ports	2 USB ports: port 1 software configurable to be host, peripheral, or OTG; port 2 is host only
Interrupts and DMA signals	Supports combined or separate interrupts and DMA signals for host and peripheral
Bus Interface	Supports 16-bit data bus PIO or DMA

CLOCK

Source	12 MHz crystal or direct clock source
PLL	On chip; low EMI

PHYSICAL

Temperature	Operating range: -40 to +85 °C
Packaging	ISP1362BD: 64-pin, plastic LQFP SOT314-2, 10 x 10 x 1.4 mm ISP1362EE: 64-ball, plastic TFBGA SOT543-1, 6 x 6 x 0.8 mm

ELECTRICAL

Power supply	Internal core: +3.3 V I/O: +3.3 V with 5 V tolerance
USB ports	USB bus voltage range (4.0 to 5.5 V); built-in over-current protection for host ports
V_{BUS} voltage	+5.0 V
V_{BUS} output current	8 to 50 mA (depending on external capacitor)

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North America
Philips Semiconductors C.R.M Center
2800 Wells Branch Parkway
Mailstop P-411
Austin, Texas 78728
United States

Tel: +1 800 234 7381
Fax: +1 800 943 0087
E-mail: P411webinq.smi@harte-hanks.com

Europe, Africa, Middle East and South America
Philips Semiconductors International
Fulfillment and Sales Support Center
P.O. Box 366
2700 AJ Zoetermeer
The Netherlands

Fax: +31 79 3685126

Asia Pacific
Philips Semiconductors Asia Pacific
Market Response Management Center
P.O. Box 68115
Kowloon East Post Office
Hong Kong

Fax: +852 2756 8271

Japan
Philips Semiconductors
Philips Building 13-37
Kohnan 2-chome
Minato-ku,
Tokyo 108-8507

Tel: +81 3 3740 5130
Fax: +81 3 3740 5057

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