DATA PATH INTERFACE (DPI) TO UTOPIA LEVEL 2 TRANSLATION DEVICE

PRELIMINARY
IDT77V011

Features

- Single chip interface between multiple UTOPIA PHYs and a single Data Path Interface (DPI).
- Ideal for xDSL DSLAM and 25Mbps switching applications.
- Supports ATM Forum UTOPIA Level 2 interface in both 8-bit and 16-bit modes.
- Supports UTOPIA Level 2 Cell Level Handshake.
- Supports up to 31 PHYs on the UTOPIA Level 2 interface.
- Supports either 4-bit or 8-bit DPI interface.
- Supports cell sizes from 52 to 56 bytes on the DPI interface.
- Supports DPI operation up to 50MHz.
- Either Utility Bus or Parallel Manager Management interface for configuring and reading status of PHY registers.
- In-Stream™ (In-band) programming for configuration of device and management interface communications.
- TAG Routing for flexibility in routing cells.
- Single +3.3V ± 0.3V power supply required.
- Inputs are +5.0V tolerant.

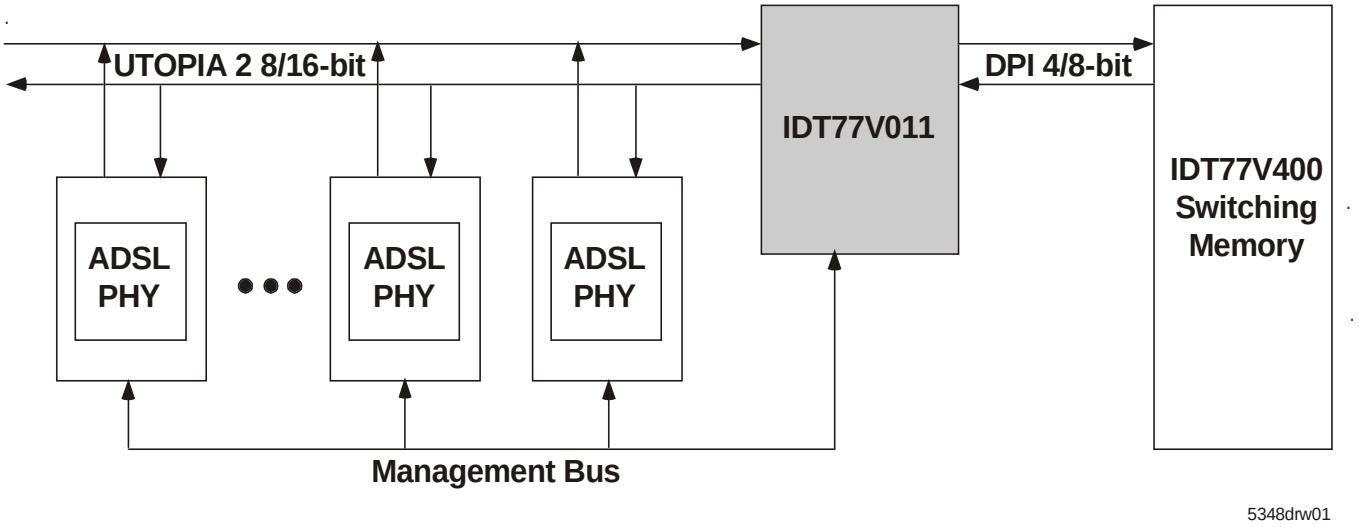


Figure 1: Typical IDT77V011 ADSL DSLAM Application with the IDT77v400 Switching Mmory.

Description

The IDT77V011provides the interface translation between a 4 or 8-bit Data Path Interface (DPI) and an 8 or 16-bit UTOPIA Level 2 interface. DPI offers a reduced device pin count and gives the IDT77V400 Switching Memory a high degree of port configuration flexibility.

By providing a smooth translation to the UTOPIA Level 2 multi-PHY interface, the IDT77V011 offers the opportunity to connect up to 31 PHY ports to a single 155Mbps port of the IDT77V400 Switching Memory.

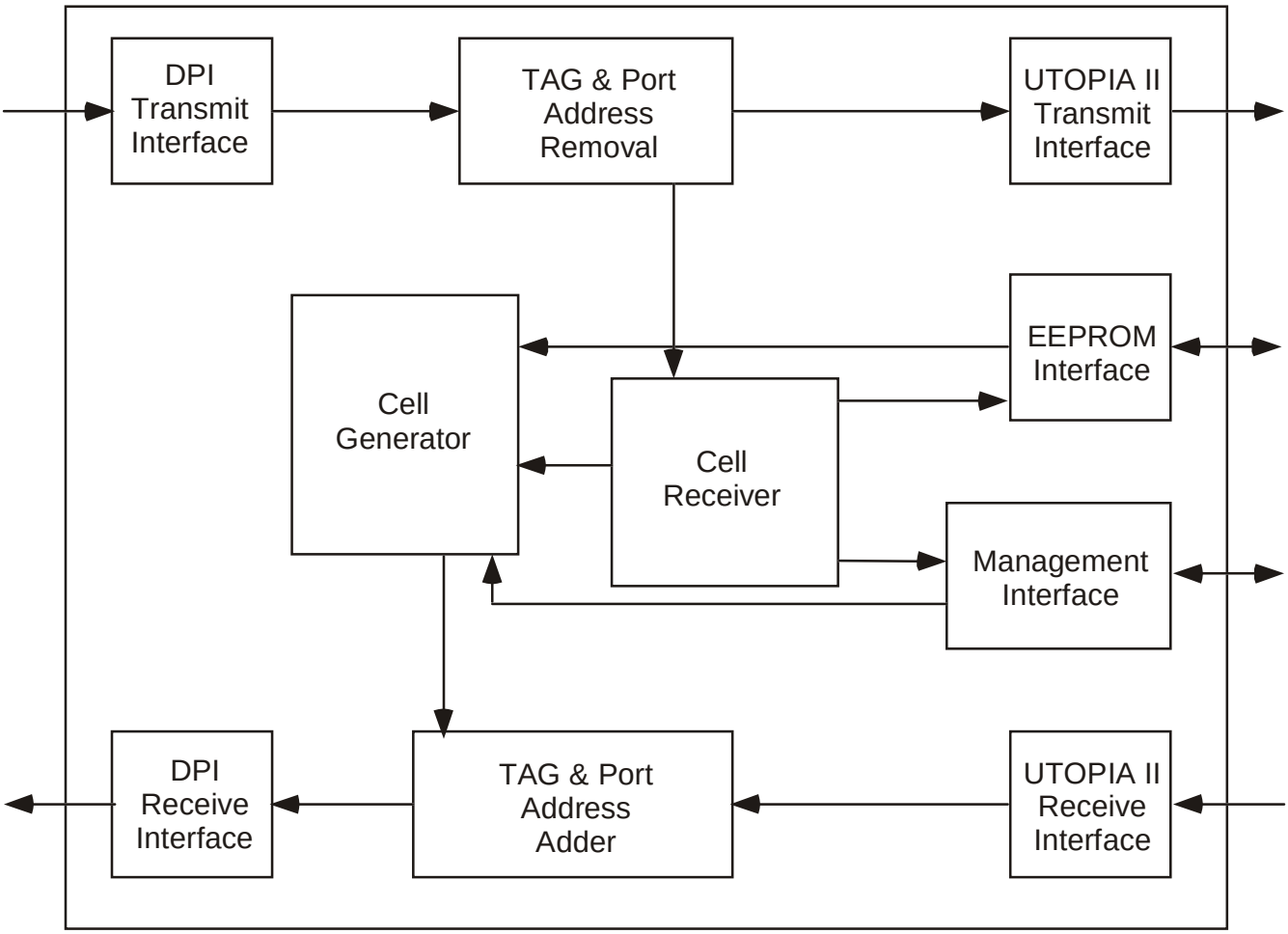
The IDT77V011 can also provide both transmit and receive TAG Routing, with each direction being individually programmed. In the receive direction up to four bytes can be added to the cell. In the transmit direction up to four bytes can be removed from the cell. This makes the IDT77V011, when combined with the IDT77V400, an ideal component for DSLAM and 25Mbps applications where the user would like to implement OC-3 bandwidth of a single IDT77V400 port to a number of lower bandwidth ports.

The 77V011 utilizes In-Stream™ programming for its device configuration options. The cells are received on the DPI transmit interface, indentified and sent to the internal cell interpreter for decoding and execution. In-Stream™ programming cells are transmitted based on a round-robin scheduler, which provides equal priority for each of the subports and the cell generator. This methodology is also used to communicate and configure the PHYs that are connected to the IDT77V011.

Other features include an EEPROM that holds information for initialization and Discovery/Identify cells, and a Management interface to access the PHY devices.

SPETEMBER 1999

Block Diagram



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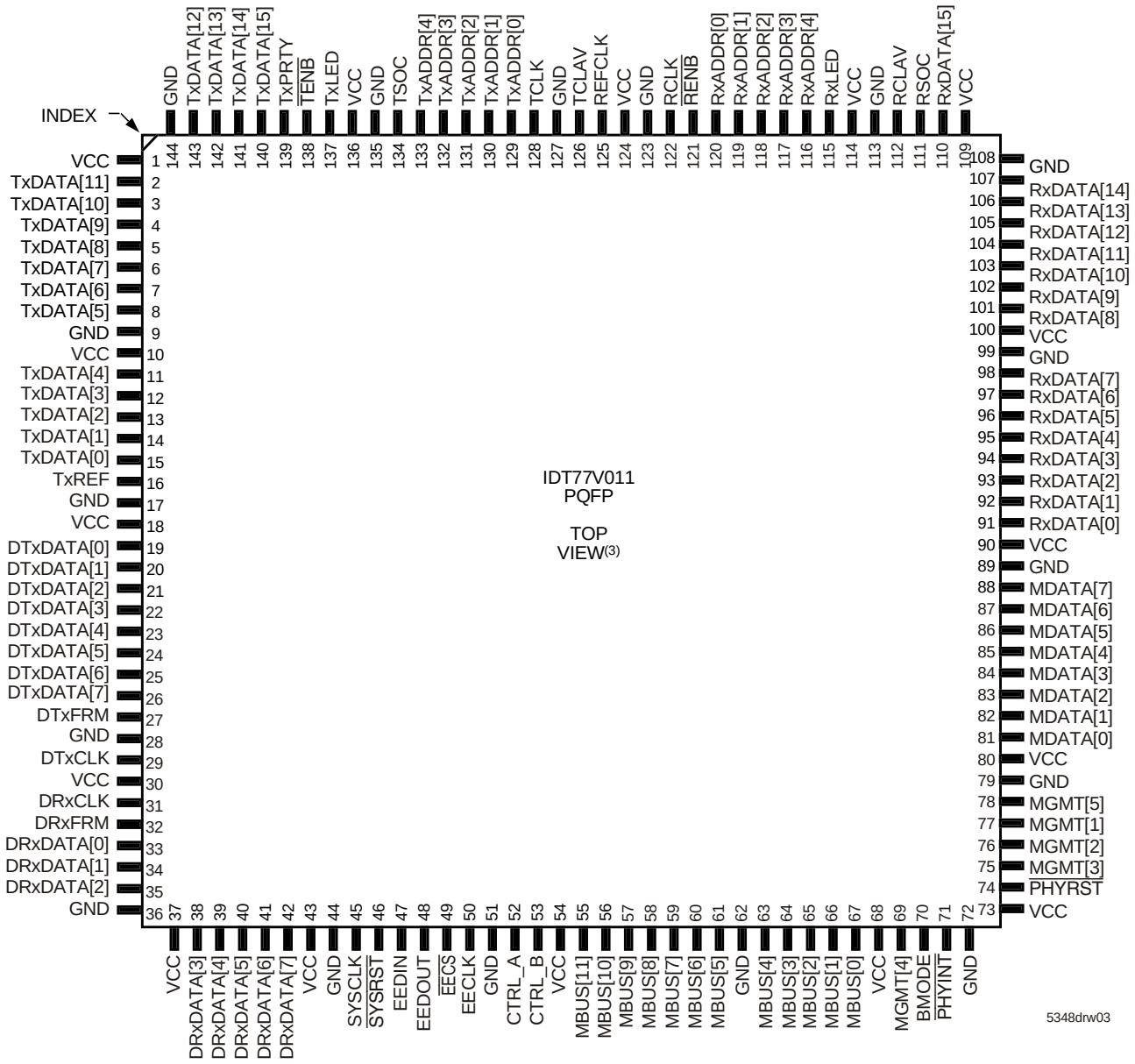
Pin Configuration



NOTES:

1. All power pins must be connected to a 3.3V ± 0.3V power supply.
2. All GND pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part-marking.

Pin Definitions

Pin Name	Pin Number	Input/ Output	Mode	Description
DTxDATA [0]	19	I	Normal	4-bit or 8-bit input data bus used to transfer data from a DPI device. When in 4-bit mode use DTxDATA [3:0].
DTxDATA [1]	20	I	Normal	4-bit or 8-bit input data bus used to transfer data from a DPI device. When in 4-bit mode use DTxDATA [3:0].
DTxDATA [2]	21	I	Normal	4-bit or 8-bit input data bus used to transfer data from a DPI device. When in 4-bit mode use DTxDATA [3:0].
DTxDATA [3]	22	I	Normal	4-bit or 8-bit input data bus used to transfer data from a DPI device. When in 4-bit mode use DTxDATA [3:0].
DTxDATA [4]	23	I	Normal	4-bit or 8-bit input data bus used to transfer data from a DPI device. When in 4-bit mode use DTxDATA [3:0].
DTxDATA [5]	24	I	Normal	4-bit or 8-bit input data bus used to transfer data from a DPI device. When in 4-bit mode use DTxDATA [3:0].
DTxDATA [6]	25	I	Normal	4-bit or 8-bit input data bus used to transfer data from a DPI device. When in 4-bit mode use DTxDATA [3:0].
DTxDATA [7]	26	I	Normal	4-bit or 8-bit input data bus used to transfer data from a DPI device. When in 4-bit mode use DTxDATA [3:0].
DTxFRM	27	I	Normal	DPI Transmit Start of Frame Marker.
DTxCLK	29	O	Normal	Transmit DPI Clock.
DRxDATA [0]	33	O	Normal	4-bit or 8-bit output data bus used to transfer data to a DPI device. When in 4-bit mode use DRxDATA [3:0].
DRxDATA [1]	34	O	Normal	4-bit or 8-bit output data bus used to transfer data to a DPI device. When in 4-bit mode use DRxDATA [3:0].
DRxDATA [2]	35	O	Normal	4-bit or 8-bit output data bus used to transfer data to a DPI device. When in 4-bit mode use DRxDATA [3:0].
DRxDATA [3]	38	O	Normal	4-bit or 8-bit output data bus used to transfer data to a DPI device. When in 4-bit mode use DRxDATA [3:0].
DRxDATA [4]	39	O	Normal	4-bit or 8-bit output data bus used to transfer data to a DPI device. When in 4-bit mode use DRxDATA [3:0].
DRxDATA [5]	40	O	Normal	4-bit or 8-bit output data bus used to transfer data to a DPI device. When in 4-bit mode use DRxDATA [3:0].
DRxDATA [6]	41	O	Normal	4-bit or 8-bit output data bus used to transfer data to a DPI device. When in 4-bit mode use DRxDATA [3:0].
DRxDATA [7]	42	O	Normal	4-bit or 8-bit output data bus used to transfer data to a DPI device. When in 4-bit mode use DRxDATA [3:0].
DRxFRM	32	O	Normal	DPI Receive Start of Frame Marker.
DRxCLK	31	I/O	Normal	Receive DPI Clock.
RxDATA [0]	91	I	Normal	8-bit or 16-bit UTOPIA 2 input data bus used to transfer data from a PHY device. When in 8-bit mode use RxDATA [7:0].
RxDATA [1]	92	I	Normal	8-bit or 16-bit UTOPIA 2 input data bus used to transfer data from a PHY device. When in 8-bit mode use RxDATA [7:0].
RxDATA [2]	93	I	Normal	8-bit or 16-bit UTOPIA 2 input data bus used to transfer data from a PHY device. When in 8-bit mode use RxDATA [7:0].
RxDATA [3]	94	I	Normal	8-bit or 16-bit UTOPIA 2 input data bus used to transfer data from a PHY device. When in 8-bit mode use RxDATA [7:0].
RxDATA [4]	95	I	Normal	8-bit or 16-bit UTOPIA 2 input data bus used to transfer data from a PHY device. When in 8-bit mode use RxDATA [7:0].
RxDATA [5]	96	I	Normal	8-bit or 16-bit UTOPIA 2 input data bus used to transfer data from a PHY device. When in 8-bit mode use RxDATA [7:0].
RxDATA [6]	97	I	Normal	8-bit or 16-bit UTOPIA 2 input data bus used to transfer data from a PHY device. When in 8-bit mode use RxDATA [7:0].
RxDATA [7]	98	I	Normal	8-bit or 16-bit UTOPIA 2 input data bus used to transfer data from a PHY device. When in 8-bit mode use RxDATA [7:0].
RxDATA [8]	101	I	Normal	8-bit or 16-bit UTOPIA 2 input data bus used to transfer data from a PHY device. When in 8-bit mode use RxDATA [7:0].
RxDATA [9]	102	I	Normal	8-bit or 16-bit UTOPIA 2 input data bus used to transfer data from a PHY device. When in 8-bit mode use RxDATA [7:0].
RxDATA [10]	103	I	Normal	8-bit or 16-bit UTOPIA 2 input data bus used to transfer data from a PHY device. When in 8-bit mode use RxDATA [7:0].

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Pin Definitions (con't.)

Pin Name	Pin Number	Input/ Output	Mode	Description
RxDATA [11]	104	I	Normal	8-bit or 16-bit UTOPIA 2 input data bus used to transfer data from a PHY device. When in 8-bit mode use RxDATA [7:0].
RxDATA [12]	105	I	Normal	8-bit or 16-bit UTOPIA 2 input data bus used to transfer data from a PHY device. When in 8-bit mode use RxDATA [7:0].
RxDATA [13]	106	I	Normal	8-bit or 16-bit UTOPIA 2 input data bus used to transfer data from a PHY device. When in 8-bit mode use RxDATA [7:0].
RxDATA [14]	107	I	Normal	8-bit or 16-bit UTOPIA 2 input data bus used to transfer data from a PHY device. When in 8-bit mode use RxDATA [7:0].
RxDATA [15]	110	I	Normal	8-bit or 16-bit UTOPIA 2 input data bus used to transfer data from a PHY device. When in 8-bit mode use RxDATA [7:0].
RSOC	111	I	Normal	UTOPIA 2 Receive Start of Cell marker.
RCLAV	112	I	Normal	UTOPIA 2 Receive Cell Available.
$\overline{\text{RENB}}$	121	O	Normal	UTOPIA 2 Receive Enable.
RxADDR [0]	120	O	Normal	UTOPIA 2 Receive Address Bus.
RxADDR [1]	119	O	Normal	UTOPIA 2 Receive Address Bus.
RxADDR [2]	118	O	Normal	UTOPIA 2 Receive Address Bus.
RxADDR [3]	117	O	Normal	UTOPIA 2 Receive Address Bus.
RxADDR [4]	116	O	Normal	UTOPIA 2 Receive Address Bus.
RxLED	115	O	Normal	UTOPIA 2 Receive LED.
RCLK	122	O	Normal	UTOPIA 2 Receive Clock.
TxDATA [0]	15	O	Normal	8-bit or 16-bit UTOPIA 2 output data bus used to transfer data to a PHY device. When in 8-bit mode use TxDATA [7:0].
TxDATA [1]	14	O	Normal	8-bit or 16-bit UTOPIA 2 output data bus used to transfer data to a PHY device. When in 8-bit mode use TxDATA [7:0].
TxDATA [2]	13	O	Normal	8-bit or 16-bit UTOPIA 2 output data bus used to transfer data to a PHY device. When in 8-bit mode use TxDATA [7:0].
TxDATA [3]	12	O	Normal	8-bit or 16-bit UTOPIA 2 output data bus used to transfer data to a PHY device. When in 8-bit mode use TxDATA [7:0].
TxDATA [4]	11	O	Normal	8-bit or 16-bit UTOPIA 2 output data bus used to transfer data to a PHY device. When in 8-bit mode use TxDATA [7:0].
TxDATA [5]	8	O	Normal	8-bit or 16-bit UTOPIA 2 output data bus used to transfer data to a PHY device. When in 8-bit mode use TxDATA [7:0].
TxDATA [6]	7	O	Normal	8-bit or 16-bit UTOPIA 2 output data bus used to transfer data to a PHY device. When in 8-bit mode use TxDATA [7:0].
TxDATA [7]	6	O	Normal	8-bit or 16-bit UTOPIA 2 output data bus used to transfer data to a PHY device. When in 8-bit mode use TxDATA [7:0].
TxDATA [8]	5	O	Normal	8-bit or 16-bit UTOPIA 2 output data bus used to transfer data to a PHY device. When in 8-bit mode use TxDATA [7:0].
TxDATA [9]	4	O	Normal	8-bit or 16-bit UTOPIA 2 output data bus used to transfer data to a PHY device. When in 8-bit mode use TxDATA [7:0].
TxDATA [10]	3	O	Normal	8-bit or 16-bit UTOPIA 2 output data bus used to transfer data to a PHY device. When in 8-bit mode use TxDATA [7:0].
TxDATA [11]	2	O	Normal	8-bit or 16-bit UTOPIA 2 output data bus used to transfer data to a PHY device. When in 8-bit mode use TxDATA [7:0].
TxDATA [12]	143	O	Normal	8-bit or 16-bit UTOPIA 2 output data bus used to transfer data to a PHY device. When in 8-bit mode use TxDATA [7:0].
TxDATA [13]	142	O	Normal	8-bit or 16-bit UTOPIA 2 output data bus used to transfer data to a PHY device. When in 8-bit mode use TxDATA [7:0].
TxDATA [14]	141	O	Normal	8-bit or 16-bit UTOPIA 2 output data bus used to transfer data to a PHY device. When in 8-bit mode use TxDATA [7:0].
TxDATA [15]	140	O	Normal	8-bit or 16-bit UTOPIA 2 output data bus used to transfer data to a PHY device. When in 8-bit mode use TxDATA [7:0].
TSOC	134	O	Normal	UTOPIA 2 Transmit Start of Cell marker.
TCLAV	126	I	Normal	UTOPIA 2 Transmit Cell Available.
$\overline{\text{TENB}}$	138	O	Normal	UTOPIA 2 Transmit Enable.

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Pin Definitions (con't.)

Pin Name	Pin Number	Input/ Output	Mode	Description
TxADDR[0]	129	O	Normal	UTOPIA 2 Transmit Address Bus [LSB].
		I	Reset	Subport Byte Location. Indicates what byte the Tx and Rx Subport Address is located in [LSB].
TxADDR[1]	130	O	Normal	UTOPIA 2 Transmit Address Bus [LSB+1].
		I	Reset	Subport Byte Location. Indicates what byte the Tx and Rx Subport Address is located in [LSB+1].
TxADDR[2]	131	O	Normal	UTOPIA 2 Transmit Address Bus [LSB+2].
		I	Reset	Subport Byte Location. Indicates what byte the Tx and Rx Subport Address is located in [MSB].
TxADDR[3]	132	O	Normal	UTOPIA 2 Transmit Address Bus [LSB+3].
		I	Reset	Initialize from EEPROM. Selects whether five bytes of EEPROM are to be written to In-Stream™ Cell Header and In-Stream™ Subport. "0" do not write five byte value, "1" write five byte value from EEPROM.
TxADDR[4]	133	O	Normal	UTOPIA 2 Transmit Address Bus [MSB].
TxLED	137	O	Normal	UTOPIA 2 Transmit LED.
TCLK	128	O	Normal	UTOPIA 2 Transmit Clock.
TxPRTY	139	O	Normal	Parity for DTxDATA [15:0].
REFCLK	125	I	Normal	8 KHz reference clock used to generate TxREF.
TxREF	16	O	Normal	8KHz reference clock used by PHY.
EECLK	50	O	Normal	EEPROM Clock.
$\overline{\text{EECS}}$	49	O	Normal	EEPROM Chip Select.
EEDIN	47	I	Normal	Serial Input from the EEPROM.
EEDOUT	48	O	Normal	Serial Output to the EEPROM.
BMODE	70	I	Normal	Bus Mode. Selects Motoral or Intel bus mode. "0" selects Motorola, "1" selects Intel.
MBUS[0]	67	O	UTOPIA 2	Address Bus. Upper 64 bytes used for 32 address pointers describing PHY's.
			Utility Bus	Utility bus PHY chip select (CS[1]).
		I	Reset	TxSIZE[0] - Number of bytes to remove from cell in transmit direction (LSB).
MBUS[1]	66	O	UTOPIA 2	Address bus. Upper 64 bytes used for 32 address pointers describing PHY's.
			Utility Bus	Utility bus PHY chip select (CS[2]).
		I	Reset	TxSIZE[1] - number of bytes to remove from cell in transmit direction (LSB + 1).
MBUS[2]	65	O	UTOPIA 2	Address bus. Upper 64 bytes used for 32 address pointers describing PHY's.
			Utility Bus	Utility bus PHY chip select (CS[3]).
		I	Reset	TxSIZE[2] - number of bytes to remove from cell in transmit direction (MSB).
MBUS[3]	64	O	UTOPIA 2	Address bus. Upper 64 bytes used for 32 address pointers describing PHY's.
			Utility Bus	Utility bus PHY chip select (CS[4]).
		I	Reset	TxLOC - Location of Tx TAG in cell. "0" TAG located at beginning of cell, "1" TAG located at end of cell.
MBUS[4]	63	O	UTOPIA 2	Address bus. Upper 64 bytes used for 32 address pointers describing PHY's.
			Utility Bus	Utility bus PHY chip select (CS[5]).
		I	Reset	TxHEC - Add HEC placeholder. "0" donot add placeholder, "1" add placeholder.
MBUS[5]	61	O	UTOPIA 2	Address bus. Upper 64 bytes used for 32 address pointers describing PHY's.
			Utility Bus	Utility bus PHY chip select (CS[6]).
		I	Reset	RxSIZE[0] - Number of bytes to add to cell in the receive direction (LSB).
MBUS[6]	60	O	UTOPIA 2	Address bus. Upper 64 bytes used for 32 address pointers describing PHY's.
			Utility Bus	Utility bus PHY chip select (CS[7]).
		I	Reset	RxSIZE[1] - Number of bytes to add to cell in the receive direction (LSB + 1).

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Pin Definitions (con't.)

Pin Name	Pin Number	Input/ Output	Mode	Description
MBUS[7]	59	O	UTOPIA 2	Address bus. Upper 64 bytes used for 32 address pointers describing PHY's.
			Utility Bus	Utility bus PHY chip select (CS[8]).
		I	Reset	RxSIZE[2] - Number of bytes to add to cell in the receive direction (MSB).
MBUS[8]	58	O	UTOPIA 2	Address bus. Upper 64 bytes used for 32 address pointers describing PHY's.
			Utility Bus	Utility bus PHY chip select (CS[9]).
		I	Reset	RxLOC - Location of TAG in cell int he receive direction. RxLOC = "0" TAG located at beginning of cell, TxLOC = "1" TAG located at end of cell.
MBUS[9]	57	O	UTOPIA 2	Address bus (LSB+9).
			Utility Bus	Utility bus PHY chip select (CS[10]).
		I	Reset	RxHEC - Remove HEC from cell. "0" donot remove HEC, "1" remove HEC.
MBUS[10]	56	O	UTOPIA 2	Address bus. Upper 64 bytes used for 32 address pointers describing PHY's.
			Utility Bus	Utility bus PHY chip select (CS[11]).
		I	Reset	DPI Bus Size. Indicates whether DPI transmit and receive bus is 4-bits or 8-bits wide. "0" 4-bit DPI bus, "1" 8-bit DPI bus.
MBUS[11]	55	O	UTOPIA 2	Address bus. Upper 64 bytes used for 32 address pointers describing PHY's.
			Utility Bus	Utility bus PHY chip select (CS[12]).
		I	Reset	UTOPIA Bus Size. Indicates whether the UTOPIA transmit and receive data bus is 8-bits or 16-bits wide. "0" 8-bit UTOPIA bus, "1" 16-bit UTOPIA bus.
MDATA[0]	81	I/O	UTOPIA 2	Management interface data bus [LSB].
			Utility Bus	Utility Bus address and data bus [LSB].
MDATA[1]	82	I/O	UTOPIA 2	Management interface data bus [LSB+1].
			Utility Bus	Utility Bus address and data bus [LSB+1].
MDATA[2]	83	I/O	UTOPIA 2	Management interface data bus [LSB+2].
			Utility Bus	Utility Bus address and data bus [LSB+2].
MDATA[3]	84	I/O	UTOPIA 2	Management interface data bus [LSB+3].
			Utility Bus	Utility Bus address and data bus [LSB+3].
MDATA[4]	85	I/O	UTOPIA 2	Management interface data bus [LSB+4].
			Utility Bus	Utility Bus address and data bus [LSB+4].
MDATA[5]	86	I/O	UTOPIA 2	Management interface data bus [LSB+5].
			Utility Bus	Utility Bus address and data bus [LSB+5].
MDATA[6]	87	I/O	UTOPIA 2	Management interface data bus [LSB+6].
			Utility Bus	Utility Bus address and data bus [LSB+6].
MDATA[7]	88	I/O	UTOPIA 2	Management interface data bus [MSB].
			Utility Bus	Utility Bus address and data bus [MSB].
MGMT[1]	77	O	UTOPIA 2	Validates Read or Write operation on Management interface ($\overline{SEL}$).
			Utility Bus	Utility bus PHY Chip Select (CS[0]).
MGMT[2]	76	O	UTOPIA II	Management interface Read or Data Strobe ($\overline{RD/DS}$).
			Utility Bus	Utility bus read ($\overline{RD}$).
		I	Reset	MMODE - Selects what type of management mode interface to use. "0" selects Utility Bus style, "1" selects UTOPIA 2 style.
MGMT[3]	75	O	UTOPIA 2	Management interface Write or Read/Write ($\overline{WR/RW}$).
			Utility Bus	Utility bus Write ($\overline{WR}$).
		I	Reset	MGMT[3] - Selects clock direction for DRxCLK. "0" DRxCLK is an output, "1" DRxCLK is an input.
MGMT[4]	69	I	UTOPIA 2	Management interface Ready or Data Acknowledge ($\overline{RDY/DTACK}$).
			Utility Bus	No functionality.

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Pin Definitions (con't.)

Pin Name	Pin Number	Input/ Output	Mode	Description
MGMT[5]	78	O	UTOPIA II	No functionality.
			Utility Bus	Utility Bus Address Latch Enable (ALE).
$\overline{\text{PHYRST}}$	74	O	Normal	PHY Reset. Resets the PHY device attached to the 77V011.
$\overline{\text{PHYINT}}$	71	I	Normal	PHY Interrupt. Phy layer interrupt with open drain active low output.
$\overline{\text{SYSRST}}$	46	I	Normal	System Reset. Resets the 77V011 and the PHY device(s) attached to it.
SYSCLK	45	I	Normal	System Clock.
CTRL_A	52	O	Normal	Control A for system engineering usage. This signal is Low after reset.
CTRL_B	53	O	Normal	Control B for system engineering usage. This signal is Low after reset.
Vcc	1,10,18,30,37, 43,54,68,73, 80,90,100,109, 114,124,136	Power	Normal	3.3V Power supply pins.
GND	9,17,28,36, 44,51,62,72, 79,89,99,108, 113,123,127, 135,144	Ground	Normal	Ground pins.

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Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	3.3V Digital Supply Voltage	GND-0.3	3.6	V
V_{IN}	Digital Input Voltage	GND-0.3	5.50	V
V_{OUT}	Digital Output Voltage	GND-0.3	V_{CC}	V
GND	Digital Ground Voltage	0	0	V
I_{OUT}	Output Current	----	12.0	mA
T_{STG}	Storage Temperature	-55	140	C°

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Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	3.3V Digital Supply Voltage	3.0	3.6	V
V_{IN}	TTL Input Voltage	GND	5.50	V
T_A	Operating Temperature	-40	+85	C°
titr	Input TTL rise time	----	2	ns
titf	Input TTL fall time	----	2	ns
V_{IH}	TTL Input High Voltage	2.0	----	V
V_{IL}	TTL Input Low Voltage	----	0.8	V

5348tbl07

DC Electrical Characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 3.3V, V_{IN} = 0V to V_{CC}	10	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{CC}	10	10	µA
V_{OH}	TTL Output High Voltage	I_{OH} = -4mA	2.4	—	V
V_{OL}	TTL Output Low Voltage	I_{OL} = +4mA	—	0.4	V
Icc	Power Supply Current	155.52 Mbps	—	110	mA

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Capacitance

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	All Inputs	—	4	—	pF
C_{OUT}	Output Capacitance	All Outputs	—	6	—	pF
C_{BID}	Bi-Directional Capacitance	All Bi-directional Pins	—	10	—	pF

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Device Interface

The 77V011 uses a UTOPIA level 2 interface to receive and transmit ATM cells to and from the PHY device. It is a master UTOPIA interface and can operate with either an 8-bit or 16-bit data bus. Cell level handshake is used to transfer cells over the UTOPIA interface, byte level handshake is not supported.

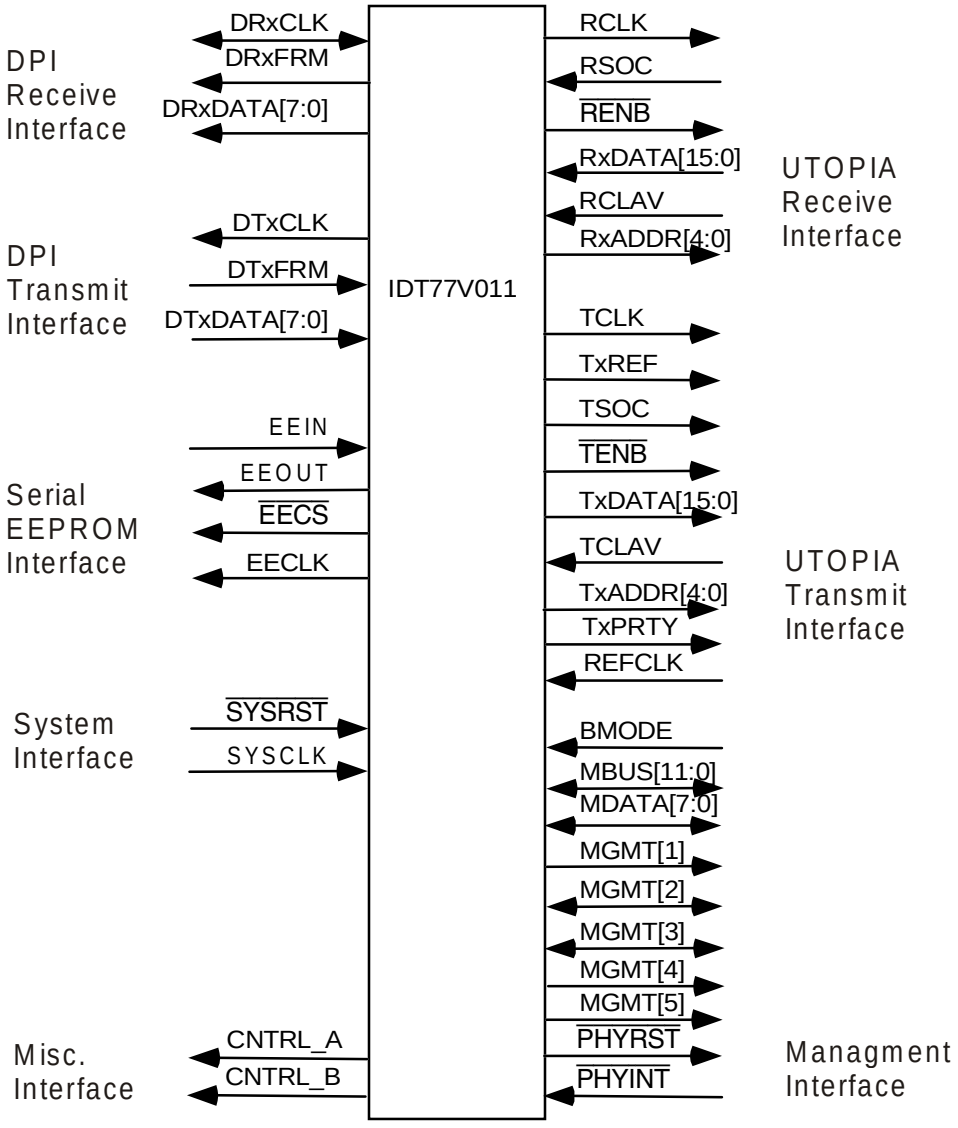
The Data Path Interface (DPI) can be used with a 4-bit or 8-bit data bus. The DPI receive interface can be programmed to operate with the clock as an input or output to accomodate either the IDT SWITCHStAR or a normal mode DPI device.

The EEPROM holds information for initialization and Discovery/ Identify cells. The EEPROM is an optional device and does not need to be implemented.

The Management interface contains the control pins used to access the internal PHY registers during normal operation, and to program the pin configurable registers at reset.

The Misc. Interface contains two output test pins that can be controlled through the registers.

Figure 2: 77V011 Interfaces



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Clock Relationships

All clocks within the 77V011 are derived from the System Clock (SYSCLK). The frequency at which each output clock operates is dependent on the SYSCLK frequency and on the width of the DPI and UTOPIA 2 interfaces. See Clock Relationship Table for the relationship between SYSCLK and the output clocks.

When DRxCLK is configured as an input it is totally asynchronous to SYSCLK. The DRxCLK clock domain within the 77V011 will run at the same frequency as the DRxCLK pin.

Table 1: Clock Relationship and Frequency

Clock Domain	DPI and UTOPIA 2 Bus Widths			
	4-bit DPI 8-bit UTOPIA 2	4-bit DPI 16-bit UTOPIA 2	8-bit DPI 8-bit UTOPIA 2	8-bit DPI 16-bit UTOPIA 2
DRxCLK DTxCLK	SYSCLK	SYSCLK	SYSCLK	SYSCLK
RCLK TCLK	SYSCLK/2	SYSCLK/4	SYSCLK	SYSCLK/2

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UTOPIA 2 Receive Interface Operation

The 77V011 offers a fully compliant UTOPIA Level 2 receive interface, as specified by the UTOPIA Level 2 specification. The interface is a UTOPIA master and will operate with either an 8-bit or 16-bit Input Data Bus (RxDATA[15:0]). UTOPIA cell level handshake is used to receive ATM cells from the PHY device. The other signals associated with this interface are Receive Start of Cell (RSOC), Receive Enable ($\overline{RENB}$), Receive Cell Available (RCLAV), Receive Clock (RCLK), Receive Address Bus (RxADDR[4:0]) and Receive LED (RxLED).

The RxADDR[4:0] bus is fully UTOPIA Level 2 compliant and operates according to the MPHY Cell-Level Handshake with one RCLAV, as described in the UTOPIA Level 2 specification.

RCLK is a continuous clock, whose relationship to SYSCLK is defined in the Clock Relationship and Frequency Table.

RxLED indicates if there is activity on the RxDATA[15:0] bus. This signal asserts high when a cell is transfered over the bus and will stay high for 2^{22} RCLK cycles. AT 40MHz this is approximately 0.1seconds.

UTOPIA transmit and receive bus size is selected at reset with the MBUS[11] signal. Setting MBUS[11] to a zero will select a 8-bit bus, while setting MBUS[11] to a one will select a 16-bit bus. The value of MBUS[11], at reset, is stored in the UTOPIA 2 Size bit of the Mode Select register. See the UTOPIA 2 Receive Register Table for register description.

Polling on the UTOPIA 2 receive bus is done in a round robin fashion. The Max Subports field of the Configuration 2 register determines the upper boundary of the polled addresses. The default value of the Max Subports field is 0x1E, which is also the maximum valid PHY address. The user should not program a value of 0x1F, as this is defined as a Null PHY port by the UTOPIA 2 specification.

When there is no cell transfer in progress, no PHY port is selected, the polling sequence is to output the Null PHY subport address (0x1F) on one RCLK cycle and then output a valid PHY subport address on the next RCLK cycle. This sequence is repeated starting at PHY port address 0x00 and ending at the value specified in Max Subports field. The 77v011 will wrap back to address 0x00 once it has polled the Max Subports address. A PHY device is selected when a PHY responds to its subport address by asserting RCLAV high. $\overline{RENB}$ will assert on the same RCLK cycle that RCLAV is asserted, assuming there is no valid cell transfer in progress. The 77V011 will resume polling starting with the next sequencial subport address once the cell transfer to a selected PHY port begins.

When a PHY port responds with a high RCLAV during a cell transfer the 77V011 will continue to place the responding PHY subport address on the RxADDR[4:0] bus until the current cell transfer has ended and the responding PHY is given controll of the bus. For example, if PHY 0x03 responds by asserting RCLAV while PHY 0x08 is still transfering a cell, then the 77V011 will continue to place PHY subport address 0x03 on the RxADDR[4:0] bus. This will continue untill PHY 0x08 has finished its cell transfer and PHY 0x03 is given control of the receive bus. Polling will then resume with PHY subport address 0x04.

A variance in the polling state machine may occur when DRxCLK is an input to the 77V011 and the frequency of DRxCLK is low enough to cause the UTOPIA receive bus to interrupt the cell transfer. The interruption will be indicated by $\overline{RENB}$ de-asserting high during the cell transfer. Data transfer will resume, where it left off, when $\overline{RENB}$ re-asserts low. In order to resume the current cell transfer the same PHY subport address is placed on the RxADDR[4:0] bus one RCLK cycle before $\overline{RENB}$ is re-asserted low. Each time a cell transfer is interrupted the polling sequence is interrupted in this manner, which may happen frequently if DRxCLK is much slower than SYSCLK. For example if PHY port 0x03 is given control of the bus to transfer a cell. Once PHY port 0x03 takes control of the bus the 77V011 begins its polling sequence starting with PHY port 0x04. In the middle of the cell transfer data is halted by $\overline{RENB}$ de-asserting high, due to the DPI interface. At this time data transfer is halted while 77V011 is polling PHY port 0x08. After some period of time the DPI interface starts to transfer the remainder of the cell. The 77V011 puts the PHY subport address 0x03 on the RxADDR[4:0] bus and then asserts $\overline{RENB}$ low on the next RCLK cycle. Data transfer resumes where it had left off and the 77V011 starts polling the PHY ports starting at PHY subport address 0x09.

Whether in 8 or 16-bit UTOPIA mode there is a minimum one clock cycle delay between back to back cells when polling is being done on multiple PHY ports. There is a minimum five clock cycle delay if polling is being done on a single PHY port. A TAG, regardless of size, does not have any adverse effects on the inter cell gap in the receive direction.

Table 2: UTOPIA 2 Receive Register Table

Register Name	Register Address	Bit #	Bit Name	Value Range	Default Value	Description
Mode Select	8006	2	UTOPIA 2 Size	0 - 1	Defined by pin	Selects the size of the UTOPIA 2 transmit and receive data bus. "0" 8-bit UTOPIA 2 transmit and receive data bus, "1" 16-bit UTOPIA 2 transmit and receive data bus.

5348tbl11

UTOPIA 2 Transmit Interface Operation

The 77V011 offers a fully compliant UTOPIA Level 2 transmit interface, as specified by the UTOPIA Level 2 specification. This is a master UTOPIA interface that uses UTOPIA cell level handshake to transmit ATM cells to the PHY device. It will operate with either a 8-bit or 16-bit Output Data Bus (TxDATA[15:0]). Other signals associated with this interface are Transmit Start of Cell (TSOC), Transmit Enable ($\overline{\text{TENB}}$), Transmit Clock (TCLK), Transmit Cell Available (TCLAV), Transmit Reference Clock (TxREF), Reference Clock (REFCLK), Transmit Parity (TxPRTY), Transmit Address Bus (TxADDR[4:0]) and Transmit LED (TxLED).

TCLK is a continuous clock, whose relationship is defined in the Clock Relationship and Frequency Table.

TxREF is a 8KHz reference clock output generated from REFCLK.

REFCLK is a 8KHz reference clock input used to generate the TxREF clock signal.

TxLED indicates if there is activity on the transmit UTOPIA 2 bus. This signal asserts high when a cell is transfered over the bus, and will stay high for 2^{22} TCLK cycles. AT 40MHz this is approximately 0.1 seconds.

TxPRTY is a parity bit for TxDATA[15:0] bus.

The TxADDR[4:0] bus is fully UTOPIA Level 2 compliant and follows the MPHY Cell-Level Handshake with one TCLAV as described in the UTOPIA Level 2 specification.

When a cell is transfered on the transmit DPI interface the subport address is analyzed and extracted by the 77V011. The subport address is then interleaved with the Null PHY subport address (0x1F) and output on the TxADDR[4:0] bus to query the corresponding PHY port. Upon detecting a high TCLAV the 77V011 will assert $\overline{\text{TENB}}$ low, TSOC and the first vaild byte/word of data. The current PHY subport address will be output on the TxADDR[4:0] bus until another cell enters the 77V011 on the transmit DPI interface. When a cell is detected on the transmit DPI interface and a cell transfer is in progress on the transmit UTOPIA 2 interface, the subport is extracted and output on the TxADDR[4:0] bus, interleaved with the Null PHY subport address, to query the new PHY port. Once the current cell transfer on the transmit UTOPIA 2 interface is complete and the new PHY port has responded, the new cell will be transfered on the transmit UTOPIA 2 interface.

With an 8-bit UTOPIA bus there is a minimum one clock cycle delay between back to back cells when switching is being done without a TAG, and there is a maximum four clock cycle delay if a four byte TAG is being used. There is a minimum one clock cycle delay between back to back cells in 16-bit UTOPIA mode, and a maximum four clock cycle delay if a four byte TAG is being used.

There are several registers associated with the UTOPIA 2 Transmit Interface. In-Stream™ programming cells are used to program the registers, which are described in the UTOPIA 2 Transmit Register Table.

Figure 3: Polling Sequence with no Cell Transfer in Progress

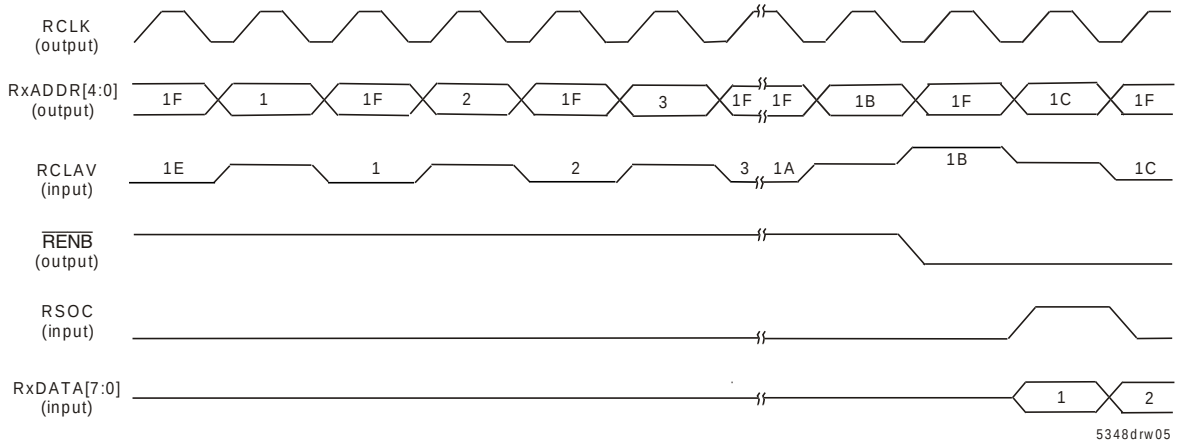


Figure 4: Polling Sequence with Cell Transfer in Progress

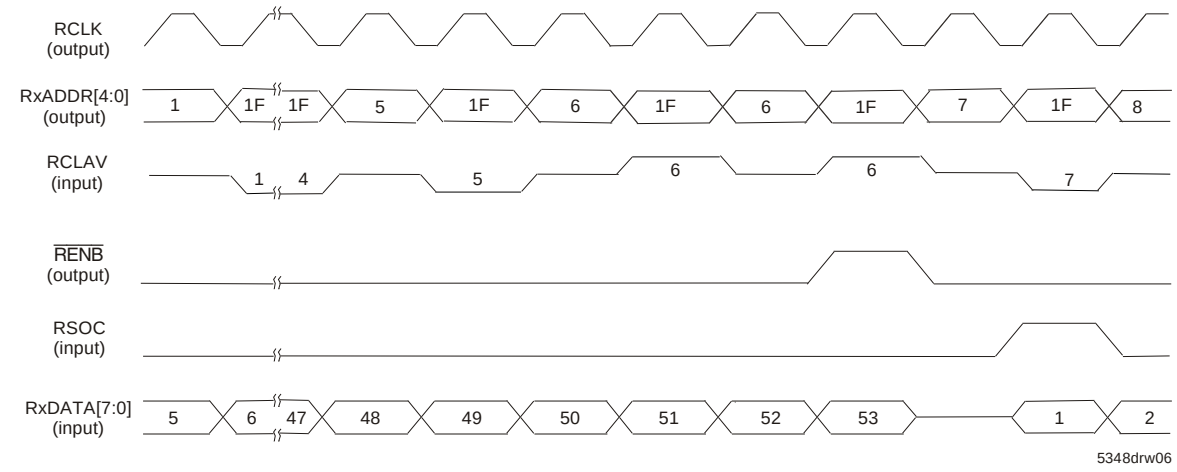


Figure 5: Single Cell Transfer with no Cell Transfer in Progress

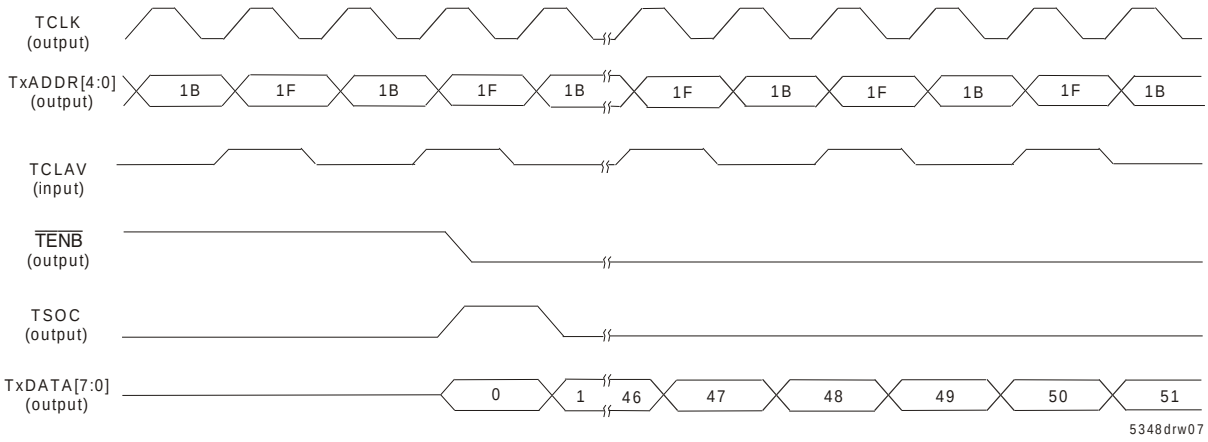


Figure 6: Back-to-Back Cell Transfer on Transmit UTOPIA 2 Bus

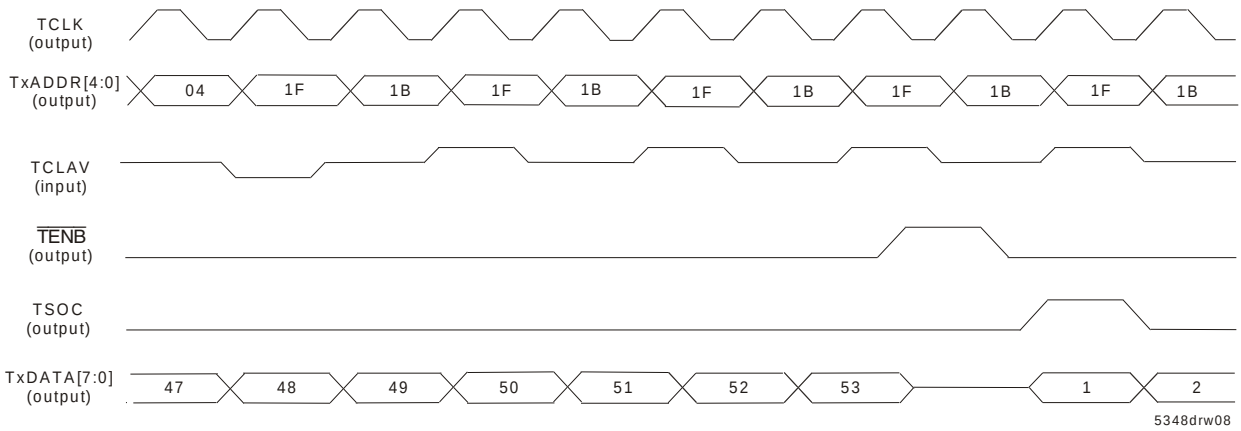


Table 3: UTOPIA 2 Transmit Register Table

Register Name	Register Address	Bit #	Bit Name	Value Range	Default Value	Description
Configuration 1	8001	0	Drop Tx Cell	0 - 1	0	Drop a cell with an invalid subport address. "0" do not drop the cell, "1" drop the cell.
Configuration 2	8002	[1:0]	Stall Tx	0x2	0x0	Selects whether or not to stall the pipeline if the PHY transmit FIFO is full. "0" drop cell, "1" stall pipeline indefinitely, "2" stall pipeline for Stall Cycles.
		[6:2]	Max Subports	0x00 - 0x1E	0x1E	Indicates the maximum subport address value for the PHY(s) connected to the transmit UTOPIA 2 interface.
Configuration 3	8003	[7:0]	Stall Tx Cycles	0x00 - 0xFF	0xFF	Number of TCLK cycles the interface has to stall the pipeline when the PHY transmit FIFO is full. This field is valid only if the Stall Tx for Stall Cycles option is selected.
Status	8009	2	Tx Cell Dropped	0 - 1	0	Indicates if any cells have been dropped at the transmit UTOPIA 2 interface. This is a status indicator for the Stall Tx bit of the Configuration 2 register. "0" no cells have been dropped, "1" a cell was dropped because the PHY did not respond.

5348tbl12

DPI Interface

The Data Path Interface (DPI) is a synchronous bus interface designed to transfer ATM cells between two devices. The 77V011 DPI interface will support either a 4-bit wide data bus (DPI-4) or an 8-bit wide data bus (DPI-8). There are seperate transmit and receive interfaces, with all signals being sampled on the rising edge of their respective clock.

DPI Receive Interface

The DPI Receive Interface is used to transfer cells from the 77V011 to the IDT SWITCHStAR or other DPI device. It supports either a 4-bit or 8-bit Output Data Bus (DRxDATA[7:0]) and follows the standard DPI timing characteristics as described in the DPI specification. Other signals associated with this interface are DPI Receive Start of Frame (DRxFRM), and DPI Receive Clock (DRxCLK).

DRxCLK operates at a frequency less than or equal to SYSCLK. Depending on the DPI mode selected this clock will be either an input or an output. In Normal Mode DRxCLK is an input to the 77V011, and its frequency must be less than or equal to SYSCLK. In Switch Mode DRxCLK is a continuous clock generated by the 77V011, with its frequency being equal to SYSCLK. There is no flow control in Switch mode, as it is assumed that the IDT SWITCHStAR will be able to accept all incoming cells (non-blocking). Programming the clock direction is done at reset.

The DPI mode is selected with the MGMT[3] signal at reset, with the condition of MGMT[3] being stored in the DPI Mode bit of the Mode Select register. Setting MGMT[3] ="0" selects Switch Mode (output), while setting MGMT[3] ="1" selects Normal Mode (input).

The DPI bus size is selected with the MBUS[10] pin at reset, with the condition of MBUS[10] being stored in the DPI Size bit of the Mode Select register. Setting MBUS[10] ="0" selects a 4-bit data bus, while setting MBUS[10] ="1" selects an 8-bit data bus.

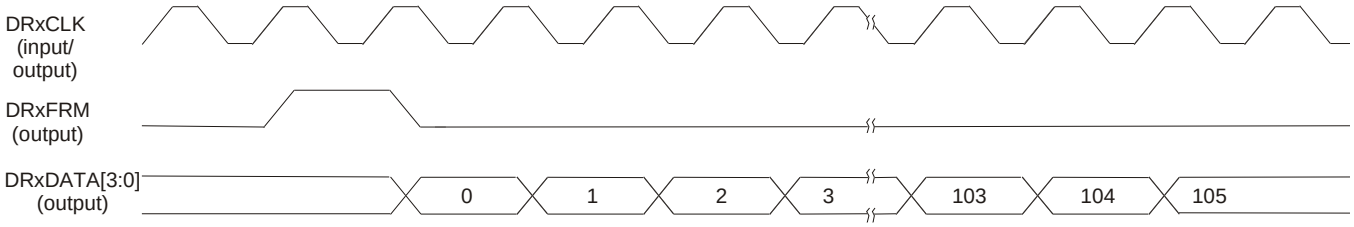
DRxFRM is the start of frame marker. This signal is one DRxCLK cycle long and is asserted high one DRxCLK cycle before the first nibble/byte of valid data.

Table 4: Receive DPI Register Table

Register Name	Register Address	Bit #	Bit Name	Value Range	Default Value	Description
Mode Select	8006	0	DPI Size	0 - 1	Defined by pin	Selects the size of DPI data bus. "0" 4-bit DPI transmit and receive data bus, "1" 8-bit DPI transmit and receive data bus.
		1	DPI Mode	0 - 1	Defined by pin	Selects DRxCLK direction. "0" switch mode (output), "1" normal mode (input).

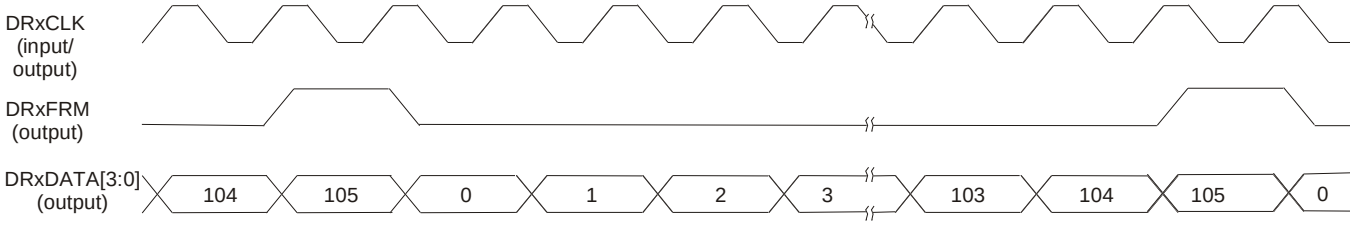
5348tbl13

Figure 7: Nibble Mode One Cell Transfer on Receive DPI Bus



5348drw09

Figure 8: Nibble Mode Back-to-Back Cell Transfer on Receive DPI Bus



5348drw10

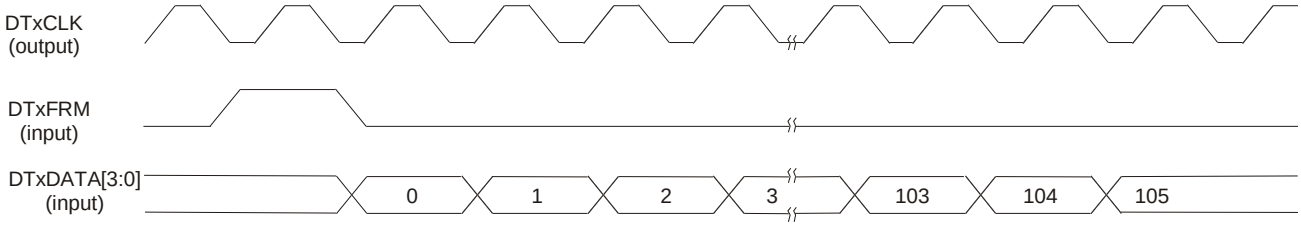
DPI Transmit Interface

The DPI Transmit Interface is used to transfer cells from the IDT SWITCHStAR or other DPI device to the 77V011. It supports either a 4-bit or 8-bit Input Data Bus (DTxDATA[7:0]) and follows the standard DPI timing characteristics as described in the DPI specification. Other signals associated with this interface are DPI Transmit Start of Frame (DTxFRM) and DPI Transmit Clock (DTxCLK).

DTxCLK operates at a frequency equal to SYSCLK. DTxCLK can be stopped to control data flow to the PHY device.

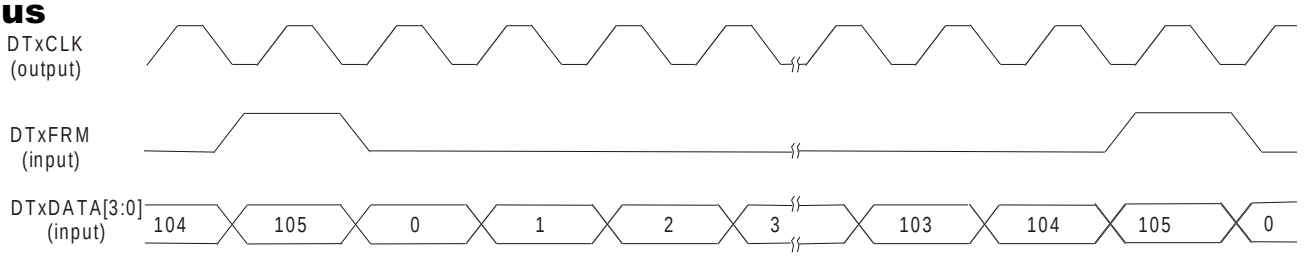
DTxFRM is the start of frame marker. This signal is one DTxCLK cycle long and is asserted high one DTxCLK cycle before the first valid nibble/byte of data.

Figure 9: Nibble Mode One Cell Transfer on Transmit DPI Bus



5348drw11

Figure 10: Nibble Mode Back-to-Back Cell Transfer on Transmit DPI Bus



5348drw12

UTOPIA to DPI Conversion

Byte swapping must be performed to convert the 8 or 16-bit transmit and receive of the UTOPIA interface to the 4 or 8-bit transmit and receive of the DPI interface.

In 4-bit DPI mode cell formatting is big endian, or upper nibble first, while in 8-bit DPI mode cell formatting is done little endian to match the IDT 77V400 Switching Memory. The UTOPIA to DPI Conversion Table illustrates how the 77V011 performs cell formatting in 4 and 8-bit DPI mode.

Figure 11: UTOPIA to DPI Conversion

8-bit UTOPIA

bit 7	bit 0
GFC	VPI[7:4]
VPI[3:0]	VCI[15:12]
VCI[11:4]	

4-bit DPI

bit 3	bit 0
GFC	
VPI[7:4]	
VPI[3:0]	

5348tbl14

8-bit UTOPIA

bit 7	bit 0
GFC	VPI[7:4]
VPI[3:0]	VCI[15:12]
VCI[11:4]	

8-bit DPI

bit 7	bit 0
VPI[7:4]	GFC
VCI[15:12]	VPI[3:0]
VCI[7:4]	VCI[11:8]

5348tbl15

Programming Pin Configurable Registers at Reset

Pull-up or pull-down resistors must be connected to MBUS[11:0], MGMT[3:2] and TxADDR[3:0] signals, on the PCB, to select desired register values. The $\overline{SYSRST}$ signal must be asserted for at least one SYSCLK cycle to load the desired values. On the rising edge of $\overline{SYSRST}$ the 77V011 will begin loading the register values, which takes an additional 16 SYSCLK cycles. During this 16 clock cycle period all outputs will be tri-stated.

Table 5: Reset Configuration Pins

Pin Name	Function @ Reset	Options	Register
MBUS[2:0]	Tx TAG Size	Number of bytes to remove from the cell. Valid values are from zero to four bytes.	Tx TAG [2:0]
MBUS[3]	Tx TAG Location	Location of the transmit TAG. "0" transmit TAG located at the beginning of the cell, "1" transmit TAG located at the end of the cell.	Tx TAG [4]
MBUS[4]	Tx Add HEC	Add a HEC placeholder to the cell. "0" do not add HEC placeholder, "1" add HEC placeholder.	Tx TAG [3]
MBUS[7:5]	Rx TAG Size	Number of bytes to add to the cell. Valid values are from zero to four bytes.	Rx TAG [2:0]
MBUS[8]	Rx TAG Location	Location of the receive TAG. "0" receive TAG located at the beginning of the cell, "1" receive TAG located at the end of the cell.	Rx TAG [4]
MBUS[9]	Rx HEC	Remove HEC byte from cell. "0" do not remove HEC byte, "1" remove HEC byte.	Rx TAG [3]
MBUS[10]	DPI Size	DPI bus size. "0" 4-bit transmit and receive data bus, "1" 8-bit transmit and receive data bus.	Mode Select [0]
MBUS[11]	UTOPIA 2 Size	UTOPIA 2 bus size. "0" 8-bit transmit and receive data bus, "1" 16-bit transmit and receive data bus.	Mode Select [2]
MGMT[2]	MMODE	Managemant mode. "0" Utility Bus style, "1" UTOPIA 2 style.	Mode Select [3]
MGMT[3]	DPI Mode	DRxCLK direction. "0" switch mode (output), "1" normal mode (input).	Mode Select [1]
TxADDR [2:0]	Subport Byte Location	Transmit and receive subport address location. Indicates what byte of the header the transmit and receive subport addresses are located in. Valid values are zero to three.	Tx Subport Position [2:0] and Rx Subport Position [2:0]
TxADDR [3]	Init from EEPROM	Five byte write from EEPROM to In-Stream™ Cell Header and In-Stream™ Subport registers at reset. "0" do not write five byte value, "1" write five byte value.	Mode Select [4]

5348tbl17

Programming Pin Configurable Registers after Reset

The 77V011 has the option to change the Read only pin configurable registers to Read/Write registers. Writing a one to the Override Pin Configuration bit of the Pin Controls register will change the pin configurable registers from Read only to Read/Write. This allows the 77V011 configuration parameters to be changed during normal operation. See Pin Configuration Table for register description.

Table 6: Pin Configuration Table

Register Name	Register Address	Bit #	Bit Name	Range Values	Default Values	Description
Pin Controls	801A	0	Override Pin Configuration	0 - 1	0	Enables writing to pin configurable registers during normal operation. "0" pin configurable registers are read only, "1" pin configurable registers are read/write registers.

5348tbl16

Reset Options

The System Reset ($\overline{SYSRST}$) pin or an In-Stream™ cell carrying the Reset command (Message Type ID 0x3) will reset the 77V011 and the PHY devices. The $\overline{SYSRST}$ pin must be asserted low for a minimum of 100ns, while the In-Stream™ (internal) reset command will keep the 77V011 in reset for 35 SYSCLK cycles.

The 77V011 will remain in reset for 16 SYSCLK cycles after the deassertion of $\overline{SYSRST}$, or the internal reset in the case of a Reset command. All outputs will be tri-stated starting two SYSCLK cycles after the assertion of $\overline{SYSRST}$ or the internal reset, and will stay tri-stated for 24 SYSCLK cycles after the deassertion of $\overline{SYSRST}$ or internal reset. The $\overline{PHYRST}$ pin will then assert low resetting the PHY devices for eight additional SYSCLK cycles. After the eight clock cycle period $\overline{PHYRST}$ pin will deassert high. Eight clock cycles may not be long enough to properly reset some PHY devices. In this case a pull down resistor should be connected to the $\overline{PHYRST}$ pin. This will allow the $\overline{PHYRST}$ pin to be asserted as soon as it is tri-stated, which will lenghten the time that the $\overline{PHYRST}$ pin is a logical zero.

The PHY can be reset at any time by writing a one to the PHY Reset bit of the Reset register. Writing a one will force the external $\overline{PHYRST}$ pin low for 16 SYSCLK cycles. This register bit will return to zero once the reset command is completed. This method will only reset the PHY device connected to the $\overline{PHYRST}$ pin.

Table 7: Reset Table

	Device to be Reset	
	77V011	PHY Device
Software Reset (In-Stream™)	x	x
$\overline{SYSRST}$ (external pin)	x	x
$\overline{PHYRST}$ (register bit)		x

5348tbl18

Bandwidth and Clock Speeds

The 77V011 can run at a maximum SYSCLK speed of 50MHz. The DPI clocks must run at 40MHz, or greater, to achive 155.52Mbps data rate with overhead. The Clock Speed vs Bandwidth Table lists some of the possible data rates and the clock frequencies required to achieve them.

Table 8: Clock Speed verses Bandwidth Table

SYSCLK (MHz)	DPI Bus Width	DTxCLK & DRxCLK (MHz)	UTOPIA Bus Width	TCLK & RCLK (MHz)	Calculated Bandwidth of UTOPIA Interface (cell rate in Mbps)	
					53 byte cell (normal cell, no TAG added)	56 byte cell (four bytes of TAG added w/o HEC)
32	4	32	8	16	125.6	113.1
40	4	40	8	20	157	141.6
50	4	50	8	25	196.3	176.7
16	8	16	8	16	125.6	113.1
25	8	25	8	25	196.3	176.7
33	8	33	8	33	259.1	233.2
32	8	32	16	16	246.9	230.4
50	8	50	16	25	385.7	360

5348tbl19

Management Interface

The Management interface is a multi-function interface used to read and write to the PHY registers during normal operation, and to configure the pin configurable registers during reset.

Signals associated with the Management Interface are Bus Mode (BMODE), Management Bus (MBUS[11:0]), Management Data Bus (MDATA[7:0]), Management 1 (MGMT[1]), Management 2 (MGMT[2]), Management 3 (MGMT[3]), Management 4 (MGMT[4]), Management 5 (MGMT[5]), PHY Reset ($\overline{\text{PHYRST}}$) and PHY Interrupt ($\overline{\text{PHYINT}}$).

During normal operation the Management Interface is used to access the PHY registers. The 77V011 will operate in either a Utility Bus mode or the Management Mode described in the UTOPIA 2 mode section A2.4.2 of the UTOPIA Level 2 specification.

Refer to the Address Map for addressing description of the PHY registers.

Utility Bus Mode

The Utility Bus is used to access and configure the PHY registers. Read and write commands are sent to the PHY with In-Stream™ programming cells.

MBUS[11:0] are active low Chip Select Enable ($\overline{\text{CS}}$[12:1]) signals used to select a particular PHY device. These are active low signals used to validate read, write, or addressing operations on the Utility Bus.

MDATA[7:0] is a multiplexed byte wide address and data bus (AD[7:0]) used to address, read and write data on the Utility Bus.

MGMT[1] is an active low Chip Select Enable ($\overline{\text{CS}}$[0]) signal used to validate read, write, or addressing operations on the Utility Bus.

MGMT[2] is an active low Read Enable ($\overline{\text{RD}}$) used as an enable to read data from an addressed location on MDATA[7:0].

MGMT[3] is an active low Write Enable ($\overline{\text{WR}}$) used as an enable to write data to an addressed location on MDATA[7:0].

MGMT[5] is an active high Address Latch Enable (ALE) used to latch the address in the address phase of a Utility Bus read or write command.

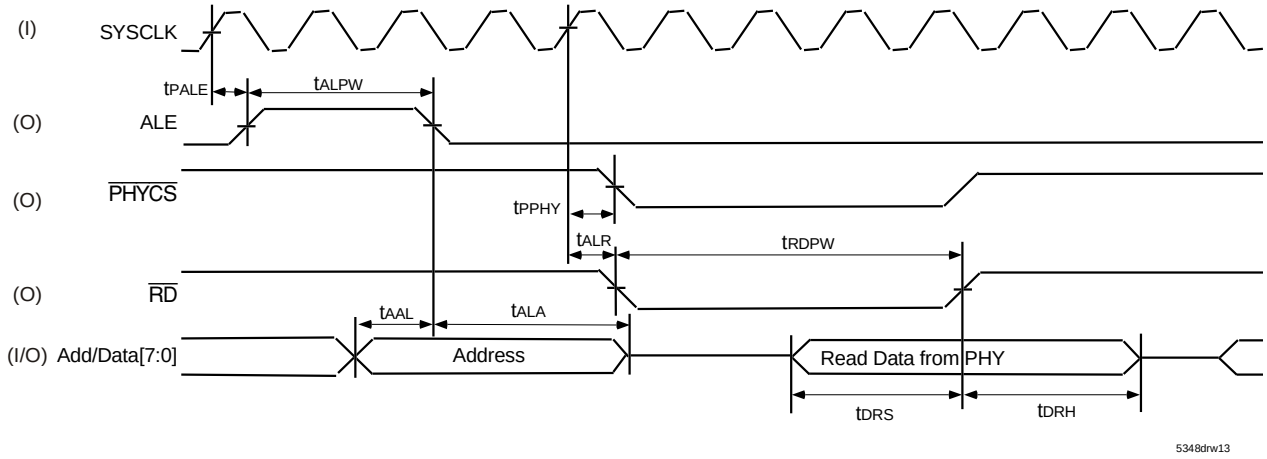
$\overline{\text{PHYRST}}$ is an active low PHY reset signal. $\overline{\text{PHYRST}}$ can be asserted by writing to the PHY Reset bit in the PHY Reset register.

$\overline{\text{PHYINT}}$ is an active low interrupt signal. This signal is driven by the PHY layer and indicates that an interrupt has occurred. The interrupt must be cleared by the controlling CPU before another interrupt event can be reported. Registers associated with the management interface are described in the Management Register Table.

Utility Bus Read Operation

A Utility bus read is initiated by an In-Stream™ programming cell. Once the 77V011 interperts the cell as a read command it will drive $\overline{\text{PHYCS}}$, ALE, $\overline{\text{RD}}$, and AD[7:0]. The PHY samples the address on the falling edge of ALE. Once $\overline{\text{PHYCS}}$ and $\overline{\text{RD}}$ assert the bus tristates and switches to an input for the PHY to place data on. The PHY drives the bus until the rising edge of $\overline{\text{PHYCS}}$ or $\overline{\text{RD}}$. One Utility Bus read can include up to 32 bytes of data.

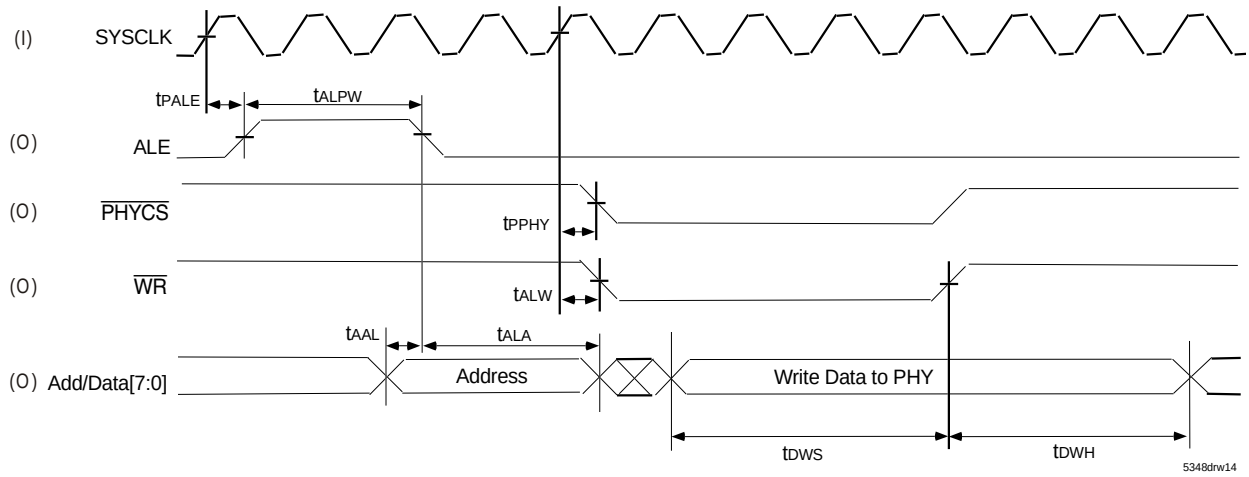
Figure 12: Utility Bus Read Operation



Utility Bus Write Operation

A Utility bus write is initiated by an In-Stream™ programming cell. Once the 77V011 interperts the cell as a write command it will drive $\overline{\text{PHYCS}}$, ALE, $\overline{\text{WR}}$, and AD[7:0]. The PHY samples the address on the falling edge of ALE. Once $\overline{\text{PHYCS}}$ and $\overline{\text{WR}}$ assert the 77V011 will write data to the PHY. One Utility Bus write can include up to 32 bytes of data.

Figure 13: Utility Bus Write Operation



UTOPIA 2 Management Mode

The UTOPIA 2 Management interface is used to access and configure the PHY registers. Read and write commands are sent to the PHY with In-Stream™ programming cells.

BMODE selects the type of UTOPIA 2 Management Mode interface to be used as defined by the UTOPIA Level 2 specification. Setting BMODE ="0" selects the Motorola style, while setting BMODE ="1" selects the Intel mode.

MBUS[11:0] are address bits in this mode and are used to access the internal registers of a particular PHY device. The addressing scheme of what PHY and register address is user definable. An example would be to use the upper five bits (MBUS[11:7]) for the subport number and the lower seven bits (MBUS[6:0]) for the PHY register address.

MDATA[7:0] is a byte wide bi-directional data bus used to read data from or write data to a PHY device.

MGMT[2] is an active low signal used as an enable to read data from the addressed location on the data bus when BMODE = "1", and when BMODE = "0" it is an active low enable used to read data from the PHY layer, or strobe write data to the PHY.

MGMT[3] is an active low write enable used to write data to an addressed location when BMODE = "1", and when BMODE = "0" it defines the current transaction as a read, if equal to one, or a write, if equal to zero.

MGMT[4] is an active low signal that indicates when a transfer on the MDATA[7:0] bus is complete.

$\overline{\text{PHYRST}}$ is an active low PHY reset signal. $\overline{\text{PHYRST}}$ can aslo be asserted by writing to the PHY Reset bit in the PHY Reset register.

$\overline{\text{PHYINT}}$ is an active low interrupt signal. This signal is driven by the PHY layer and indicates that an interrupt has occurred. The interrupt must be cleared by the controlling CPU before another interrupt event can be reported.

Registers associated with the management interface are described in the Management Register Table.

Table 9: Management Register Table

Register Name	Register Address	Bit #	Bit Name	Range Values	Default Values	Description
Mode Select	8006	3	UTOPIA Management Mode	0 - 1	Defined by pin	Selects type of management interface to use. "0" Utility bus style, "1" UTOPIA 2 management style.
PHY Reset	8007	0	PHY Reset	0 - 1	0	PHY Reset. "0" do not reset the PHY device, "1" reset the PHY device ($\overline{\text{PHYRST}}$ signal will be asserted low for at least 16 SYSCLK cycles).

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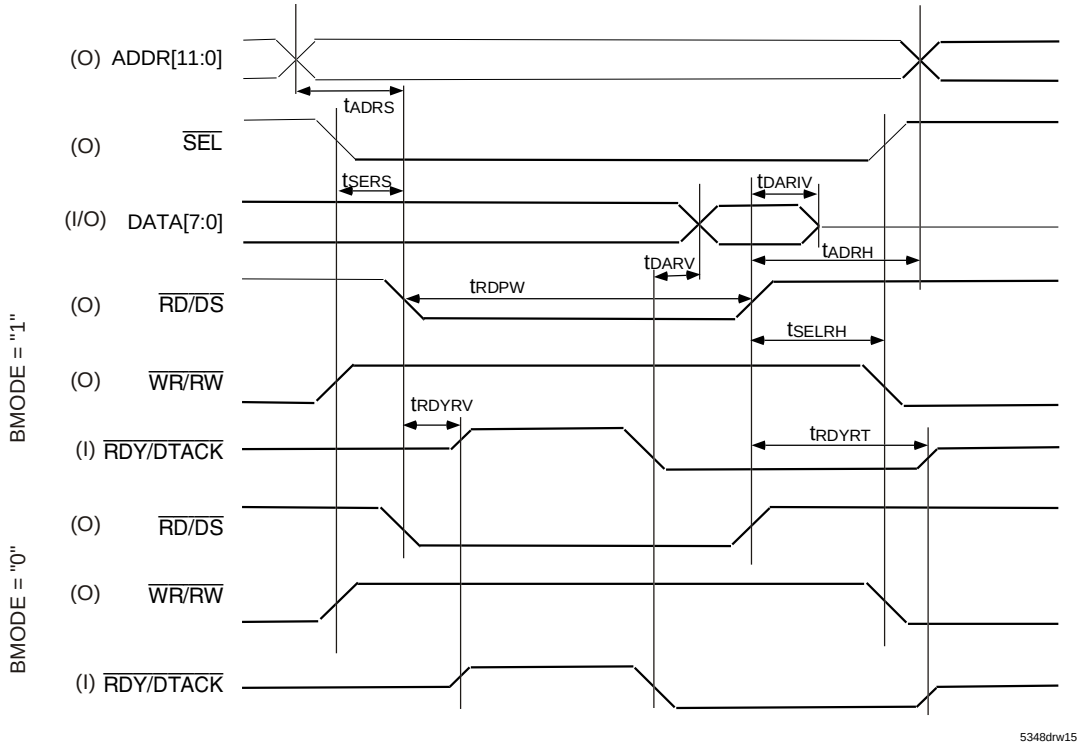
UTOPIA 2 Management Mode Read Operation

A read is initiated by the 77V011 driving the Address bus (MBUS[0:11]), asserting $\overline{\text{SEL}}$ (MGMT1) = "0" and asserting the appropriate strobe, which is dependant on the condition of BMODE. The PHY then drives $\overline{\text{RDY/DTACK}}$ (MGMT[4]) and the Data bus (MDATA[0:7]). The PHY will de-assert $\overline{\text{RDY/DTACK}}$ to signal the completion of the data cycle.

When BMODE = "1" the data is strobed by asserting $\overline{\text{RD/DS}}$, (MGMT[2]) = "0" , with the $\overline{\text{WR/RW}}$, (MGMT[3]) = "1". When BMODE = "0" the data is strobed by setting the $\overline{\text{WR/RW}}$ and $\overline{\text{RD/DS}}$ = "1".

Figure 14: UTOPIA 2 Parallel Interface Read Cycle



UTOPIA 2 Management Mode Write Operation

A write is initiated by the 77V011 driving Address bus (MBUS[0:11]), the Data (MDATA[0:7]), and asserting the appropriate strobe. The PHY will drive $\overline{\text{RDY/DTACK}}$ (MGMT[4]) to specify the beginning and end of the cycle.

When BMODE = "1" the data is strobed setting $\overline{\text{WR/RW}}$ (MGMT[3]) and $\overline{\text{RD/DS}}$ (MGMT[2]) = "1". When BMODE = "0" the data is strobed by setting $\overline{\text{RD/DS}}$ = "1" and setting $\overline{\text{WR/RW}}$ = "0".

Figure 15: UTOPIA 2 Parallel Interface Write Cycle

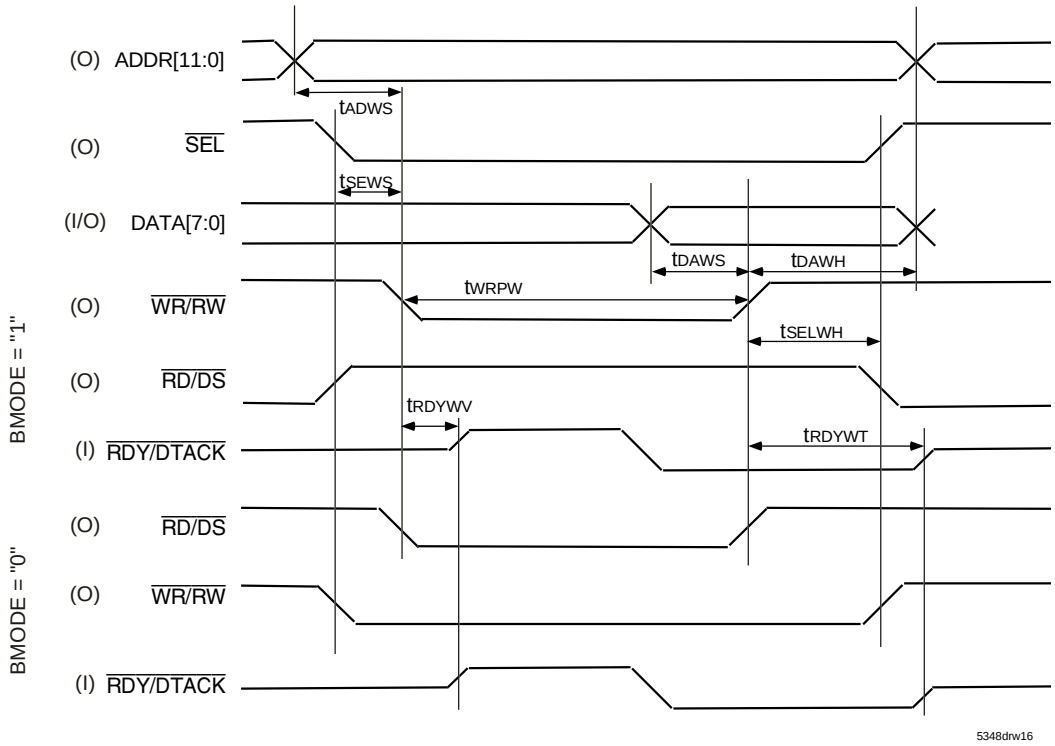


Table 10: Multiplexed Management Interface

Device Pin Name	Reset	Utility Bus Interface	UTOPIA 2 (Parallel) Interface
BMODE	---	---	BMODE
MBUS[0]	Tx TAG Size[0]	$\overline{CS}$[1]	ADDR[0]
MBUS[1]	Tx TAG Size[1]	$\overline{CS}$[2]	ADDR[1]
MBUS[2]	Tx TAG Size[2]	$\overline{CS}$[3]	ADDR[2]
MBUS[3]	TxLOC	$\overline{CS}$[4]	ADDR[3]
MBUS[4]	TxHEC	$\overline{CS}$[5]	ADDR[4]
MBUS[5]	Rx TAG Size[0]	$\overline{CS}$[6]	ADDR[5]
MBUS[6]	Rx TAG Size [1]	$\overline{CS}$[7]	ADDR[6]
MBUS[7]	Rx TAG Size [2]	$\overline{CS}$[8]	ADDR[7]
MBUS[8]	RxLOC	$\overline{CS}$[9]	ADDR[8]
MBUS[9]	RxHEC	$\overline{CS}$[10]	ADDR[9]
MBUS[10]	DPI_SEL	$\overline{CS}$[11]	ADDR[10]
MBUS[11]	UTOPIA_SEL	$\overline{CS}$[12]	ADDR[11]
MDATA[7:0]	---	ADD/DATA[7:0]	DATA[7:0]
MGMT[1]	---	$\overline{CS}$[0]	$\overline{SEL}$
MGMT[2]	MMODE	$\overline{RD}$	$\overline{RD/DS}$
MGMT[3]	DPI_MODE	$\overline{WR}$	$\overline{WR/RW}$
MGMT[4]	---	---	$\overline{RDY/DTACK}$
MGMT[5]	---	ALE	---
$\overline{PHYRST}$	---	$\overline{PHYRST}$	$\overline{PHYRST}$
$\overline{PHYINT}$	---	$\overline{PHYINT}$	$\overline{PHYINT}$

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Table 11: Utility Bus Management Interface

Pin Name	Function	Input/ Output	Description
MGMT[1]	$\overline{CS}$[0]	O	Chip Select[0]. Active low PHY chip select.
MBUS[11:0]	$\overline{CS}$[12:1]	O	Chip Select[12:1]. Active low PHY chip select for 12 additional PHYs connected to this device.
MGMT[2]	$\overline{RD}$	O	Read Enable. Active low read enable.
MGMT[3]	$\overline{WR}$	O	Write Enable. Active low write enable.
MGMT[5]	$\overline{ALE}$	O	Address Latch Enable. Active high address latch enable.
MDATA[7:0]	ADDR/DATA[7:0]	I/O	Address/Data bus. Bidirectional address and data bus.
$\overline{PHYINT}$	$\overline{PHYINT}$	I	PHY Interrupt. Active low PHY interrupt.
$\overline{PHYRST}$	$\overline{PHYRST}$	O	PHY Reset. Active low PHY layer reset.

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Table 12: UTOPIA 2 Management Interface

Pin Name	Function	Input/ Output	Description
BMODE	BMODE	I	Bus Mode. "0" selects Motorola management mode interface, "1" selects Intel management mode interface.
MBUS[11:0]	ADDR[11:0]	O	Address bus used to select a register in a particular PHY device.
MDATA[7:0]	DATA[7:0]	I/O	Byte wide bidirectional data bus.
MGMT[1]	$\overline{SEL}$	O	Select. Active low signal used to validate ADDR[11:0] for a read or write operation.
MGMT[2]	$\overline{RD/DS}$	O	Read or Data Strobe. If BMODE = "0" then read data from the PHY layer, or strobe write data to the PHY layer. If BMODE ="1" then read data from the addressed location onto the DATA[7:0] bus.
MGMT[3]	$\overline{WR/RW}$	O	Write or Read/Write. If BMDOE ="0" then access is a read if high and a write if low. If BMODE ="1" then write data from DATA[7:0] to the addressed location.
MGMT[4]	$\overline{RDY/DTACK}$	I	Ready or Data Acknowledge. Tri-stateable signal used to acknowledge the end of a transfer over DATA[7:0] bus.
$\overline{PHYRST}$	$\overline{PHYRST}$	O	PHY Reset. Active low PHY layer reset.
$\overline{PHYINT}$	$\overline{PHYINT}$	I	PHY Interrupt. PHY layer interrupt, with open-drain active low output.

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EEPROM Interface

The EEPROM interface is an optional device that can be used for initialization and Discovery/Identify commands. The data is broken up into five fields.

Bytes [4:0] contain a 5-byte value that can be read at reset and placed in the In-Stream™ Cell Header and In-Stream™ Subport registers. Bytes [3:0] are used for the In-Stream™ Cell Header registers, while byte [4] is used for the In-Stream™ Subport register. Bytes [7:5] are not used at this time, while bytes [39:8] contain 32-bytes of data, which is read when a Discovery/Identifycommand is encountered. Bytes [40:127] are reserved and bytes [128:255] are user defined. The registers associated with the EEPROM are listed in the EEPROM Register Table.

Signals associated with this interface are Clock (EECLK), Chip Select ($\overline{EECS}$), Data Out (EEDOUT), and Data In (EEDIN).

EECLK is generated from SYSCLK and is an output of the 77V011.

$\overline{EECS}$ is an active low chip select signal used to validate a read or write operation.

EEDOUT is a serial data output pin to the EEPROM.

EEIN is a serial input data pin from the EEPROM.

At reset TxADDR[3] selects whether or not to write the first five bytes stored in the EEPROM to the In-Stream™ Cell Header and In-Stream™ Subport registers. Setting TxADDR[3] to a zero will select not to write the five byte value, while setting it to a one will write the value to the registers. The state of the TxADDR[3] signal, at reset, is stored in the Init from EEPROM bit of the Mode Select register.

The EEPROM can be controlled with the EEPROM registers, which include Mux Select (EEPROM Mux Sel), Clock Out (EEPROM Clock Out), Chip Select (EEPROM Chip Select), Data Out (EEPROM Out), and Data In (EEPROM In).

EEPROM Mux Select indicates whether the EEPROM pins will be connected to the internal logic, or to the EEPROM registers. When connected to the Internal logic 32-bytes of data are read from the EEPROM when a Discovery/Identify command is filtered. Controlling the EEPROM from the registers enables the user the flexibility of reading and writing the EEPROM at any time. Programming is accomplished with In-Stream™ cells regardless of the method used to access the EEPROM.

EEPROM Clock Out is used to clock the EEPROM when it is being controlled by the registers. This register must be written to twice to execute one EEPROM clock cycle. You must write to the clock register to perform a read or write command.

EEPROM Chip Select validates transactions on the EEPROM interface when being controlled by the EEPROM registers.

EEPROM Out is a 1-bit register used to output data to the EEPROM.

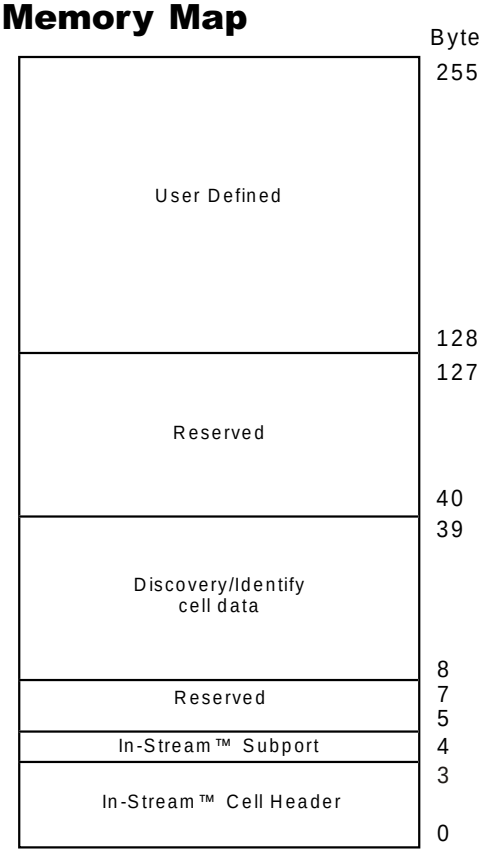
EEPROM In is a 1-bit register used to input data from the EEPROM.

Transmit Cell Routing

A subport address is used to select a PHY port. The address can be up to five bits wide and be located anywhere in the first four bytes of the ATM cell, or first eight bytes of the cell if a four byte pre-pended TAG is being used. It can start in any bit location of a byte and can span over the byte boundary.

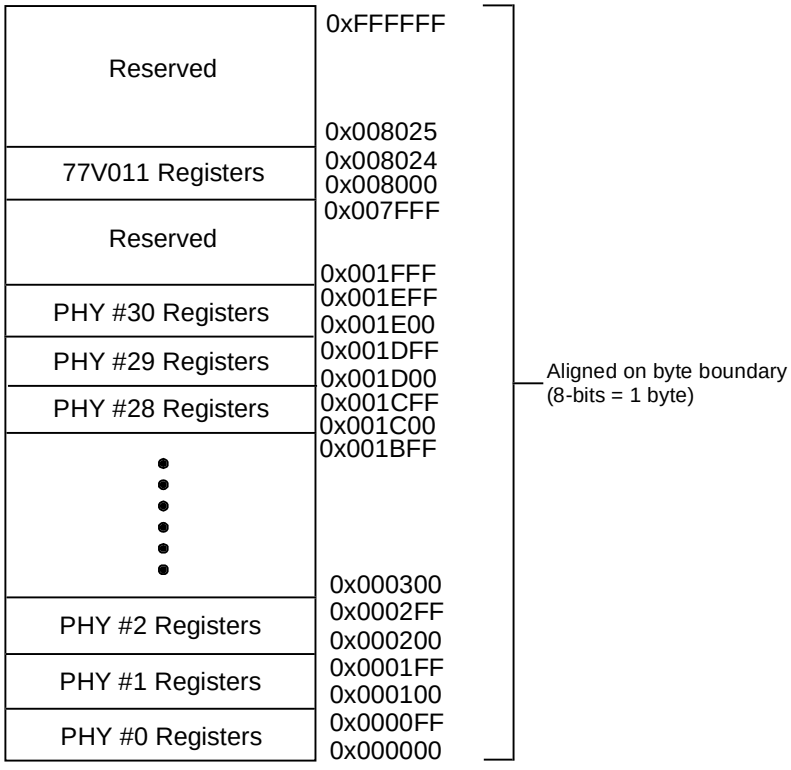
The 77V011 uses the transmit subport field in determining how to route the cell. Normal cells have a PHY subport value from zero to the value stored in Max Subports bits of the Configuration 2 register. The Max Subport can be any value between zero and 30, as the UTOPIA 2 specification allows a total of 31 PHY ports to be

Figure 16: EEPROM Memory Map



5348drw17

Figure 17: Register Address Map



5348drw18

Table 13: EEPROM Register Table

Register Name	Register Address	Bit #	Bit Name	Value Range	Default Value	Description
Mode Select	8006	4	Init from EEPROM	0 - 1	Defined by pin	Five byte write from EEPROM to In-Stream™ Cell Header and In-Stream™ Subport registers at reset. "0" do not write five byte value, "1" write five byte value to registers.
Pin Controls	801A	3	EEPROM Mux Select	0 - 1	0	Indicates if the EEPROM interface will be connected to the internal logic or the EEPROM registers. "0" connected to internal logic, "1" connected to EEPROM registers.
		4	EEPROM Clock Out	0 - 1	0	EEPROM clock when EEPROM interface is connected to the EEPROM registers. "0" clock low, "1" clock high.
		5	EEPROM Chip Select	0 - 1	0	EEPROM chip select when EEPROM interface is connected to the EEPROM registers. "0" EEPROM interface is selected, "1" EEPROM interface is not selected.
		6	EEPROM Out	0 - 1	0	EEPROM serial output when EEPROM interface is connected to the EEPROM registers.
		7	EEPROM In	0 - 1	0	EEPROM serial input when EEPROM interface is connected to the EEPROM registers.

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connected to a UTOPIA 2 interface. The cell will be dropped if a subport greater than the Max Subports value is used.

Once the subport field is read the 77V011 can replace the subport value with the value contained in the New Subport bits of the Modify Tx Subport register. Overwriting is determined by the Replace Subport bit of the Modify Tx Subport register. Only the data cells are affected when the 77V011 is configured to overwrite the subport field. The subport field of In-Stream™ cells are not altered.

The Tx Byte Location bits of the Tx Subport Position register indicate what byte of the header the subport field starts in. Vaild values are zero to three without using a TAG, and zero to seven when using a TAG. The subport field can start in any byte location of the header. This value is programmed at reset with TxADDR[2:0] pins. The 77V011 will concatenate the transmit subport field if any part of the subport field extends into the payload area of the cell. This is to ensure that the payload will not be altered.

Bits [5:3] of the Tx Subport Position register contain the Tx Bit Location. This value indicates what bit in the byte the subport MSB is located in. A value of zero means that bit zero of the selected byte is MSB, bit 7 of the next byte is MSB-1, ect... The subport can start on any bit of a byte and span multiple bytes.

The number of bits to be used for the transmit subport field is programmed in the Tx Subport Width field bits of the Subport Configuration 1 register. The subport width can be any value between one and five, with the default value being five.

A special mode of operation occurs when the Tx Subport Width is set to zero. When this is done, the cell will be passed to the transmit UTOPIA bus unchanged, and the polled address will be 0x0. This mode of operation is intended for system configurations with a single PHY device.

Registers associated with the transmit cell routing are defined in the Transmit Cell Routing Register Table.

Receive Cell Routing

The receive cell routing is done by inserting the originating PHY port address into the receive subport address field. The 77V011 uses the subport field in determining how to route the cell. Normal cells have a PHY subport value from zero to the value stored in Max Subports bits of the Configuration 2 register. The Max Subport can be any value between zero and 30, as the UTOPIA 2 specification allows a total of 31 PHY ports to be connected to a UTOPIA 2 interface.

In-Stream™ cells have a subport value that is defined in the In-Stream™ Subport bits of the Subport Configuration 1 register. In order for In-Stream™ cells to be filtered properly two things must happen. First, the subport value within the received cell must match the In-Stream™ Subport, Tx Subport Width, Tx Byte Location, and the Tx Bit Location register fields. Second, the received cell's header, excluding the PT, CLP and HEC fields, must match the In-Stream™ Cell Header register bits [31:4]. This dual check allows the In-Stream™ subport value to be the same as a valid PHY subport address.

The Rx Byte Location bits of the Rx Subport Position register indicate what byte of the header the subport field starts in. Vaild values are zero to three without using a TAG, and zero to seven when using a TAG. The subport field can start in any byte location of the header. This value is programmed at reset with TxADDR[2:0] pins. The 77V011 will concatenate the receive subport field if any part of the subport field extends into the payload area of the cell. This is to ensure that the payload will not be altered.

Bits [5:3] of the Rx Subport Position register contain the Rx Bit Location. This value indicates what bit in the byte the subport MSB is located in. A value of zero means that bit zero of the selected byte is MSB, bit 7 of the next byte is MSB-1, ect... The subport can start on any bit of a byte and span multiple bytes.

The number of bits to be used for the receive subport field is programmed in the Rx Subport Width field bits of the Subport Configuration 2 register. The subport width can be any value between one and five, with the default value being five.

The Rx Out of Range Address Mask registers validate the VPI/VCI field, default value is 0x000000. This 24-bit value is used to compare against the incoming cell headers on the receive UTOPIA 2 inter-

face. A bit wise AND operation is done between each bit of the incoming cell header and its corresponding bit of the Rx Out of Range Address Mask register. The Address Range Error bit of the Status register will be set to a one if the result of any of these AND operations is a one, indicating an invalid cell has been received. A Notification cell will be generated if the Rx Address Error bit of the Notification Mask register is set to a one. Another Notification cell will be generated 25ms after the error occurred if the Address Range Error bit has not been cleared. Additional Notification cells will be generated on 12ms intervals, thereafter,until the Address Range Error bit is cleared.

The Rx Out of Range Subport bits of the Rx Out of Range Subport register stores the subport address of the violating Rx Out of Range cell. The CPU can read this register to determine what PHY port the invalid cell came from. The Rx Out of Range Subport bits will be overwritten when a new address range error occurrs.

Figure 18: Transmit Subport Interpreter

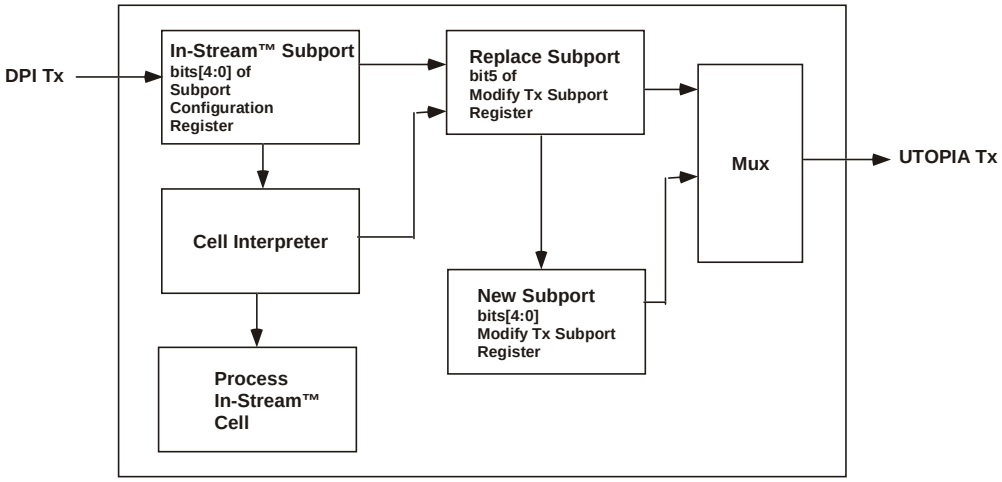

Figure 19: Example Subport Programming

Register Content			
Max Subports	0x1E	In-Stream™ Subport	0x07 (matches bits[5:1] of In-Stream™ Cell Header byte 2
Subport Width	0x5	In-Stream™ Cell Header byte 3	0x00
Replace Subport	1	In-Stream™ Cell Header byte 2	0xE0
Bit Location	0x5	In-Stream™ Cell Header byte 1	0x01
Byte Location	0x2	In-Stream™ Cell Header byte 0	0xF0
New Subport	0x1F		

x = Any valid subport address

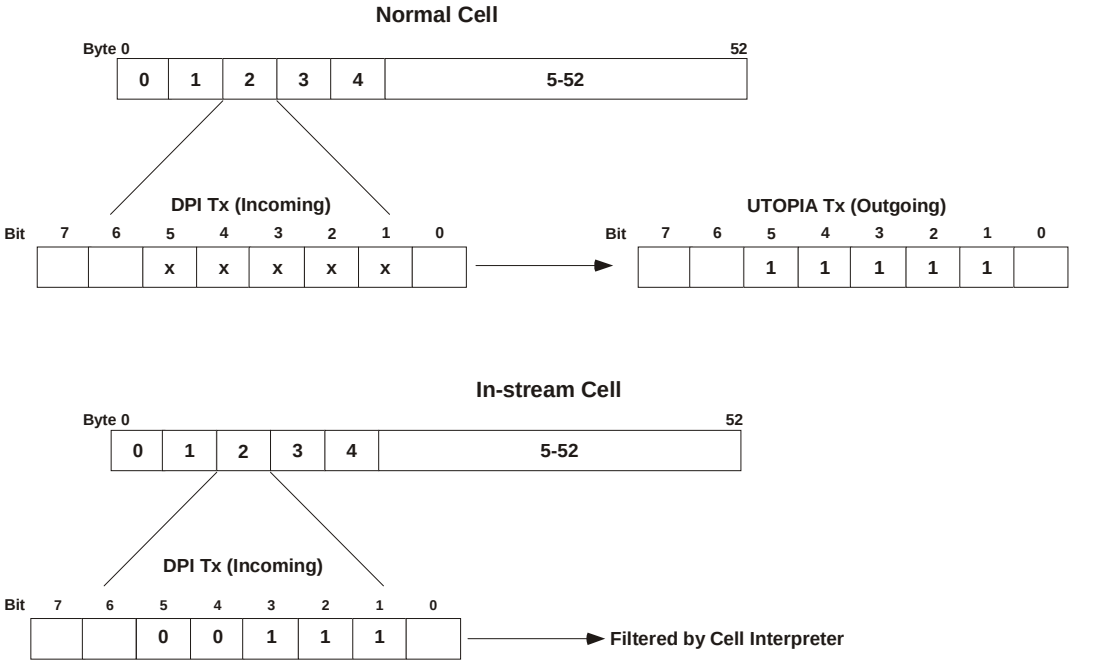

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Table 14: Transmit Cell Routing Register Table

Register Name	Register Address	Bit #	Bit Name	Value Range	Default Value	Description
Configuration 2	8002	[6:2]	Max Subports	0x00 - 0x1E	0x1E	Indicates the maximum subport address for the PHY's connected to the transmit UTOPIA 2 interface.
Subport Configuration 1	8013	[4:0]	In-Stream™ Subport	0x00 - 0x1F	0x00	Subport address used to filter In-Stream™ programming cells.
		[7:5]	Tx Subport Width	0x0 - 0x7	0x5	Programs how many bits will be used for subport addressing in the transmit direction.
Modify Tx Subport	8014	[4:0]	New Subport	0x00 - 0x1F	0x00	New value used to replace subport address in outgoing cells. This value will only be used if the Replace Subport bit of the Modify Tx Subport register is set to a one.
		5	Replace Subport	0x0 - 0x7	0	Indicates whether or not to replace the subport address in outgoing cells. "0" do not replace the subport address, "1" replace the subport address with the value in the New Subport bits of the Modify Tx Subport register.
Tx Subport Position	8015	[2:0]	Tx Byte Location	0x0 - 0x7	Defined by pin	Indicates what byte of the transmit cell header the subport address starts in. The subport address can cross the byte boundary.
		[5:3]	Tx Bit Location	0x0 - 0x7	0x5	Indicates what bit of the byte defined by the Tx Byte Location bits of the Tx Subport Position register the MSB of the transmit subport address starts. The subport address can cross the byte boundary.

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Clearing the interrupt is done by writing a one to the Address Range Error bit of the Status register. Writing a one will clear the interrupt and reset the register bit to a zero.

Registers associated with the receive cell routing are defined in the Receive Cell Routing Register Table.

Tag Interface

A TAG can be added to the cell in either the transmit or receive direction. It can be up to four bytes long, and be added to the beginning or end of the cell.

Programming a TAG for both the transmit and receive direction is done with external pins and internal registers, with each direction being individually programmed. Registers associated with the TAG are listed in the Transmit and Receive TAG Register Table.

Receive Tag

A TAG is added in the receive direction by first configuring the external pins and then programming the internal registers. The external pins are multiplexed with the MBUS[9:5] pins.

The Rx TAG Size [2:0] indicates the size of the TAG to be appended. This value can be from zero to four and is set with the MBUS[7:5] pins at reset. This value is stored in Rx TAG Size bits of the Rx TAG register.

The Rx TAG Location indicates whether the TAG is located at the beginning or end of the cell. Setting this bit to a zero indicates that the TAG is appended to the beginning of the cell,while setting this bit to a one indicates the TAG is appended to the end of the cell. This register bit is programmed at reset with the MBUS[8] pin and is stored in Rx TAG Location bit of the Rx TAG register.

Rx Remove HEC is defined by pin MBUS[9] at reset and indicates whether the HEC byte should be removed or not. Setting this bit to zero will indicate not to remove the HEC byte, while setting it to a one will remove the HEC byte. This value is stored in the Rx Remove HEC bit of the Rx TAG register.

The TAG 1, 2, 3 and 4 registers contain the header value used for the TAG. This value is only used for all cells. The default value is 0x000001FX, which can be changed by writing to the registers with In-Stream™ cells.

Rx Move PT/CLP bit, of the Configuration 1 register, is an option to move the PT and CLP fields of the ATM cell header into the four bytes of TAG area. Setting this bit to zero will not move these fields, while setting it to a one will move these fields from the incoming cell header to the TAG area. This enables a DPI device or SWITCHStAR that is switching on the TAG area to find OAM cells, do low prioity cell discards and EFCI processing. This option is only valid if using all four bytes of TAG and switching is being done on the TAG.

The Copy EFCI bit, of the Configuration 1 register, selects whether or not to OR the EFCI bit of the cell header with the EFCI bit of the TAG area, and place the OR'ed EFCI bit in the cell header. Setting this bit to zero will select not to OR the EFCI bits, while setting it to a one will OR the EFCI bits.

Registers associated with the Receive TAG are listed in the Receive TAG Register Table.

Transmit Tag

A transmit TAG is programmed by first configuring the external pins and then programming the internal registers. The external pins are multiplexed with the MBUS[4:0] bus.

Tx TAG Size [2:0] indicates the size of the TAG to be removed from the cell. This value is set with the MBUS[2:0] pins at reset and is stored in bits [2:0] of the Tx TAG register. Valid values for this field are zero to four.

Tx TAG Location indicates whether the TAG is located at the beginning or end of the cell. Setting this bit to a zero indicates the TAG is located at the beginning of the cell, while setting this bit to a one indicates that the TAG is located at the end of the cell. This value is programmed at reset with the MBUS[3] pin and is stored in the Tx TAG Location bit of the Tx TAG register.

Tx Add HEC indicates if a HEC placeholder should be added to the cell. Setting this bit to a zero indicates not to add the HEC byte, while setting it to a one indicates to add the HEC byte. This value is programmed at reset with the MBUS[4] pin and is stored in Tx ADD HEC bit of the Tx TAG register.

The TAG 1, 2, 3 and 4 registers contain the header value used for the TAG. This value is only used for all cells. The default value is 0x000001FX, which can be changed by writing to the registers with In-Stream™ cells.

The Tx Move PT/CLP bit, of the Configuration 1 register, is an option to move the PT/CLP fields from the 4-byte TAG area to the cell header. Setting this bit to a one will not move the fields, while setting it to a one will move the PT/CLP fields.

Registers associated with the Transmit TAG are listed in the Transmit TAG Register Table.

Table 15: Receive Cell Routing Register Table

Register Name	Register Address	Bit #	Bit Name	Value Range	Default Value	Description
Notification Mask	8008	1	Rx Address Error	1 - 0	0	Mask Address Range Error notification. "0" no Event Notification cell will be generated when a Rx Out of Range Address Error occurrs, "1" generate Event Notification cell when a Rx Out of Range Address Error occurrs.
Status	8009	1	Address Range Error	1 - 0	0	Address Range Error indication when an Address Range Error occurrs. "0" no Address Range Error detected, "1" Address Range Error has been detected.
Timeout Status	800A	1	Address Error Status	1 - 0	0	Indicates that a Address Error occurred more than 25ms ago, and Address Range error status bit has not been cleared. This bit will return to zero once the interrupt is cleared. "0" no Address Range Errors detected, "1" Address Range Error occurred more than 25ms ago and has not been cleared.
Rx Out of Range Subport	800B	[4:0]	Rx Out of Range Subport	0x00 - 0x1F	0x00	The subport address of a cell containing an invalid cell header.
Rx Out of Range Address Mask byte 2	801C	[7:0]	Address Mask Register [23:16]	0xFF	0x00	Value used to validate cells on the receive UTOPIA interface.
Rx Out of Range Address Mask byte 1	800D	[7:0]	Address Mask Register [15:8]	0xFF	0x00	Value used to validate cells on the receive UTOPIA interface.
Rx Out of Range Address Mask byte 0	800E	[7:0]	Address Mask Register [7:0]	0xFF	0x00	Value used to validate cells on the receive UTOPIA interface.
Subport Configuration 2	8023	[2:0]	Rx Subport Width	0x0 - 0x7	0x5	Programs how many bits will be used for subport addressing in the receive direction.
Rx Subport Position		[2:0]	Rx Byte Location	0x0 - 0x7	Defined by pin	Indicates what byte of the receive cell header the subport starts in. The subport address can cross the byte boundary.
		[5:3]	Rx Bit Location	0x0 - 0x7	0x5	Indicates what bit of the byte defined by the Rx Byte Location bits of the Rx Subport Position register the MSB of the receive subport address starts. The subport address can cross the byte boundary.

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Table 16: Receive Tag Register Table

Register Name	Register Address	Bit #	Bit Name	Value Range	Default Value	Description
Configuration 1	8001	1	Copy EFCI	0 - 1	0	Selects whether or not to OR the EFCI bit of the cell header with the EFCI bit of the 4-byte TAG area, and place the OR'ed EFCI bit in the cell header. "0" do not OR the EFCI bit to the 4-byte TAG area, "1" OR the EFCI bit to the 4-byte TAG area.
		2	Rx Move PT/CLP	0 - 1	0	Selects whether or not to move the PT/CLP fields from the cell header into the 4-byte TAG area. "0" do not move the PT/CLP to the 4-byte TAG area, "1" move the PT/CLP to the 4-byte TAG area.
Rx TAG	8005	[2:0]	Rx Tag Size [2:0]	0 - 4	Defined by pin	Number of bytes to add to ATM cell in the receive direction. Valid values are from zero to four.
		3	Rx Remove HEC	0 - 1	Defined by pin	Remove HEC byte from cell. "0" do not remove the HEC byte from the cell, "1" remove the HEC byte from the cell.
		4	Rx TAG Location	0 - 1	Defined by pin	TAG location in receive direction. "0" receive TAG is located at the beginning of the cell, "1" receive TAG is located at the end of the cell.
TAG byte 3	8016	[7:0]	TAG [31:24]	0x00 - 0xFF	0x00	TAG added to cell.
TAG byte 2	8017	[7:0]	TAG [23:16]	0x00 - 0xFF	0x00	TAG added to cell.
TAG byte 1	8018	[7:0]	TAG [17:8]	0x00 - 0xFF	0x01	TAG added to cell.
TAG byte 0	8019	[7:0]	TAG [7:0]	0x00 - 0xFF	0xF0	TAG added to cell.

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Table 17: Transmit Tag Register Table

Register Name	Register Address	Bit #	Bit Name	Value Range	Default Value	Description
Configuration 1	8001	3	Tx Move PT/CLP	0 - 1	0	Selects whether or not to move the PT/CLP fields from the 4-byte TAG area into the cell header. "0" do not move the PT/CLP fields to the cell header, "1" move the PT/CLP fields to the cell header.
Tx TAG	8004	[2:0]	Tx TAG Size	0x0 - 0x4	Defined by pin	Number of bytes to remove from the ATM cell in the transmit direction. Valid values are from zero to four.
		3	Tx Add HEC	0 - 1	Defined by pin	Add a HEC placeholder in the transmit direction. "0" do not add a HEC placeholder, "1" add a HEC placeholder.
		4	Tx TAG Location	0 - 1	Defined by pin	TAG location in transmit direction. "0" transmit TAG is located at the beginning of the cell, "1" transmit TAG is located at the end of the cell.
TAG byte 3	8016	[7:0]	TAG [31:24]	0x00 - 0xFF	0x00	TAG added to cell.
TAG byte 2	8017	[7:0]	TAG [23:16]	0x00 - 0xFF	0x00	TAG added to cell.
TAG byte 1	8018	[7:0]	TAG [17:8]	0x00 - 0xFF	0x01	TAG added to cell.
TAG byte 0	8019	[7:0]	TAG [7:0]	0x00 - 0xFF	0xF0	TAG added to cell.

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In-Stream™ Programming

In-Stream™ programming cells are used to carry commands to the 77V011 and for the CPU to receive information from the 77V011. Cells are received on the DTxDATA[7:0] bus. All cells received on the DTxDATA[7:0] data bus are filtered by the cell interpreter to determine if they are In-Stream™ programming cells. In order to be reconized In-Stream™ programming cells have a unique cell header. The default value is 0x000001FX, which can be changed by writing to the In-Stream™ Cell Header 1, 2, 3 and 4 registers. All four registers can be written to in one four byte write with an In-Stream™ cell. The bytes are written MSB to LSB. The new cell header will be used for returning a Reply Notification cell, following the write operation.

The 77V011 supports the following set of In-Stream™ functions, Discover/Identify, Reset, Register Read, Register Write, Event Notification and Reply Notification.

The Discover/Identify command is sent by the CPU to the 77V011, and is used to either discover the 77V011 or to ensure that the 77V011 is still attached (heart beat).

The Reset command is sent from the CPU to the 77V011, which indicates that the 77V011 must perform a hard reset and re-initialize itself to its default state.

The Register Read command is used to read the value of one or more registers. Up to 32-bytes can be read with one In-Stream™ cell.

The Register Write command is used to write a value to one or more registers. Up to 32-bytes can be written with one In-Stream™ cell.

The Event Notification command is sent from the 77V011 to the CPU and indicates that an event has happened that requires CPU intervention.

The Reply Notification command is sent from the 77V011 to the CPU in response to command cells sent by the CPU. The 77V011 will generate a Reply Notification response to a Discover/Identify, Register Read and Register Write command, but not for a Reset command. This option is enabled by setting the Acknowledge Request bit in the Message Type Field of the In-Stream™ command cell.

The In-Stream™ cell format is broken up into six sections, which vary slightly depending on the type of command the cell caries.

The first five bytes contain the cell header. The In-Stream™ programming cell address is in the first 28-bits with the default value of GFC =0x0, VPI =0x0, VCI =0x001F, PT/CLP =0xX, where X=don't care. The remaining byte is the HEC.

Bytes six and seven of the cell contain the Transaction ID information. This field is two bytes wide and is used to correlate messages requiring a reply to a command. This allows more than one command to be sent to a device without waiting for a Reply Notification cell, as the field is copied from the Command cell to the Reply Notification cell. The 2-byte field is set to zero when an Event Notification cell is generated by the 77V011, with the zero value being valid for this condition only. It is up to the CPU to generate and manage values for it's In-Stream™ commands and not re-use the value for some set amount of time.

Byte 8 contains the Message Type field, which indicates what type of command the cell contains. Bit location eight is not used. Bit seven is the Acknowledge Request bit, which indicates if an acknowledgement to the command cell is required or not. When a Reply Notification cell has to be returned this bit is set to a one. When the Reply Notification cell is returned the bit is reset to zero. This option is not valid with the Reset command, which does not return a Reply Notification cell. Bit five is the Acknowledge bit which indicates whether the cell is a Reply Notification cell or a Command cell. The bit is set to a zero when the cell is a Reply Notification cell, and a one when the cell is a Command cell. Bits zero thru four are the Message Type Indicator. There are currently five options for this field. The Discover/Identify (value = 0x2) command, which will generate a Reply Notification cell with 32 bytes of device specific data located in the Message Data field. The Reset (value = 0x3) command performs a reset on the 77V011. There is no Reply Notification cell returned for this command. The Read Registers (value = 0x5) command performs a read operation to a set of consecutive registers. The returned register data is contained in the Message Data field. The Write Registers (value = 0x6) command performs a write operation to a set of consecutive registers. The data to be written is contained in the Message Data field. The Event Notification (value = 0x8) command generates a Event Notification cell indicating that an interrupt has been detected.

The Device ID field is located in the bytes 9 thru 15. This field is divided into two parts. The first is byte nine, which must be set to 0x01 for the cell to be valid. The remaining six bytes are currently not used and should contain zeros when returning a Reply Notification cell.

Bytes 16 thru 51 are the Message Data field. The layout of this field is dependant on the Message Type field. A Read or Write command will have a Message Data field divided into three sub fields. The first sub field is one byte wide and indicates how many bytes of data are valid in the data portion of the Message Data field. The second sub field is three bytes wide and contains the base address for the Read or Write command. The third sub field is the valid data and padding. Valid data is written starting at the base address in accordance with the number of valid bytes indicator (first sub field). The remaining space, if any, is padded with zeros. A Discover/Identify command has a Message Data field divided into two sub fields.The first sub field is the first 32-bytes of the Message Data field, which contains up to 32 bytes read from the EEPROM. The remaining four bytes are reserved. An Event Notification command will have a Message Data field split into two sub fields. The first sub field is four bytes wide and contains an event number, which is always zeros. The second sub field contains one byte of data (byte 20) indicating what type of event happened, which is described in the Event Notification Table. The remaining bytes 21 to 51 are padding and contain zeros.

Bytes 52 and 53 contain the CRC-10 trailer, with the upper six bits of byte 52 containing zeros. The CRC-10 is generated and used in the same manner as in AAL3/4 cells.

Table 18: In-Stream™ Register Table

Register Name	Register Address	Bit #	Bit Name	Value Range	Default Value	Description
In-Stream™ Cell Header Byte 0	800F	[7:0]	In-Stream™ Header [31:24]	0x00 - 0xFF	0x00	Cell header used for In-Stream™ programming cells.
In-Stream™ Cell Header Byte 1	8010	[7:0]	In-Stream™ Header [23:16]	0x00 - 0xFF	0x00	Cell header used for In-Stream™ programming cells.
In-Stream™ Cell Header Byte 2	8011	[7:0]	In-Stream™ Header [15:8]	0x00 - 0xFF	0x01	Cell header used for In-Stream™ programming cells.
In-Stream™ Cell Header Byte 3	8012	[7:0]	In-Stream™ Header [7:0]	0x00 - 0xFF	0xF0	Cell header used for In-Stream™ programming cells.

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Table 19: In-Stream™ Programming Message Type Indicator

Name	Message Type ID	Description
Discover/ Identify	2	This command will generate an Acknowledge Reply cell containing 32 bytes of device specific data, which is stored in bytes 8 through 39 of the EEPROM.
Reset	3	Performs a reset on 77V011 device. No Reply Notification Cell is returned acknowledging that the reset command has been completed.
Read Registers	5	Read from a consecutive number of registers.
Write Registers	6	Write to a consecutive number of registers.
Event Notification	8	An unsolicited Event Notification cell indicating an event has taken place. The event can be either a PHY interrupt or a Address Range Error.

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Table 20: Event Notification Table

Bit #	Event	Description
0	PHY Interrupt Time Out	A PHY interrupt was detected more than 25ms ago, but the PHY Interrupt bit of the Status register has not been cleared.
1	PHY Interrupt Status	A PHY interrupt has been detected.
2	Address Range Error Time Out	An address range error was detected more than 25ms ago, but the Address Range Error bit of the Status register has not been cleared.
3	Address Range Error Status	An address range error has been detected.
7:4	Not Used	

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Figure 20: General Format In-Stream™ Prgramming Cell Format

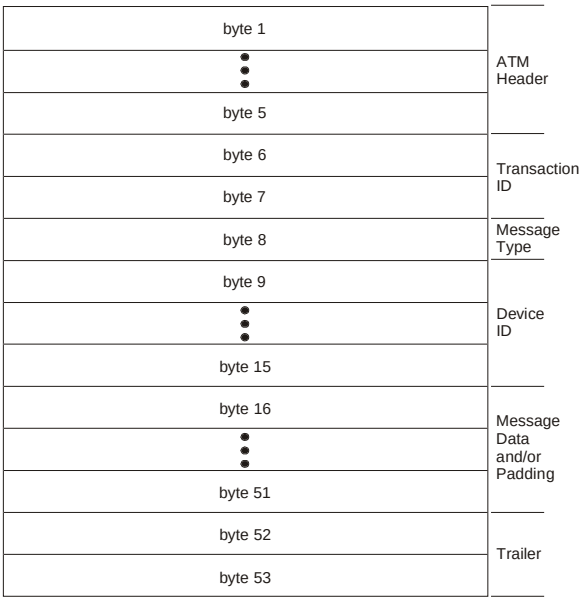


Figure 21: Valid header Formats for In-Stream™ Programming Cell

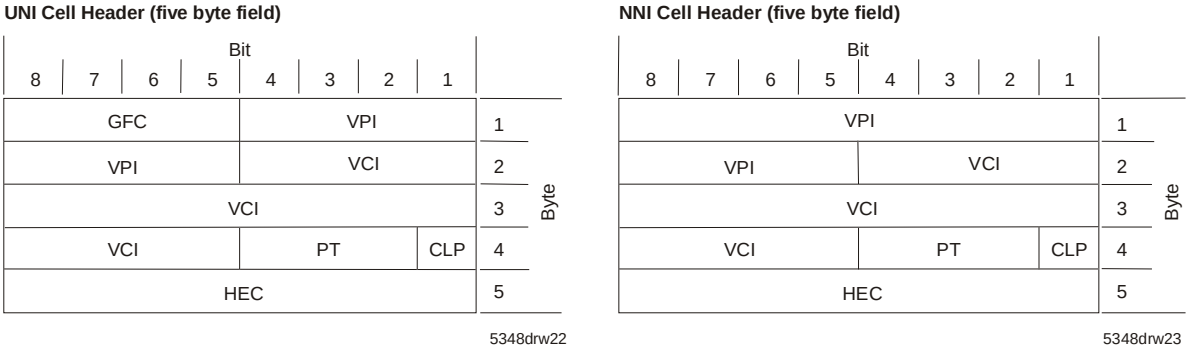


Figure 22: Valid Transaction Field Formats for In-Stream™ Programming Cell

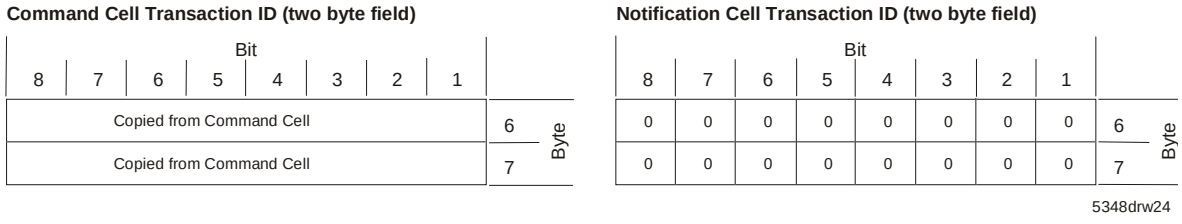


Figure 23: Valid Message Type Format for In-Stream™ Programming Cell

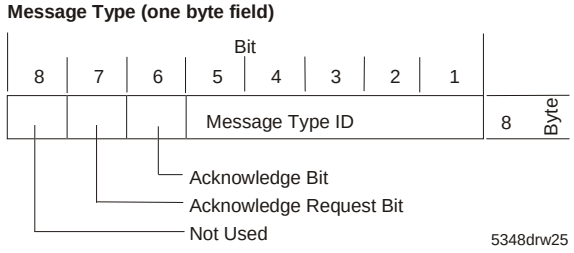


Figure 24: Valid Device ID Field Format for In-Stream™ Programming Cell

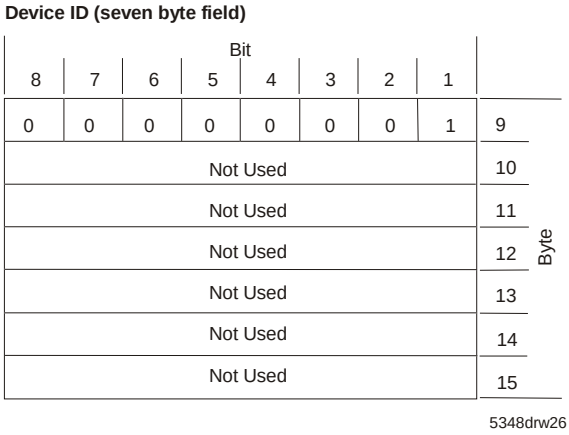
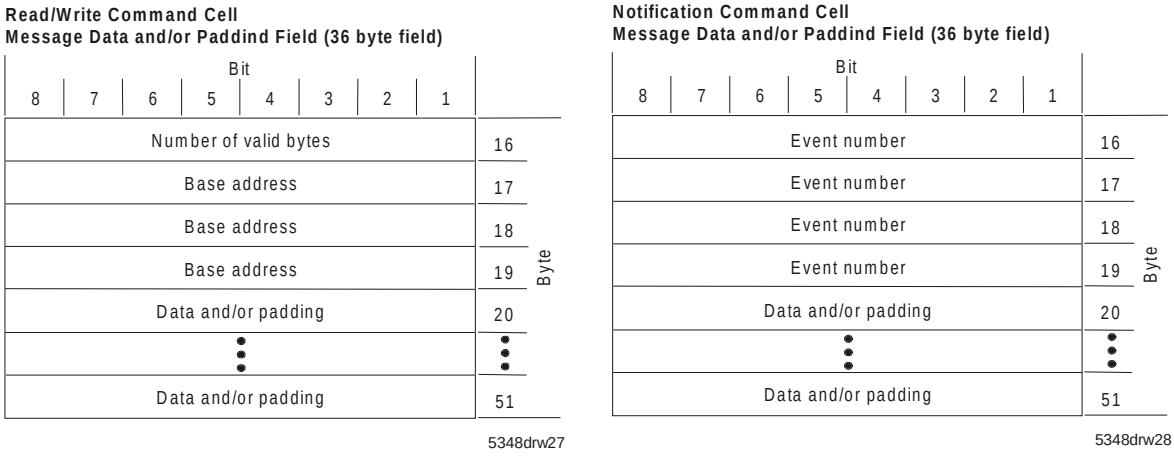


Figure 25: Valid Message and/or Data Field Format for In-Stream™ Programming Cell



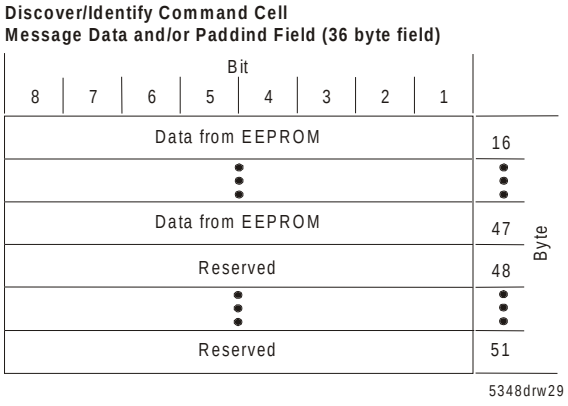
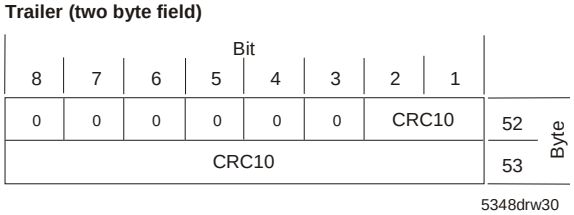


Figure 26: Valid Trailer Field Format for In-Stream™ Programming Cell



Notification Cell

There are two types of Notification cells, Event and Reply, that can be generated by the 77V011.

The 77V011 will generate an Event Notification Cell if an interrupt is detected on the external $\overline{\text{PHYINT}}$ pin, or if an Address Range Error is encountered. A second Event Notification cell will be generated if the interrupt is not cleared within 25ms of when it occurred. Additional Event Notification cells will be generated every 12ms thereafter until the interrupt is cleared. A new event will not be reported until the related interrupt has been cleared. It is up to the CPU to clear the interrupt, or to notify higher layers that an interrupt has occurred. The interrupts are cleared by writing a one to the PHY Interrupt or Address Range Error bits in the Status register. Writing a one will clear the interrupt and reset the register bit to zero.

The 77V011 will generate a Reply Notification cell if the Acknowledge Request bit is set to a one. Reply Notification cells enable the CPU to keep status of its command cells.

Interpreting and Clearing Interrupts

When an interrupt occurs the Status register will indicate where the interrupt occurred.

The PHY Interrupt Mask and Rx Address Error bits of the Notification Mask register determine if a Event Notification cell will be generated when an interrupt is detected. The 77V011 will not generate a Event Notification cell when an interrupt occurs if the register is set to the default of zero, and will generate a Event Notification cell if set to a one.

The Tx Cell Drop bit of the Status register must be polled by the CPU to determine if it is set or not set. An Event Notification cell is not generated when this bit is set, and no action needs to be taken by the CPU. However, the bit must be cleared, by writing a zero to it, in order to detect additional cells that have been dropped.

The PHY Interrupt Status and Address Error Status bits of the Timeout Status register indicate that the interrupt occurred more than 25ms ago. This is a read only register used to verify that the interrupts are being cleared by the CPU. Once an interrupt is detected the 77V011 will monitor the appropriate Status register bit to determine if the interrupt is cleared. The 77V011 will generate a Event Notification cell, mask bit must be set to a one, if the interrupt is not cleared within 25ms of when the interrupt occurred and will set the Timeout Status bit. It will generate additional Event Notification cells on 12ms intervals, thereafter, until the interrupt is cleared. It is the CPU's responsibilty to clear the interrupt and/or notify higher layers that an interrupt has been encountered. The interrupt is cleared by the CPU writing a one to the appropriate Status register bit. Writing a one will clear the interrupt and reset the register bit back to zero.

See Interrupt Register Table for description of interrupt registers.

Table 21: Interrupt Register Table

Register Name	Register Address	Bit #	Bit Name	Value Range	Default Value	Description
Notification Mask	8008	0	PHY Interrupt Mask	0 - 1	0	Mask interrupt notification. "0" no Event Notification cell will be generated when a PHY interrupt occurrs, "1" generate Event Notification cell when a PHY interrupt occurrs.
Status	8009	0	PHY Interrupt	0 - 1	0	When a interrupt occurrs on the $\overline{\text{PHYINT}}$ pin this bit will be set to a one. "0" no interrupt detected, "1" PHY interrupt detected.
Timeout Status	800A	0	PHY Interrupt Status	0 - 1	0	Indicates that a PHY interrupt occurred more than 25ms ago, and the PHY Interrupt bit of the Status register has not been cleared. This bit will return to zero once the interrupt is cleared. "0" no PHY interrupt detected, "1" interrupt occurred more than 25ms ago and has not been cleared.

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Cell Accounting

The transmit and receive cell counters are always enabled. At reset the counters are set to zero and will increment by one each time a cell is received or transmitted over the UTOPIA interface. The counter values are stored in the UTOPIA Tx and Rx Cell Counter registers and can be read at any time. The counters will roll over once the maximum cell count is reached.

Misc. Features

The 77V011 offers two external control pins, CNTRL_A and CNTRL_B, that can be connected to an external device for system design engineer usage. Both of these signals are low after reset. There is also a register associated with each control pin signal, which is described in the Misc. Register Table.

Table 22: Cell Counter Register Table

Register Name	Address (HEX)	Bit Location	Bit Name	Default Value	Description
UTOPIA Rx Cell Counter byte 3	801B	[7:0]	Rx Cell Counter [31:24]	0x00	Counter for cells transferred on the receive UTOPIA 2 bus. This counter will wrap around once the maximum cell count is reached.
UTOPIA Rx Cell Counter byte 2	801C	[7:0]	Rx Cell Counter [23:16]	0x00	Counter for cells transferred on the receive UTOPIA 2 bus. This counter will wrap around once the maximum cell count is reached.
UTOPIA Rx Cell Counter byte 1	801D	[7:0]	Rx Cell Counter [15:8]	0x00	Counter for cells transferred on the receive UTOPIA 2 bus. This counter will wrap around once the maximum cell count is reached.
UTOPIA Rx Cell Counter byte 0	801E	[7:0]	Rx Cell Counter [7:0]	0x00	Counter for cells transferred on the receive UTOPIA 2 bus. This counter will wrap around once the maximum cell count is reached.
UTOPIA Tx Cell Counter byte 3	801F	[7:0]	Tx Cell Counter [31:24]	0x00	Counter for cells transferred on the transmit UTOPIA 2 bus. This counter will wrap around once the maximum cell count is reached.
UTOPIA Tx Cell Counter byte 2	8020	[7:0]	Tx Cell Counter [23:16]	0x00	Counter for cells transferred on the transmit UTOPIA 2 bus. This counter will wrap around once the maximum cell count is reached.
UTOPIA Tx Cell Counter byte 1	8021	[7:0]	Tx Cell Counter [15:8]	0x00	Counter for cells transferred on the transmit UTOPIA 2 bus. This counter will wrap around once the maximum cell count is reached.
UTOPIA Tx Cell Counter byte 0	8022	[7:0]	Tx Cell Counter [7:0]	0x00	Counter for cells transferred on the transmit UTOPIA 2 bus. This counter will wrap around once the maximum cell count is reached.

5348tbl33

Table 23: Misc. Register Table

Register Name	Register Address	Bit #	Bit Name	Range Values	Default Values	Description
Pin Controls	801A	1	Control A	0 - 1	0	Stores condition of Control A pin. "0" CNTRL_A = "0", "1" CNTRL_A = "1".
		2	Control B	0 - 1	0	Stores condition of Control B pin. "0" CNTRL_B = "0", "1" CNTRL_B = "1".

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AC Electrical Characteristics

(Industrial: Vcc= 5V ± 10%, T_A = -40°C to 85°C)

Symbol	Parameter	77V011 Min.	77V011 Max.	Unit
t_{CYC}	SCLK Cycle Time	20	—	ns
t_{CH}	SCLK High Time	8	—	ns
t_{CL}	SCLK Low Time	8	—	ns
t_{UCYC}	UTOPIA TCLK/RCLK Cycle Time	25	—	ns
t_{UCH}	UTOPIA TCLK/RCLK High Time	10	—	ns
t_{UCL}	UTOPIA TCLK/RCLK Low Time	10	—	ns
t_{TOV}	TxDATA, TENB, TSOC Output Valid from TCLK	2	20	ns
t_{UTS}	TCLAV to TCLK Setup Time	4	—	ns
t_{UTH}	TCLAV to TCLK Hold Time	10	—	ns
t_{ROV}	$\overline{RENB}$ Output Valid from RCLK	—	20	ns
t_{URS}	RxDATA, RSOC, RCLAV to RCLKSetup Time	10	—	ns
t_{URH}	RxDATA, RSOC, RCLAV to RCLK Hold Time	1	—	ns
t_{DCYC}	DPI DTxCLK/DRxCLK Cycle Time	20	—	ns
t_{DCH}	DPI DTxCLK/DRxCLK High Time	8	—	ns
t_{DCL}	DPI DTxCLK/DRxCLK Low Time	8	—	ns
t_{DTS}	DTxFRM, DTxDATA to DTCLK Setup Time	4	—	ns
t_{DTH}	DTxFRM, DTxDATA to DTCLK Hold Time	2	—	ns
t_{PDRD}	DRxCLK to DRxDATA(0-3), DRxFRM Propagation Delay	—	10	ns
t_{ALPW}	ALE Pulse Width	20	—	ns
t_{ALR}	System Clock to $\overline{READ}$ Low Propagation Delay	—	20	ns
t_{ALW}	System Clock to $\overline{WRITE}$ Low Propagation Delay	—	20	ns
t_{RDPW}	Read Pulse Width	80	—	ns
t_{AAL}	Address to ALE Falling Edge Setup Time	20	—	ns
t_{ALA}	Address to ALE Falling Edge Hold Time	10	—	ns
t_{DRS}	Data to rising edge of $\overline{READ}$ Setup Time	5	—	ns
t_{DRH}	Data to rising edge of $\overline{READ}$ Hold Time	1	—	ns
t_{DWS}	Data to rising edge of $\overline{WRITE}$ Setup Time	5	—	ns
t_{DWH}	Data to rising edge of $\overline{WRITE}$ Hold Time	1	—	ns
t_{WRPW}	Write Pulse Width	40	—	ns
t_{PINTS}	System Clock to $\overline{PHYINT}$ Setup Time	10	—	ns
t_{PINTH}	System Clock to $\overline{PHYINT}$ Hold Time	1	—	ns
t_{PALE}	ALE to System Clock Propagation Delay	—	20	ns
t_{PPHY}	System Clock to $\overline{PHYCS}$ Propagation Delay	—	20	ns
t_{PPHYR}	System Clock to $\overline{PHYRST}$ Propagation Delay	—	20	ns
t_{PRCLK}	System Clock to Utopia Receive Clock Propagation Delay	—	20	ns
t_{PTCLK}	System Clock to Utopia Transmit Clock Propagation Delay	—	20	ns
$t_{PDRxCLK}$	System Clock to DPI Receive Clock Propagation Delay	—	20	ns
$t_{PDTxCLK}$	System Clock to DPI Transmit Clock Propagation Delay	—	20	ns
t_{PRLED}	System Clock to RxLED Propagation delay	—	20	ns
t_{PTLED}	System Clock to TxLED Propagation delay	—	20	ns
t_{PCNTA}	System Clock to CONT_A Propagation delay	—	20	ns
t_{PCNTB}	System Clock to CONT_B Propagation delay	—	20	ns

5348tbl35

AC Electrical Characteristics Continued

(Industrial: Vcc= 5V ± 10%, TA = -40°C to 85°C)

Symbol	Parameter	77V011 Min.	77V011 Max.	Unit
t_{RSTW}	$\overline{SYSRST}$ pulse width	100	—	ns
t_{ECYC}	EECLK Cycle Time	1000	—	ns
t_{PECLK}	SYSCLK to EECLK, $\overline{EECS}$, EEDOUT Propagaton Delay	—	20	ns
t_{SEDI}	SYSCLK to EEDIN Setup Time	—	10	ns
t_{HEDI}	SYSCLK to EEDIN Hold Time	2	—	ns
t_{ADRS}	ADDR to $\overline{RD/DS}$ Falling Edge Setup Time	10	—	ns
t_{ADRH}	ADDR to $\overline{RD/DS}$ Rising Edge Hold Time	4	—	ns
t_{SELRS}	$\overline{SEL}$ to $\overline{RD/DS}$ Falling Edge Setup Time	5	—	ns
t_{SELRH}	$\overline{SEL}$ to $\overline{RD/DS}$ Rising Edge Hold Time	0	—	ns
t_{DARIV}	DATA Invalid/Tri-state to $\overline{RD/DS}$ Rising Edge	15	—	ns
t_{DARV}	DATA Valid to $\overline{RDY/DTACK}$ Falling Edge	—	10	ns
t_{RDYRV}	$\overline{RDY/DTACK}$ Valid to $\overline{RD/DS}$ Falling Edge	—	15	ns
t_{RDYRT}	$\overline{RDY/DTACK}$ Tri-state to $\overline{RD/DS}$ Rising Edge	10	—	ns
t_{RDPW}	$\overline{RD/DS}$ Pulse Width	50	—	ns
t_{RDYWV}	$\overline{RDY/DTACK}$ to $\overline{WR/RW}$ Falling Edge	—	15	ns
t_{RDYWT}	$\overline{RDY/DTACK}$ Tri-state to $\overline{WR/RW}$ Rising Edge	—	10	ns
t_{ADWS}	ADDR to $\overline{WR/RW}$ Falling Edge Setup Time	15	—	ns
t_{SELWS}	$\overline{SEL}$ to $\overline{WR/RW}$ Falling Edge Setup Time	5	—	ns
t_{SELWH}	$\overline{SEL}$ to $\overline{WR/RW}$ Rising Edge Hold Time	0	—	ns
t_{DAWS}	DATA to $\overline{WR/RW}$ Rising Edge Setup Time	15	—	ns
t_{DAWH}	ADDR, DATA to $\overline{WR/RW}$ Rising Edge Hold Time	4	—	ns
t_{WRPW}	$\overline{WR/RW}$ Pulse Width	50	—	ns

5348tbl36

Figure 27: System Clock Timing Waveform

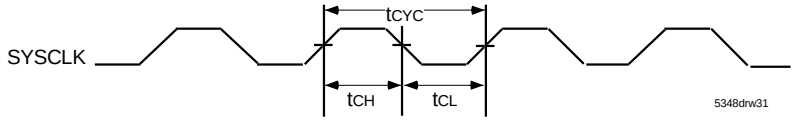

Figure 28: System Clock to UTOPIA Receive Clock Propagation Delay

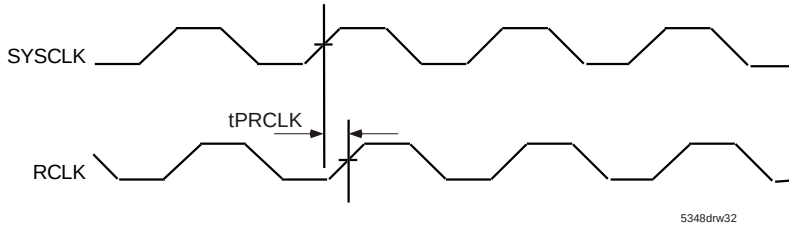

Figure 29: System Clock to UTOPIA Transmit Clock Propagation Delay

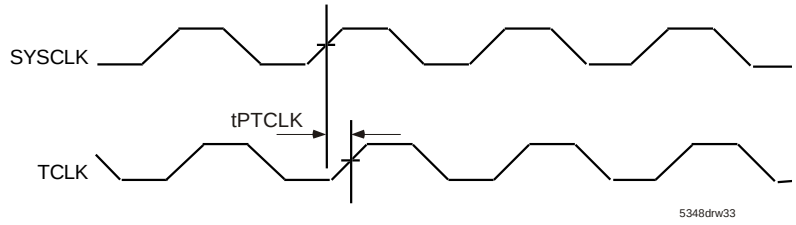

Figure 30: System Clock to DPI Receive Clock Propagation Delay

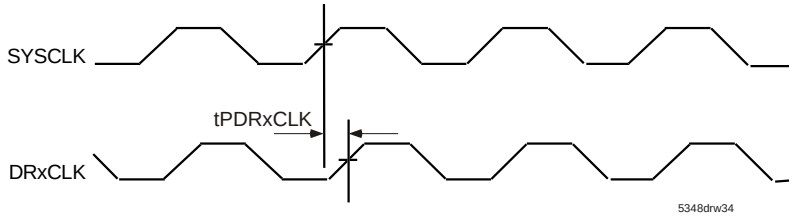

Figure 31: System Clock to DPI Transmit Clock Propagation Delay

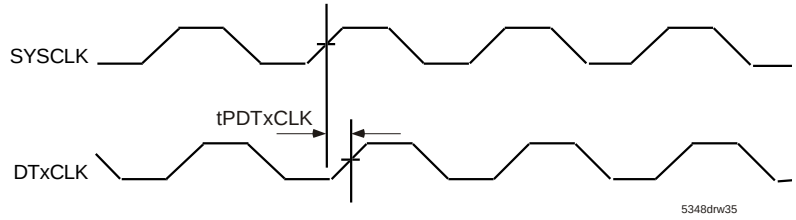

Figure 32: UTOPIA Transmit Timing Waveform

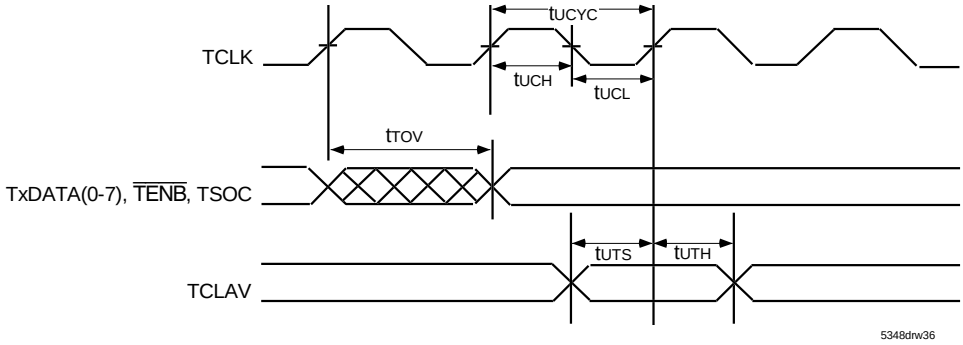

Figure 33: UTOPIA Receive Timing Waveform

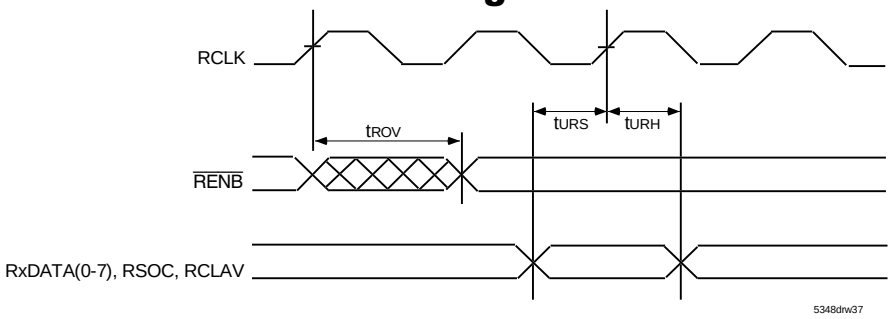

Figure 34: DPI Transmit Timing Waveform

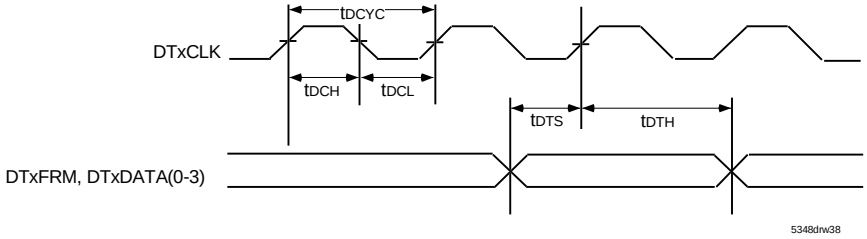

Figure 35: DPI Receive Timing Waveform

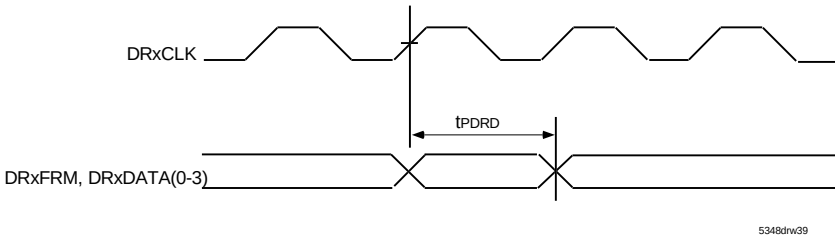

Figure 36: System Clock to $\overline{\text{PHYRST}}$ Propagation Delay

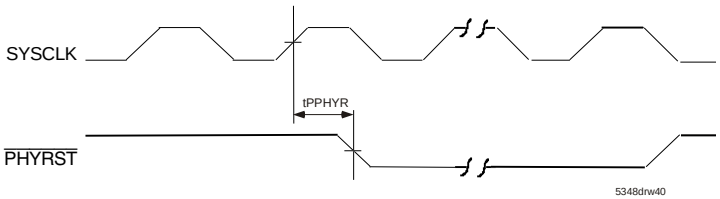

Figure 37: System Clock to $\overline{\text{PHYINT}}$ Propagation Delay

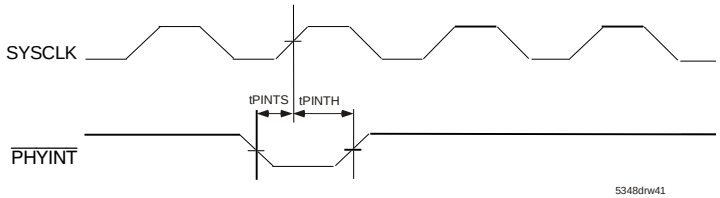

Figure 38: $\overline{\text{SYSRST}}$ Timing Waveform

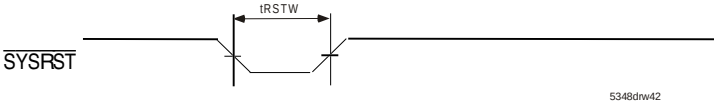

Figure 39: EEPROM Timing Waveform

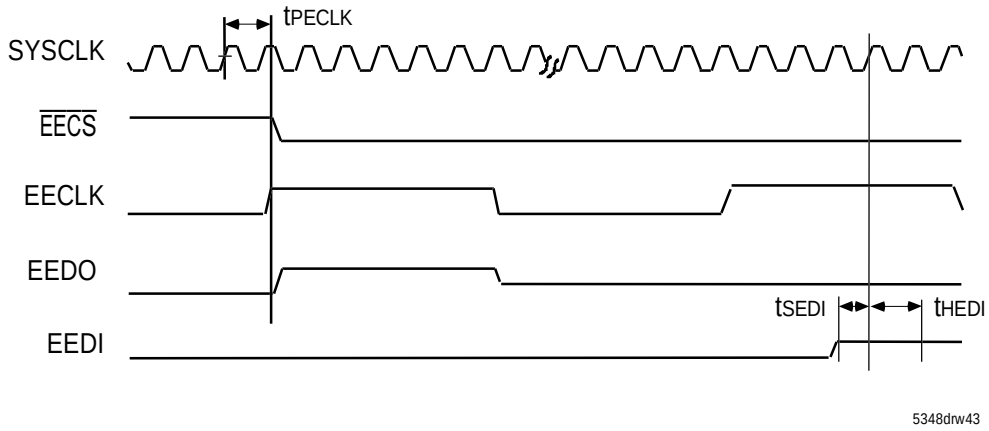

Table 24: Internal Register Map

Register Name	Address (HEX)	Bit Location	Bit Name	Default Value	Description
Device ID	8000	[7:0]	Device Version Number	0x10	This is the device version number. 77V011 = 0x10.
Configuration 1	8001	0	Drop Tx Cell	0	Selects whether or not to drop cell with invalid Subport Address. "0" do not drop the cell, "1" drop the cell.
		1	Copy EFCI	0	Selects whether or not to OR the EFCI bit of the cell header with the EFCI bit of the 4-byte TAG area, and place the OR'ed EFCI bit in the cell header. "0" do not OR the EFCI bit to the 4-byte TAG area, "1" OR the EFCI bit to the 4-byte TAG area.
		2	Rx Move PT/CLP	0	Selects whether or not to move the PT/CLP fields from the cell header into the 4-byte TAG area. "0" do not move the PT/CLP to the 4-byte TAG area, "1" move the PT/CLP to the 4-byte TAG area.
		3	Tx Move PT/CLP	0	Selects whether or not to move the PT/CLP fields from the 4-byte TAG area to the cell header. "0" do not move the PT/CLP fields to the cell header, "1" move the PT/CLP fields to the cell header.
		[7:4]	Not Used		
Configuration 2	8002	[1:0]	Stall Tx	0x0	Selects whether or not to stall the pipeline if the PHY transmit FIFO is full. "0" drop the cell, "1" stall the pipeline indefinitely, "2" stall the pipeline for Stall Cycles.
		[6:2]	Max Subports	0x1E	Indicates the maximum subport address value for the PHY(s) connected to the transmit UTOPIA II interface.
		7	Not Used		
Configuration 3	8003	[7:0]	Stall Tx Cycles	0xFF	Number of TCLK cycles the interface has to stall the pipeline when the PHY transmit FIFO is full. This field is valid only if the Stall Pipeline for Stall Cycles option is selected.
Tx TAG	8004	[2:0]	Tx TAG Size	Defined by pin	Number of bytes to remove from the ATM cell in the transmit direction. Valid values are from zero to four.
		3	Tx Add HEC	Defined by pin	Add a HEC placeholder in the transmit direction. "0" do not add a HEC placeholder, "1" add a HEC placeholder.
		4	Tx TAG Location	Defined by pin	TAG location in transmit direction. "0" transmit TAG is located at the beginning of the cell, "1" transmit TAG is located at the end of the cell.
		[7:5]	Not Used		
Rx TAG	8005	[2:0]	Rx TAG Size	Defined by pin	Number of bytes to add to ATM cel in the receive direction. Valid values are from zero to four.
		3	Rx Remove HEC	Defined by pin	Remove HEC byte from cell. "0" do not remove the HEC byte from the cell, "1" remove the HEC byte from the cell.
		4	Rx TAG Location	Defined by pin	TAG location in receive direction. "0" receive TAG is located at the beginning of the cell, "1" receive TAG is located at the end of the cell.
		[7:5]	Not Used		
Mode Select	8006	0	Dpi Size	Defined by pin	Selects the size of the DPI Tx and Rx data bus. "0" 4-bit DPI Tx and Rx data bus, "1" 8-bit DPI Tx and Rx data bus.
		1	Dpi Mode	Defined by pin	Selects DRxCLK direction. "0" switch mode (output), "1" normal mode (input).
		2	UTOPIA 2 Size	Defined by pin	Selects the size of the UTOPIA 2 Tx and Rx data bus. "0" 8-bit UTOPIA 2 Tx and Rx data bus, "1" 16-bit UTOPIA 2 Tx and Rx data bus.
		3	UTOPIA Management Mode	Defined by pin	Selects type of management interface to use. "0" Utility bus style, "1" UTOPIA 2 management style.
		4	Init from EEPROM	Defined by pin	Five byte write from EEPROM to In-Stream™ Cell Header and In-Stream™ Subport registers at reset. "0" do not write five byte value, "1" write five byte value to registers.
		[7:5]	Not Used		
PHY Reset	8007	0	PHY Reset	0	PHY Reset. "0" do not reset the PHY, "1" reset the PHY(PHYRST signal will be asserted low for at least 16 SYSCLK cycles.
		[7:1]	Not Used		
Notification Mask	8008	0	PHY Interrupt Mask	0	Mask interrupt notification. "0" no Event Notification cell will be generated when a PHY interrupt occurrs, "1" generate Event Notification cell when a PHY interrupt occurrs.
		1	Rx Address Error	0	Mask Address Range Error notification. "0" no Event Notification cell will be generated when a Rx Out of Range Address Error occurrs, "1" generate Event Notification cell when a Rx Out of Range Address Error occurrs.
		[7:2]	Not Used		
Status	8009	0	PHY Interrupt	0	When a PHY interrupt occurrs on the external PHY interrupt pin this bit will be set high. "0" no interrupt detected, "1" PHY interrupt detected.
		1	Address Range Error	0	Address Range Error indication when an Address Range Error occurrs. "0" no Address Range Error detected, "1" Address Range Error has been detected.
		2	Tx Cell Dropped	0	Indicates if any cells have been dropped at the transmit UTOPIA interface. This is a status indicator for the Stall Tx bit of the Configuration 2 register "0" no cells have been dropped, "1" a cell was dropped because the PHY did not respond.
		[7:3]	Not Used		

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Internal Register Map (con't.)

Register Name	Address (HEX)	Bit Location	Bit Name	Default Value	Description
Timeout Status	800A	0	PHY Interrupt Status	0	Indicates that a PHY interrupt occurred more than 25ms ago, and the PHY Interrupt bit of the Status register has not been cleared. This bit will return to zero once the interrupt is cleared. "0" no PHY interrupt detected, "1" interrupt occurred more than 25ms ago and has not been cleared.
		1	Address Error Status	0	Indicates that a Address Error occurred more than 25ms ago, and Address Range Error bit of the Status register has not been cleared. This bit will return to zero once the interrupt is cleared. "0" no Address Range Errors detected, "1" Address Range Error occurred more than 25ms ago and has not been cleared.
		[7:2]	Not Used		
Rx Out of Range Subport	800B	[4:0]	Rx Out of Range Subport	0x00	The subport address of a cell containing an invalid cell header.
		[7:5]	Not Used		
Rx Out of Range Address Mask byte 2	801C	[7:0]	Address Mask Register [23:16]	0x00	Value used to validate cells on the Rx UTOPIA interface.
Rx Out of Range Address Mask byte 1	800D	[7:0]	Address Mask Register [15:8]	0x00	Value used to validate cells on the Rx UTOPIA interface.
Rx Out of Range Address Mask byte 0	800E	[7:0]	Address Mask Register [7:0]	0x00	Value used to validate cells on the Rx UTOPIA interface.
In-Stream™ Cell Header byte 3	800F	[7:0]	In-Stream™ Header [31:24]	0x00	Cell header used for In-Stream™ programming cells.
In-Stream™ Cell Header byte 2	8010	[7:0]	In-Stream™ Header [23:16]	0x00	Cell header used for In-Stream™ programming cells.
In-Stream™ Cell Header byte 1	8011	[7:0]	In-Stream™ Header [15:8]	0x01	Cell header used for In-Stream™ programming cells.
In-Stream™ Cell Header byte 0	8012	[7:0]	In-Stream™ Header [7:0]	0xF0	Cell header used for In-Stream™ programming cells.
Subport Configuration 1	8013	[4:0]	In-Stream™ Subport	0x00	Subport address used to filter In-Stream™ programming cells.
		[7:5]	Tx Subport Width	0x5	Programs how many bits will be used for subport addressing in the transmit direction.
Modify Tx Subport	8014	[4:0]	New Subport	0x00	New value used to replace subport address in outgoing cells. This value will only be used if the Replace Subport bit of the Modify Tx Subport register is set to a one.
		5	Replace Subport	0	Indicates whether or not to replace the subport address in transmit cells. "0" do not replace the subport address, "1" replace the subport address with the value in the New Subport bits of the Modify Tx Subport register.
		[7:6]	Not Used		
Tx Subport Position	8015	[2:0]	Tx Byte Location	Defined by pin	Indicates what byte of the transmit cell header the subport starts in. The subport address can cross the byte boundary.
		[5:3]	Tx Bit Location	0x5	Indicates what bit of the byte defined by the Tx Byte Location bits of the Tx Subport Position register the MSB of the transmit subport address starts. The subport address can cross the byte boundary.
		[7:6]	Not Used		
TAG byte 3	8016	[7:0]	TAG [31:24]	0x00	TAG added to cell.
TAG byte 2	8017	[7:0]	TAG [23:16]	0x00	TAG added to cell.
TAG byte 1	8018	[7:0]	TAG [17:8]	0x01	TAG added to cell.
TAG byte 0	8019	[7:0]	TAG [7:0]	0xF0	TAG added to cell.

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Internal Register Map (con't.)

Register Name	Address (HEX)	Bit Location	Bit Name	Default Value	Description
Pin Controls	801A	0	Override Pin Configuration	0	Enables writing to pin configurable registers during normal operation. "0" pin configurable registers are read only, "1" pin configurable registers are read/write registers.
		1	Control A	0	Stores condition of Control A pin. "0" CNTRL_A = "0", "1" CNTRL_A = "1".
		2	Control B	0	Stores condition of Control B pin. "0" CNTRL_B = "0", "1" CNTRL_B = "1".
		3	EEPROM Mux Select	0	Indicates if the EEPROM interface will be connected to the internal logic or the EEPROM registers. "0" connected to internal logic, "1" connected to EEPROM registers.
		4	EEPROM Clock Out	0	EEPROM clock when EEPROM interface is connected to the EEPROM registers. "0" clock low, "1" clock high.
		5	EEPROM Chip Select	0	EEPROM chip select when EEPROM interface is connected to the EEPROM registers. "0" EEPROM interface is selected, "1" EEPROM interface is not selected.
		6	EEPROM Out	0	EEPROM serial output when EEPROM interface is connected to the EEPROM registers.
		7	EEPROM In	0	EEPROM serial input when EEPROM interface is connected to the EEPROM registers.
UTOPIA Rx Cell Counter byte 3	801B	[7:0]	Rx Cell Counter [31:24]	0x00	Counter for cells transferred on the receive UTOPIA 2 bus. This counter will wrap around once the maximum cell count is reached.
UTOPIA Rx Cell Counter byte 2	801C	[7:0]	Rx Cell Counter [23:16]	0x00	Counter for cells transferred on the receive UTOPIA 2 bus. This counter will wrap around once the maximum cell count is reached.
UTOPIA Rx Cell Counter byte 1	801D	[7:0]	Rx Cell Counter [15:8]	0x00	Counter for cells transferred on the receive UTOPIA 2 bus. This counter will wrap around once the maximum cell count is reached.
UTOPIA Rx Cell Counter byte 0	801E	[7:0]	Rx Cell Counter [7:0]	0x00	Counter for cells transferred on the receive UTOPIA 2 bus. This counter will wrap around once the maximum cell count is reached.
UTOPIA Tx Cell Counter byte 3	801F	[7:0]	Tx Cell Counter [31:24]	0x00	Counter for cells transferred on the transmit UTOPIA 2 bus. This counter will wrap around once the maximum cell count is reached.
UTOPIA Tx Cell Counter byte 2	8020	[7:0]	Tx Cell Counter [23:16]	0x00	Counter for cells transferred on the transmit UTOPIA 2 bus. This counter will wrap around once the maximum cell count is reached.
UTOPIA Tx Cell Counter byte 1	8021	[7:0]	Tx Cell Counter [15:8]	0x00	Counter for cells transferred on the transmit UTOPIA 2 bus. This counter will wrap around once the maximum cell count is reached.
UTOPIA Tx Cell Counter byte 0	8022	[7:0]	Tx Cell Counter [7:0]	0x00	Counter for cells transferred on the transmit UTOPIA 2 bus. This counter will wrap around once the maximum cell count is reached.
Subport Configuration 2	8023	[2:0]	Rx Subport Width	0x5	Programs how many bits will be used for subport addressing in the receive direction.
		[7:3]	Not Used		
Rx Subport Position	8024	[2:0]	Rx Byte Location	Defined by pin	Indicates what byte of the receive cell header the subport starts in. The subport address can cross the byte boundary.
		[5:3]	Rx Bit Location	0x5	Indicates what bit of the byte defined by the Rx Byte Location bits of the Rx Subport Position register the MSB of the receive subport address starts. The subport address can cross the byte boundary.
		[7:6]	Not Used		

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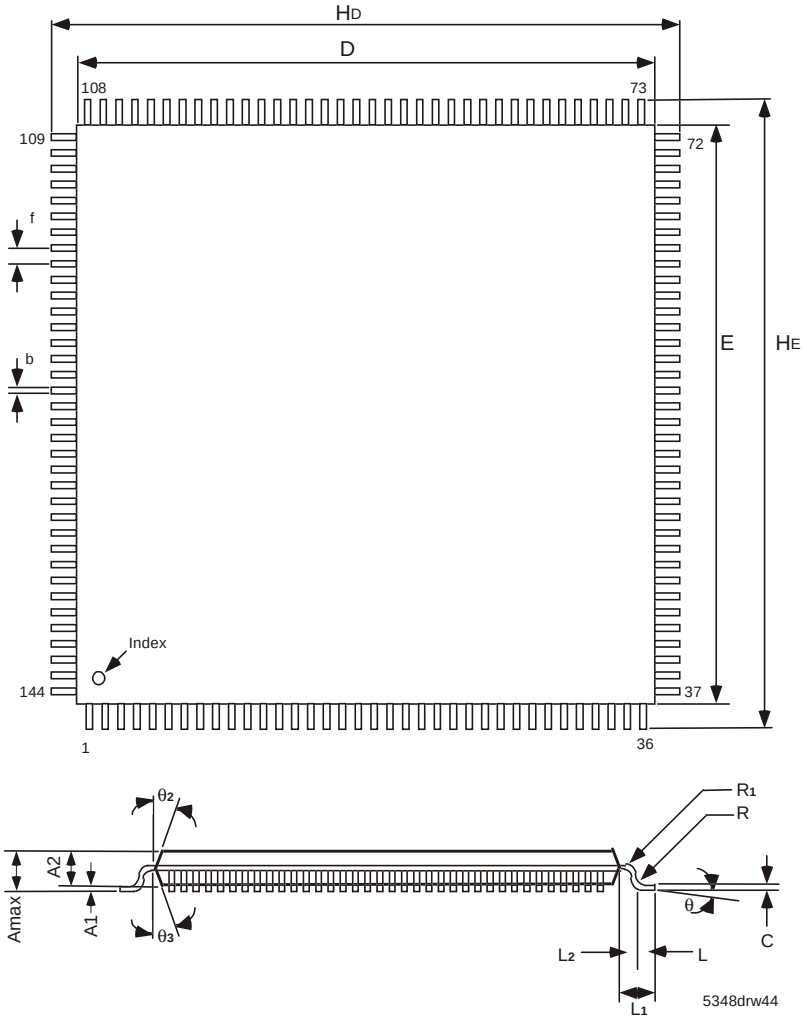
Package Information

Plastic QFP 144pin Body size 20 x 20 x 1.4 mm



Symbol	Dimension in Milimeters			Dimension in inches *		
	Min.	Nom.	Max.	Min.	Nom.	Max.
E	19.9	20	20.1	(0.784)	(0.787)	(0.791)
D	19.9	20	20.1	(0.784)	(0.787)	(0.791)
A			1.7			(0.066)
A1		0.1			(0.004)	
A2	1.3	1.4	1.5	(0.052)	(0.055)	(0.059)
f		0.5			(0.020)	
b	0.15	0.2	0.3	(0.006)	(0.008)	(0.011)
C	0.1	0.125	0.175	(0.004)	(0.005)	(0.006)
q	0°		10°	(0°)		(10°)
L	0.3	0.5	0.7	(0.012)	(0.020)	(0.027)
L1		1			(0.039)	
L2		0.5			(0.020)	
HE	21.6	22	22.4	(0.851)	(0.866)	(0.881)
HD	21.6	22	22.4	(0.851)	(0.866)	(0.881)
q2		12°			(12°)	
q3		12°			(12°)	
R		0.2			(0.008)	
R1		0.2			(0.008)	

* for reference

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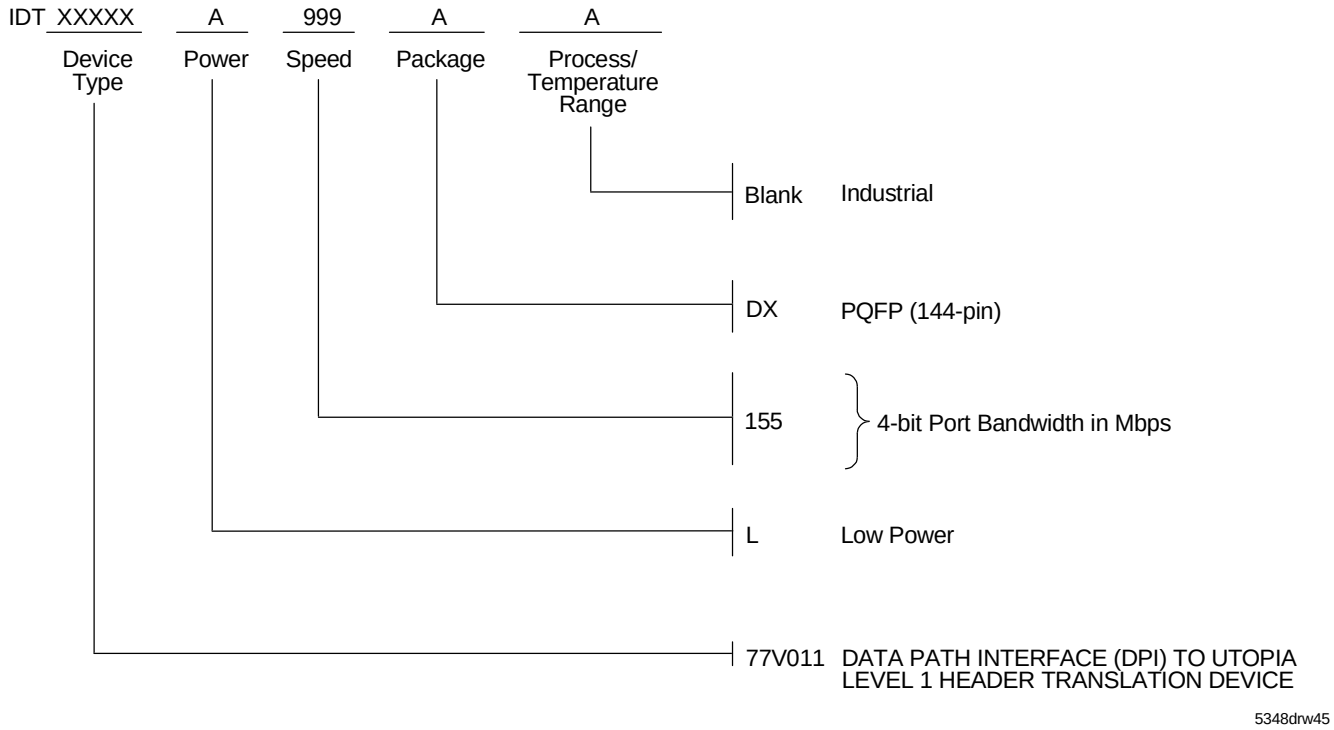
Ordering Information



5348drw45

Preliminary Datasheet: Definition

"PRELIMINARY' datasheets contain descriptions for products soon to be, or recently released to production, including features, pinouts and block diagrams. Timing data are based on simulation or initial characterization and are subject to change upon full characterization.

Datasheet Document History

9/28/99 Initial Public Release

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