CPC710 PCI Bridge and Memory Controller Data Sheet

Features

- IBM CPC710 PowerPC® to PCI bridge
  - 2.5V PPC60x processor bus running at up to 133MHz
  - Dual 32- and 64-bit PCI interfaces
  - 100- and 133-MHz SDRAM interface
  - Internal DMA controller
  - 2-MB Flash boot ROM support
  - 256-MB Extended Flash support
  - JTAG for board level testing
- PCI interfaces
  - Two independent bridges with parking
  - PCI Revision 2.1 compliant
  - 3.3V signal interface
- Synchronous DRAM (SDRAM) interface operating at 100 or 133MHz
  - Support for PC100 and PC133 SDRAM and Registered DIMMs
  - Two-way interleaved operation with ECC using external multiplexer
  - Up to 3.5GB addressing space using 16-, 64-,128-, 256-, 512- or 1024-MB DIMMs
- PPC60x Bus interface
  - Up to 133MHz bus
  - One to four processors
  - Up to 6 outstanding transaction requests
  - Little Endian mode available
- System I/O interface
  - 2-MB Flash Boot ROM
  - 256-MB Extended Flash
- DMA controller
  - Single channel
  - System memory-to-PCI transfers only
  - Store-gather for enhanced performance

Description

The CPC710 IBM PCI Bridge and Memory Controller is a highly integrated host bridge device that interfaces PowerPC 60x buses to SDRAM-based system memory and also provides two PCI interfaces. It supports up to four processors with pipelining for up to six outstanding transaction requests.

The memory controller supports SDRAM, allowing the memory to burst data on most bus cycles at 100MHz or 133MHz.

For system designs requiring high I/O bandwidth, there are two PCI host bus bridges. One bridge supports a standard 32-bit, 33MHz PCI bus, while the other supports 64 bits at up to 66MHz for graphics and high speed communications.

An internal DMA controller allows high speed data transfer between Memory and I/O. Store-gathering enhances the CPU-to-I/O performance.

Technology: IBM CMOS SA-12E, 0.25 µm

Package: 35mm, 728-ball flip chip-plastic ball grid array (FC-PBGA)

Power (estimated): Typical 2.1W, Maximum 2.6W

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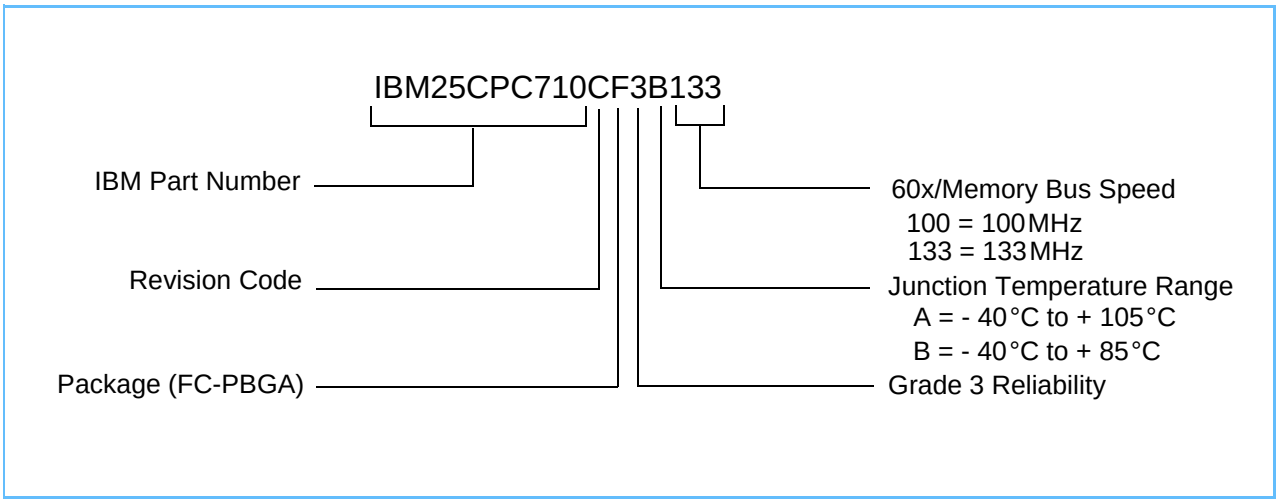
Ordering Information

Product Name	Order Part Number	Processor Bus Frequency	Package	Revision Level
CPC710-100	IBM25CPC710CF3A100	100 MHz	35 mm, 728-ball FC-PBGA	C
CPC710-133	IBM25CPC710CF3B133	133 MHz	35 mm, 728-ball FC-PBGA	C

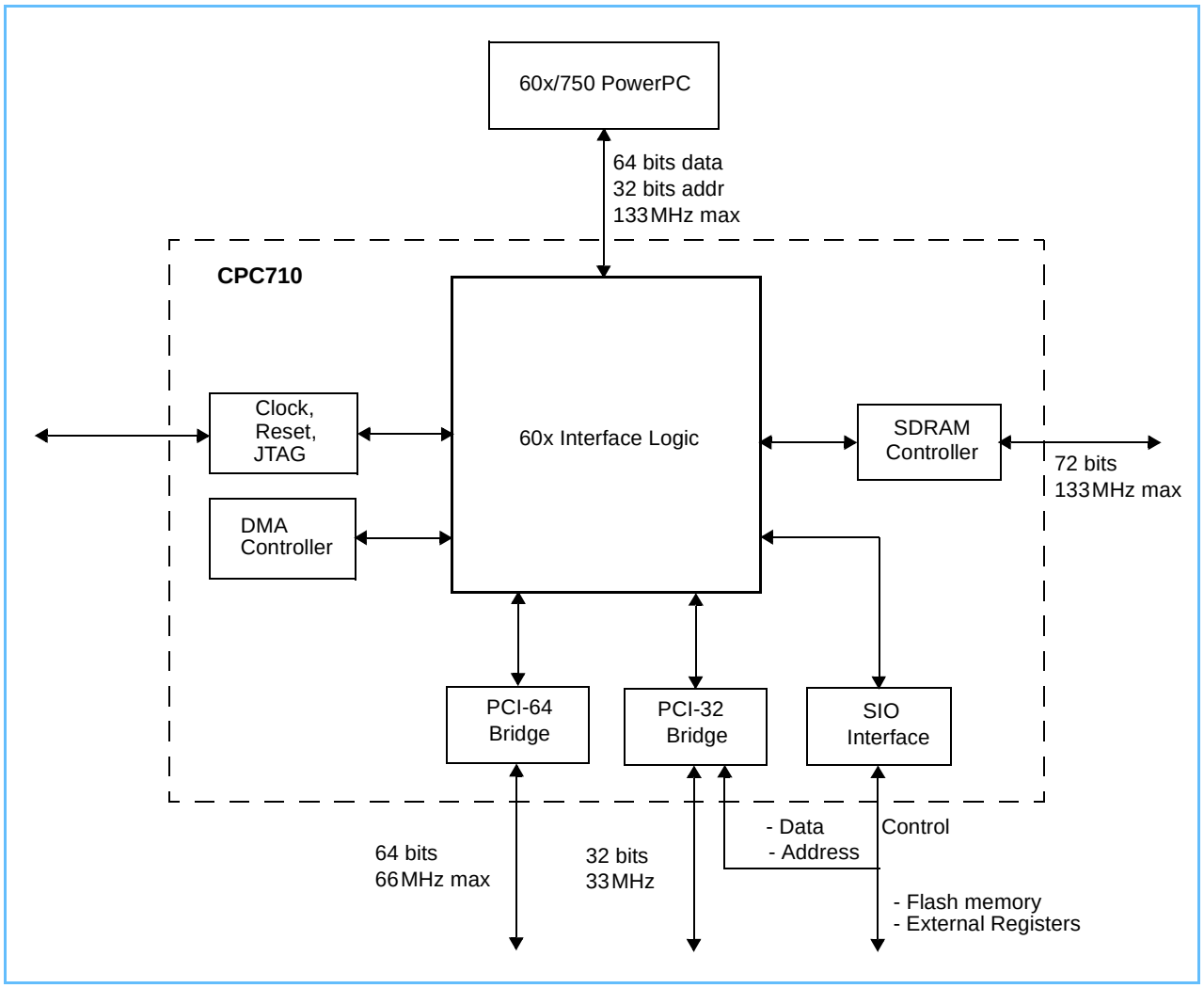
This section provides the part numbering nomenclature for the CPC710. For availability, contact your local IBM sales office.

Each part number contains a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

IBM Part Number Key



CPC710 PCI Bridge and Memory Controller Functional Block Diagram



CPC710 PCI Bridge and Memory Controller Data Sheet

Features

- Up to 133 MHz PowerPC 60x 64-bit bus
- 2.5 V 60x PowerPC bus
- Supports 100- and 133-MHz SDRAM including PC100 and PC133
- Up to 2 MB Flash Boot ROM support
- 32-bit 33 MHz/64-bit 33-66 MHz asynchronous dual PCI buses
- Bidirectional interface to two external 32-bit registers
- PreP and CHRP compliant design
- One-channel chained DMA controller
- Up to 256-MB Extended Flash support
- 32-bit PCI bus has 3.3 V, 5 V-tolerant I/O
- 64-bit PCI bus has 3.3 V I/O
- Power dissipation estimate of 2.1 W at 133 MHz
- PLL to reduce on-chip system clock skew
- JTAG controller

60x Bus Interface

- Supports 740L/750L, 750CX/Cxe, or 74xx PowerPC
- Up 133-MHz external bus operation
- Supports four processors
- 64-bit data bus with 8 bits of parity
- 32-bit address bus with 4 bits of parity
- Dual 32-byte store back buffers
- High bandwidth, 4-way arbiter
- Little Endian mode PowerPC
- Supports SYNC/EIEIO ordering operations
- Supports L2 cache or bus slaves with external decode

SDRAM Memory Controller

The CPC710 Memory Controller core provides a low latency access path to SDRAM memory. A variety of system memory configurations are supported.

Features include:

- Support for 100- and 133-MHz SDRAM including PC100 and PC133 and Registered DIMMs
- Supports 16-, 64-, 128-, and 256-Mbit SDRAMs
- Up to 3.5 GB addressing range using 16-, 64-,128-, 256-, 512- or 1024-MB DIMMs
- 2-way interleaved SDRAM with ECC (external MUX to reduce pin count)
- Programmable timing parameters
- Up to 6 dual bank DIMMs
- Up to 4 banks supported for Multibanking
- SDRAM Access command queue with look ahead override option for CPU, PCIs, and DMA
- Access based on 32-byte cache line reload
- Three separate dual 32-byte load buffers (PCI-32, PCI-64, 60x)

PCI Bridges

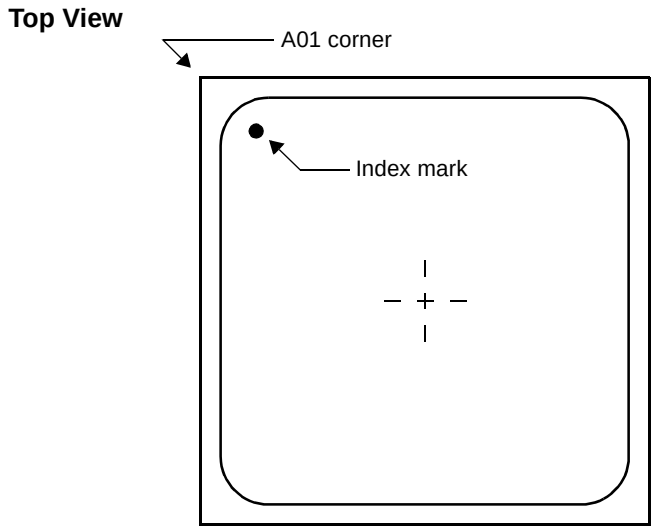
- Two independent PCI bus bridges with parking
- PCI revision 2.1 compliant
- PCI-32 with 3.3V, 5V tolerant interface
- PCI-64 with 3.3V interface
- Buses run asynchronously to processor and memory controller
- External arbitration available for both buses
- Dual 32-byte buffers in each PCI bridge
- Round-robin PCI arbiter
- Coherency for memory access through DMA controller or through PCI master

JTAG

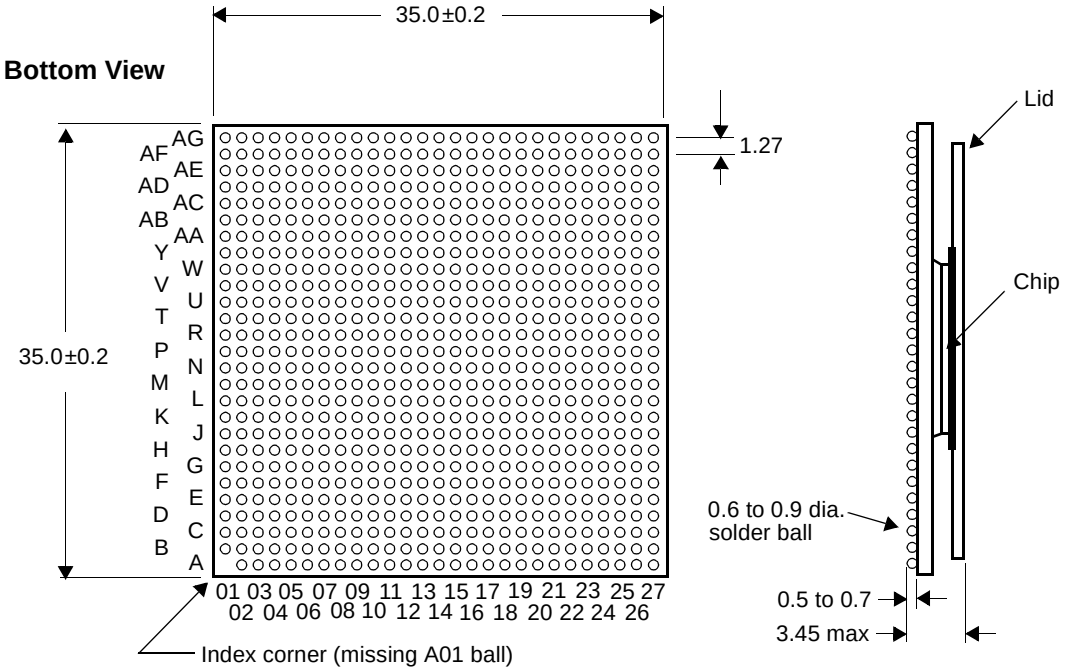
- IEEE 1149.1 Test Access Port (TAP)
- IBM RISCWatch Debugger support

CPC710 PCI Bridge and Memory Controller Data Sheet

35mm, 728-Ball FC-PBGA Package



Note: All dimensions are in mm.



Signal Lists

The following table lists all the external signals in alphabetical order and shows the ball number on which the signal appears. Multiplexed signals are shown with the default signal (following reset) *not* in brackets and the alternate signal in brackets. Multiplexed signals appear alphabetically multiple times in the list—once for each signal name on the ball. The page number listed gives the page in “Signal Functional Description” on page 36 where the signals in the indicated interface group begin.

Signals Listed Alphabetically (Part 1 of 20)

Signal Name	Ball	Interface Group	Page
AV_{DD}	D27	Power	44
BS0	J10	SDRAM	39
BS1	J09		
$\overline{\text{CE0\_TEST}}$	N23	System	43
$\overline{\text{CHKSTOP}}$	J26	60x	36
$\overline{\text{DLK}}$	G06	60x	36
$\overline{\text{FLASH\_CE}}$	G27	SIO	42
$\overline{\text{FLASH\_OE}}$	H27		
$\overline{\text{FLASH\_WE}}$	H26		

Signals Listed Alphabetically (Part 2 of 20)

Signal Name	Ball	Interface Group	Page
GND	A03		
GND	A11		
GND	A17		
GND	A25		
GND	C01		
GND	C05		
GND	C09		
GND	C13		
GND	C15		
GND	C19		
GND	C23		
GND	C27		
GND	E03		
GND	E07		
GND	E11		
GND	E17	Power	44
GND	E21		
GND	E25		
GND	F14		
GND	G05		
GND	G09		
GND	G19		
GND	G23		
GND	H12		
GND	H16		
GND	J03		
GND	J07		
GND	J21		
GND	J25		
GND	L01		
GND	L05		

Signals Listed Alphabetically (Part 3 of 20)

Signal Name	Ball	Interface Group	Page
GND	L23	Power	44
GND	L27		
GND	M08		
GND	M20		
GND	N03		
GND	N13		
GND	N15		
GND	N25		
GND	P06		
GND	P14		
GND	P22		
GND	R03		
GND	R13		
GND	R15		
GND	R25		
GND	T08		
GND	T20		
GND	U01		
GND	U05		
GND	U23		
GND	U27		
GND	W03		
GND	W07		
GND	W21		
GND	W25		
GND	Y12		
GND	Y16		
GND	AA05		
GND	AA09		
GND	AA19		
GND	AA23		
GND	AB14		
GND	AC03		
GND	AC07		
GND	AC11		
GND	AC17		
GND	AC21		
GND	AC25		
GND	AE01		
GND	AE05		
GND	AE09		
GND	AE13		
GND	AE15		

Signals Listed Alphabetically (Part 4 of 20)

Signal Name	Ball	Interface Group	Page
GND	AE19	Power	44
GND	AE23		
GND	AE27		
GND	AG03		
GND	AG11		
GND	AG17		
GND	AG25		
GPIO0	H25	60x	36
GPIO1	F25		
GPIO2	D25		
G_ACK64	R06	PCI-64	41
G_ADH00	AD02	PCI-64	41
G_ADH01	AE02		
G_ADH02	AC02		
G_ADH03	AB01		
G_ADH04	AA02		
G_ADH05	AA01		
G_ADH06	Y02		
G_ADH07	Y01		
G_ADH08	W02		
G_ADH09	V03		
G_ADH10	V02		
G_ADH11	V01		
G_ADH12	U02		
G_ADH13	T04		
G_ADH14	T03		
G_ADH15	T02		
G_ADH16	T01		
G_ADH17	R04		
G_ADH18	R02		
G_ADH19	R01		
G_ADH20	P03		
G_ADH21	P02		
G_ADH22	N07		
G_ADH23	N06		
G_ADH24	N05		
G_ADH25	N04		
G_ADH26	N02		
G_ADH27	N01		
G_ADH28	M04		
G_ADH29	M03		
G_ADH30	M02		
G_ADH31	M01		

Signals Listed Alphabetically (Part 5 of 20)

Signal Name	Ball	Interface Group	Page
G_ADL00	M09	PCI-64	41
G_ADL01	M07		
G_ADL02	M06		
G_ADL03	M05		
G_ADL04	L09		
G_ADL05	L08		
G_ADL06	L06		
G_ADL07	L04		
G_ADL08	L02		
G_ADL09	K07		
G_ADL10	K06		
G_ADL11	K05		
G_ADL12	K04		
G_ADL13	K03		
G_ADL14	K02		
G_ADL15	K01		
G_ADL16	J06		
G_ADL17	J04		
G_ADL18	J02		
G_ADL19	H05		
G_ADL20	H04		
G_ADL21	H03		
G_ADL22	H02		
G_ADL23	H01		
G_ADL24	G04		
G_ADL25	G02		
G_ADL26	G01		
G_ADL27	F03		
G_ADL28	F02		
G_ADL29	F01		
G_ADL30	E02		
G_ADL31	D01		
G_ARB[SDDQM]	H06	PCI-64	41
$\overline{\text{G\_CBE0}}$	V09	PCI-64	41
$\overline{\text{G\_CBE1}}$	U09		
$\overline{\text{G\_CBE2}}$	U08		
$\overline{\text{G\_CBE3}}$	R07		
$\overline{\text{G\_CBE4}}$	R05		
$\overline{\text{G\_CBE5}}$	P09		
$\overline{\text{G\_CBE6}}$	P07		
$\overline{\text{G\_CBE7}}$	P05		
$\overline{\text{G\_DEVSEL}}$	AB04	PCI-64	41
$\overline{\text{G\_FRAME}}$	B01	PCI-64	41

Signals Listed Alphabetically (Part 6 of 20)

Signal Name	Ball	Interface Group	Page
G_GNT0	AA04	PCI-64	41
G_GNT1	Y05		
G_GNT2	Y04		
G_GNT3	Y03		
G_GNT4	W04		
G_GNT5[P_GNT4]	V05		
G_GNT6[P_GNT5]	V04		
G_GNT7[P_GNT6]	U04		
G_IDSEL	AD03	PCI-64	41
G_INTA	T09	PCI-64	41
G_INTB	T07		
G_INTC	T06		
G_INTD	T05		
G_IRDY	K09	PCI-64	41
G_LOCK	AC04	PCI-64	41
G_PAR	R08	PCI-64	41
G_PAR64	AB05	PCI-64	41
G_PERR	F04	PCI-64	41
G_REQ0	U06	PCI-64	41
G_REQ1	V06		
G_REQ2	V07		
G_REQ3	W06		
G_REQ4	Y06		
G_REQ5[P_REQ4]	Y07		
G_REQ6[P_REQ5]	Y09		
G_REQ7[P_REQ6]	AA06		
G_REQ64	AB03	PCI-64	41
G_RESETOUT	AD01	PCI-64	41
G_RST	D02	PCI-64	41
G_SERR	AB02	PCI-64	41
G_STOP	N08	PCI-64	41
G_TRDY	J08	PCI-64	41
IT1	E22	60x	36
IT2	E24		
MADDR0_EVEN	C18	SDRAM	39
MADDR0_ODD	D17		

Signals Listed Alphabetically (Part 7 of 20)

Signal Name	Ball	Interface Group	Page
MADDR01	D18	SDRAM	39
MADDR02	E18		
MADDR03	E20		
MADDR04	F17		
MADDR05	F18		
MADDR06	F19		
MADDR07	F20		
MADDR08	F21		
MADDR09	F22		
MADDR10	G18		
MADDR11	G20		
MADDR12	H17		
MADDR13	H19		
MDATA00	A04	SDRAM	39
MDATA01	A06		
MDATA02	A07		
MDATA03	A08		
MDATA04	A10		
MDATA05	A12		
MDATA06	A13		
MDATA07	A15		
MDATA08	A16		
MDATA09	B04		
MDATA10	B05		
MDATA11	B06		
MDATA12	B07		
MDATA13	B08		
MDATA14	B09		
MDATA15	B10		
MDATA16	B11		
MDATA17	B12		
MDATA18	B13		
MDATA19	B14		
MDATA20	B15		
MDATA21	B16		
MDATA22	B17		
MDATA23	C04		
MDATA24	C06		
MDATA25	C08		
MDATA26	C10		
MDATA27	C12		
MDATA28	C14		
MDATA29	C16		
MDATA30	D05		
MDATA31	D06		

Signals Listed Alphabetically (Part 8 of 20)

Signal Name	Ball	Interface Group	Page
MDATA32	D07	SDRAM	39
MDATA33	D08		
MDATA34	D09		
MDATA35	D10		
MDATA36	D11		
MDATA37	D12		
MDATA38	D13		
MDATA39	D15		
MDATA40	D16		
MDATA41	E06		
MDATA42	E08		
MDATA43	E10		
MDATA44	E12		
MDATA45	E13		
MDATA46	E14		
MDATA47	E15		
MDATA48	E16		
MDATA49	F07		
MDATA50	F08		
MDATA51	F09		
MDATA52	F10		
MDATA53	F11		
MDATA54	F12		
MDATA55	F13		
MDATA56	F15		
MDATA57	F16		
MDATA58	G08		
MDATA59	G10		
MDATA60	G12		
MDATA61	G13		
MDATA62	G14		
MDATA63	G15		
MDATA64	G16	SDRAM	39
MDATA65	H11		
MDATA66	H13		
MDATA67	H15		
MDATA68	J11		
MDATA69	J12		
MDATA70	J14		
MDATA71	J16		
$\overline{\text{MUX\_CLKENA1}}$	F06	SDRAM	39
$\overline{\text{MUX\_CLKENA2}}$	H07		
$\overline{\text{MUX\_CLKEN1B}}$	J17	SDRAM	39
$\overline{\text{MUX\_CLKEN2B}}$	J18		

Signals Listed Alphabetically (Part 9 of 20)

Signal Name	Ball	Interface Group	Page
$\overline{\text{MUX\_OEA}}$	B03	SDRAM	39
$\overline{\text{MUX\_OEB}}$	C02		
$\overline{\text{MUX\_SEL}}$	D04	SDRAM	39
$\overline{\text{NODLK}}$	A02	60x	36
No pin	A01		
OV_{DD}	E27	Power	
OV_{DD}	G25		
OV_{DD}	J23		
OV_{DD}	L21		
OV_{DD}	P20		
OV_{DD}	P27		
OV_{DD}	U21		
OV_{DD}	W23		
OV_{DD}	AA25		
OV_{DD}	AC27		
OV_{DD}	Y14		
OV_{DD}	AA11		
OV_{DD}	AA17		
OV_{DD}	AC09		
OV_{DD}	AC19		
OV_{DD}	AE07		
OV_{DD}	AE21		
OV_{DD}	AG05		
OV_{DD}	AG14		
OV_{DD}	AG23		
OV_{DD}	E01		
OV_{DD}	G03		
OV_{DD}	J05		
OV_{DD}	L07		

Signals Listed Alphabetically (Part 10 of 20)

Signal Name	Ball	Interface Group	Page
OV_{DD}	P01	SDRAM	39
OV_{DD}	P08		
OV_{DD}	U07		
OV_{DD}	W05		
OV_{DD}	AA03		
OV_{DD}	AC01		
OV_{DD}	A05		
OV_{DD}	A14		
OV_{DD}	A23		
OV_{DD}	C07		
OV_{DD}	C21		
OV_{DD}	E09		
OV_{DD}	E19		
OV_{DD}	G11		
OV_{DD}	G17		
OV_{DD}	H14		
PCG_CLK	W08	PCI-64	41
PCI_CLK	AB27	PCI-32	40
PLL_LOCK	P23	System	43
PLL_RANGE0	K27	System	43
PLL_RANGE1	F23		
$\overline{\text{PLL\_RESET}}$	A27	System	43
PLL_TUNE0	B25	System	43
PLL_TUNE1	H20		
PLL_TUNE2	T23		
PLL_TUNE3	R27		
PLL_TUNE4	R23		
PLL_TUNE5	J20		
POWERGOOD	AG06	System	43
$\overline{\text{PRES\_OE0}}$	B26	SIO	42
$\overline{\text{PRES\_OE1}}$	C26		

Signals Listed Alphabetically (Part 11 of 20)

Signal Name	Ball	Interface Group	Page
P_ADL00	P26	PCI-32	40
P_ADL01	N26		
P_ADL02	M26		
P_ADL03	L26		
P_ADL04	K26		
P_ADL05	K25		
P_ADL06	M25		
P_ADL07	P25		
P_ADL08	N24		
P_ADL09	M24		
P_ADL10	L24		
P_ADL11	K24		
P_ADL12	J24		
P_ADL13	K23		
P_ADL14	M23		
P_ADL15	N22		
P_ADL16	M22		
P_ADL17	L22		
P_ADL18	K22		
P_ADL19	J22		
P_ADL20	H22		
P_ADL21	G22		
P_ADL22	K21		
P_ADL23	M21		
P_ADL24	N21		
P_ADL25	P21		
P_ADL26	N20		
P_ADL27	L20		
P_ADL28	K19		
P_ADL29	L19		
P_ADL30	M19		
P_ADL31	P19		
P_CBE0	R24	PCI-32	40
P_CBE1	T24		
P_CBE2	T25		
P_CBE3	T26		
P_DEVSEL	R22	PCI-32	40
P_FRAME	T22	PCI-32	40
P_GNT0	AA27	PCI-32	40
P_GNT1	Y27		
P_GNT2	W26		
P_GNT3	T27		
[P_GNT4]G_GNT5	V05		
[P_GNT5]G_GNT6	V04		
[P_GNT6]G_GNT7	U04		

Signals Listed Alphabetically (Part 12 of 20)

Signal Name	Ball	Interface Group	Page
P_LOCK	H21	PCI-32	40
P_MEMACK	G24	PCI-32	40
P_MEMREQ	H24	PCI-32	40
P_PAR	H23	PCI-32	40
P_PERR	U26	PCI-32	40
P_REQ0	V27	PCI-32	40
P_REQ1	V26		
P_REQ2	V25		
P_REQ3	V24		
[P_REQ4]G_REQ5	Y07		
[P_REQ5]G_REQ6	Y09		
[P_REQ6]G_REQ7	AA06		
P_RST	N27	PCI-32	40
P_SERR	V23	PCI-32	40
P_STOP	U24	PCI-32	40
P_TRDY	M27	PCI-32	40
Reserved	J13	Other pins	
Reserved	J15		
Reserved	J19		
Reserved	K10		
Reserved	K11		
Reserved	K12		
Reserved	K13		
Reserved	K14		
Reserved	K15		
Reserved	K16		
Reserved	K17		
Reserved	K18		
Reserved	L10		
Reserved	L11		
Reserved	L12		
Reserved	L13		
Reserved	L14		
Reserved	L15		
Reserved	L16		
Reserved	L17		

Signals Listed Alphabetically (Part 13 of 20)

Signal Name	Ball	Interface Group	Page
Reserved	L18		
Reserved	M10		
Reserved	M11		
Reserved	M12		
Reserved	M13		
Reserved	M14		
Reserved	M15		
Reserved	M16		
Reserved	M17		
Reserved	M18		
Reserved	N09		
Reserved	N10		
Reserved	N11		
Reserved	N12		
Reserved	N16		
Reserved	N17		
Reserved	N18		
Reserved	N19		
Reserved	P10		
Reserved	P11		
Reserved	P12		
Reserved	P16		
Reserved	P17	Other pins	
Reserved	P18		
Reserved	R09		
Reserved	R10		
Reserved	R11		
Reserved	R12		
Reserved	R16		
Reserved	R17		
Reserved	R18		
Reserved	R19		
Reserved	T10		
Reserved	T11		
Reserved	T12		
Reserved	T13		
Reserved	T14		
Reserved	T15		
Reserved	T16		
Reserved	T17		
Reserved	T18		
Reserved	U10		
Reserved	U11		
Reserved	U12		
Reserved	U13		

Signals Listed Alphabetically (Part 14 of 20)

Signal Name	Ball	Interface Group	Page
Reserved	U14	Other pins	
Reserved	U15		
Reserved	U16		
Reserved	U17		
Reserved	U18		
Reserved	V10		
Reserved	V11		
Reserved	V12		
Reserved	V13		
Reserved	V14		
Reserved	V15		
Reserved	V16		
Reserved	V17		
Reserved	V18		
Reserved	W09		
Reserved	W13		
Reserved	W15		
Reserved	W19		
$\overline{\text{SDCAS0}}$	E04	SDRAM	39
$\overline{\text{SDCAS1}}$[SDDQM]	F05		
SDCKE0	A22	SDRAM	39
SDCKE1	A24		
SDCKE2	A26		
SDCKE3	B22		
SDCKE4	B23		
SDCKE5	B24		
SDCKE6	C22		
SDCKE7	C24		
SDCKE8	D22		
SDCKE9	D24		
$\overline{\text{SDCS00}}$	D23	SDRAM	39
$\overline{\text{SDCS01}}$	D21		
$\overline{\text{SDCS02}}$	D20		
$\overline{\text{SDCS03}}$	D19		
$\overline{\text{SDCS04}}$	C20		
$\overline{\text{SDCS05}}$	B21		
$\overline{\text{SDCS06}}$	B20		
$\overline{\text{SDCS07}}$	B19		
$\overline{\text{SDCS08}}$	B18		
$\overline{\text{SDCS09}}$	A21		
$\overline{\text{SDCS10}}$	A20		
$\overline{\text{SDCS11}}$	A18		
[SDDQM]G_ARB [SDDQM]$\overline{\text{SDCAS1}}$ [SDDQM]$\overline{\text{SDRAS1}}$ [SDDQM]$\overline{\text{WE1}}$	G06 F05 D03 H09	SDRAM	39

Signals Listed Alphabetically (Part 15 of 20)

Signal Name	Ball	Interface Group	Page
SDRAS0	B02	SDRAM	39
SDRAS1[SDDQM]	D03		
SYS_AACK	W10	60x	36
SYS_ADDR00	W24	60x	36
SYS_ADDR01	Y22		
SYS_ADDR02	Y23		
SYS_ADDR03	Y24		
SYS_ADDR04	AA22		
SYS_ADDR05	AA24		
SYS_ADDR06	AB22		
SYS_ADDR07	AB23		
SYS_ADDR08	AB24		
SYS_ADDR09	AB25		
SYS_ADDR10	AB26		
SYS_ADDR11	AC22		
SYS_ADDR12	AC24		
SYS_ADDR13	AC26		
SYS_ADDR14	AD22		
SYS_ADDR15	AD23		
SYS_ADDR16	AD24		
SYS_ADDR17	AD25		
SYS_ADDR18	AD26		
SYS_ADDR19	AD27		
SYS_ADDR20	AE22		
SYS_ADDR21	AE24		
SYS_ADDR22	AE26		
SYS_ADDR23	AF21		
SYS_ADDR24	AF22		
SYS_ADDR25	AF23		
SYS_ADDR26	AF24		
SYS_ADDR27	AF25		
SYS_ADDR28	AF26		
SYS_ADDR29	AF27		
SYS_ADDR30	AG20		
SYS_ADDR31	AG21		
SYS_ADDRP0	Y21	60x	36
SYS_ADDRP1	W22		
SYS_ADDRP2	V22		
SYS_ADDRP3	V21		
SYS_ARTRY	W11	60x	36
SYS_BG0	AF01	60x	36
SYS_BG1	Y20		
SYS_BG2	Y25		
SYS_BG3	AA26		

Signals Listed Alphabetically (Part 16 of 20)

Signal Name	Ball	Interface Group	Page
SYS_BR0	V19	60x	36
SYS_BR1	U19		
SYS_BR2	T19		
SYS_BR3	U20		
SYS_CLK	B27	System	43
SYS_DATA00	Y08	System	43
SYS_DATA01	AA08		
SYS_DATA02	AA10		
SYS_DATA03	AA12		
SYS_DATA04	AA13		
SYS_DATA05	AA14		
SYS_DATA06	AA15		
SYS_DATA07	AA16		
SYS_DATA08	AB08		
SYS_DATA09	AB09		
SYS_DATA10	AB10		
SYS_DATA11	AB11		
SYS_DATA12	AB12		
SYS_DATA13	AB13		
SYS_DATA14	AB15		
SYS_DATA15	AB16		
SYS_DATA16	AB17		
SYS_DATA17	AB18		
SYS_DATA18	AB19		
SYS_DATA19	AC08		
SYS_DATA20	AC10		
SYS_DATA21	AC12		
SYS_DATA22	AC13		
SYS_DATA23	AC14		
SYS_DATA24	AC15		
SYS_DATA25	AC16		
SYS_DATA26	AC18		
SYS_DATA27	AD07		
SYS_DATA28	AD08		
SYS_DATA29	AD09		
SYS_DATA30	AD10		
SYS_DATA31	AD11		

Signals Listed Alphabetically (Part 17 of 20)

Signal Name	Ball	Interface Group	Page
SYS_DATA32	AD12	System	43
SYS_DATA33	AD13		
SYS_DATA34	AD15		
SYS_DATA35	AD16		
SYS_DATA36	AD17		
SYS_DATA37	AD18		
SYS_DATA38	AE08		
SYS_DATA39	AE10		
SYS_DATA40	AE12		
SYS_DATA41	AE14		
SYS_DATA42	AE16		
SYS_DATA43	AE18		
SYS_DATA44	AF07		
SYS_DATA45	AF08		
SYS_DATA46	AF09		
SYS_DATA47	AF10		
SYS_DATA48	AF11		
SYS_DATA49	AF12		
SYS_DATA50	AF13		
SYS_DATA51	AF14		
SYS_DATA52	AF15		
SYS_DATA53	AF16		
SYS_DATA54	AF17		
SYS_DATA55	AF18		
SYS_DATA56	AG07		
SYS_DATA57	AG08		
SYS_DATA58	AG10		
SYS_DATA59	AG12		
SYS_DATA60	AG13		
SYS_DATA61	AG15		
SYS_DATA62	AG16		
SYS_DATA63	AG18		
SYS_DATAP0	AG04	System	43
SYS_DATAP1	AF03		
SYS_DATAP2	AF04		
SYS_DATAP3	AF06		
SYS_DATAP4	AE04		
SYS_DATAP5	AD05		
SYS_DATAP6	AD06		
SYS_DATAP7	AB07		
$\overline{\text{SYS\_DBG0}}$	T21	System	43
$\overline{\text{SYS\_DBG1}}$	W20		
$\overline{\text{SYS\_DBG2}}$	R21		
$\overline{\text{SYS\_DBG3}}$	R20		
$\overline{\text{SYS\_GBL}}$	Y11	System	43

Signals Listed Alphabetically (Part 18 of 20)

Signal Name	Ball	Interface Group	Page
SYS_HRESET0	AD20	System	43
SYS_HRESET1	AC20		
SYS_HRESET2	AE20		
SYS_HRESET3	AD19		
SYS_L2_HIT	AF02	System	43
SYS_MCP0	W14	System	43
SYS_MCP1	Y15		
SYS_MCP2	W12		
SYS_MCP3	Y13		
SYS_SHD	AF05	System	43
SYS_SRESET0	AD21	System	43
SYS_SRESET1	AB21		
SYS_SRESET2	AB20		
SYS_SRESET3	AA20		
SYS_TA	AG01	System	43
SYS_TA_HIT	AC06	System	43
SYS_TBE	AD04	System	43
SYS_TBST	AE06	System	43
SYS_TEA	AB06	System	43
SYS_TS	Y26	System	43
SYS_TSIZ0	AF19	System	43
SYS_TSIZ1	AF20		
SYS_TSIZ2	AG02		
SYS_TT0	AA18	System	43
SYS_TT1	W18		
SYS_TT2	W17		
SYS_TT3	Y17		
SYS_TT4	W16		
TCK	Y19	JTAG	48
TDI	E26		
TDO	F27		
TMS	R26		
TRST	D26		
V_{DD}	A09	Power	
V_{DD}	A19		
V_{DD}	C03		
V_{DD}	C11		
V_{DD}	C17		

Signals Listed Alphabetically (Part 19 of 20)

Signal Name	Ball	Interface Group	Page
V_{DD}	C25		
V_{DD}	D14		
V_{DD}	E05		
V_{DD}	E23		
V_{DD}	G07		
V_{DD}	G21		
V_{DD}	H10		
V_{DD}	H18		
V_{DD}	J01		
V_{DD}	J27		
V_{DD}	K08		
V_{DD}	K20		
V_{DD}	L03		
V_{DD}	L25		
V_{DD}	N14		
V_{DD}	P04		
V_{DD}	P13		
V_{DD}	P15		
V_{DD}	P24		
V_{DD}	R14	Power	
V_{DD}	U03		
V_{DD}	U25		
V_{DD}	V08		
V_{DD}	V20		
V_{DD}	W01		
V_{DD}	W27		
V_{DD}	Y10		
V_{DD}	Y18		
V_{DD}	AA07		
V_{DD}	AA21		
V_{DD}	AC05		
V_{DD}	AC23		
V_{DD}	AD14		
V_{DD}	AE03		
V_{DD}	AE11		
V_{DD}	AE17		
V_{DD}	AE25		
V_{DD}	AG09		
V_{DD}	AG19		

Signals Listed Alphabetically (Part 20 of 20)

Signal Name	Ball	Interface Group	Page
$\overline{WE0}$	H08	SDRAM	39
$\overline{WE1}$[SDDQM]	H09		
XADR_LAT	G26	SIO	42
XCVR_RD	F26		

Signals Listed by Ball Assignment (Part 1 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A01	No pin	B01	$\overline{\text{G\_FRAME}}$	C01	GND	D01	G_ADL31
A02	$\overline{\text{NODLK}}$	B02	$\overline{\text{SDRAS0}}$	C02	$\overline{\text{MUX\_OEB}}$	D02	$\overline{\text{G\_RST}}$
A03	GND	B03	$\overline{\text{MUX\_OEA}}$	C03	V_{DD}	D03	$\overline{\text{SDRAS1}}$
A04	MDATA00	B04	MDATA09	C04	MDATA23	D04	$\overline{\text{MUX\_SEL}}$
A05	OV_{DD}	B05	MDATA10	C05	GND	D05	MDATA30
A06	MDATA01	B06	MDATA11	C06	MDATA24	D06	MDATA31
A07	MDATA02	B07	MDATA12	C07	OV_{DD}	D07	MDATA32
A08	MDATA03	B08	MDATA13	C08	MDATA25	D08	MDATA33
A09	V_{DD}	B09	MDATA14	C09	GND	D09	MDATA34
A10	MDATA04	B10	MDATA15	C10	MDATA26	D10	MDATA35
A11	GND	B11	MDATA16	C11	V_{DD}	D11	MDATA36
A12	MDATA05	B12	MDATA17	C12	MDATA27	D12	MDATA37
A13	MDATA06	B13	MDATA18	C13	GND	D13	MDATA38
A14	OV_{DD}	B14	MDATA19	C14	MDATA28	D14	V_{DD}
A15	MDATA07	B15	MDATA20	C15	GND	D15	MDATA39
A16	MDATA08	B16	MDATA21	C16	MDATA29	D16	MDATA40
A17	GND	B17	MDATA22	C17	V_{DD}	D17	MADDR0_ODD
A18	$\overline{\text{SDCS11}}$	B18	$\overline{\text{SDCS08}}$	C18	MADDR0_EVEN	D18	MADDR01
A19	V_{DD}	B19	$\overline{\text{SDCS07}}$	C19	GND	D19	$\overline{\text{SDCS03}}$
A20	$\overline{\text{SDCS10}}$	B20	$\overline{\text{SDCS06}}$	C20	$\overline{\text{SDCS04}}$	D20	$\overline{\text{SDCS02}}$
A21	$\overline{\text{SDCS09}}$	B21	$\overline{\text{SDCS05}}$	C21	OV_{DD}	D21	$\overline{\text{SDCS01}}$
A22	SDCKE0	B22	SDCKE3	C22	SDCKE6	D22	SDCKE8
A23	OV_{DD}	B23	SDCKE4	C23	GND	D23	$\overline{\text{SDCS00}}$
A24	SDCKE1	B24	SDCKE5	C24	SDCKE7	D24	SDCKE9
A25	GND	B25	PLL_TUNE0	C25	V_{DD}	D25	GPIO2
A26	SDCKE2	B26	$\overline{\text{PRES\_OE0}}$	C26	$\overline{\text{PRES\_OE1}}$	D26	TRST
A27	$\overline{\text{PLL\_RESET}}$	B27	SYS_CLK	C27	GND	D27	AV_{DD}

Signals Listed by Ball Assignment (Part 2 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
E01	OV_{DD}	F01	G_ADL29	G01	G_ADL26	H01	G_ADL23
E02	G_ADL30	F02	G_ADL28	G02	G_ADL25	H02	G_ADL22
E03	GND	F03	G_ADL27	G03	OV_{DD}	H03	G_ADL21
E04	$\overline{SDCAS0}$	F04	$\overline{G\_PERR}$	G04	G_ADL24	H04	G_ADL20
E05	V_{DD}	F05	$\overline{SDCAS1}$	G05	GND	H05	G_ADL19
E06	MDATA41	F06	$\overline{MUX\_CLKENA1}$	G06	$\overline{DLK}$	H06	G_ARB
E07	GND	F07	MDATA49	G07	V_{DD}	H07	$\overline{MUX\_CLKENA2}$
E08	MDATA42	F08	MDATA50	G08	MDATA58	H08	$\overline{WE0}$
E09	OV_{DD}	F09	MDATA51	G09	GND	H09	$\overline{WE1}$
E10	MDATA43	F10	MDATA52	G10	MDATA59	H10	V_{DD}
E11	GND	F11	MDATA53	G11	OV_{DD}	H11	MDATA65
E12	MDATA44	F12	MDATA54	G12	MDATA60	H12	GND
E13	MDATA45	F13	MDATA55	G13	MDATA61	H13	MDATA66
E14	MDATA46	F14	GND	G14	MDATA62	H14	OV_{DD}
E15	MDATA47	F15	MDATA56	G15	MDATA63	H15	MDATA67
E16	MDATA48	F16	MDATA57	G16	MDATA64	H16	GND
E17	GND	F17	MADDR04	G17	OV_{DD}	H17	MADDR12
E18	MADDR02	F18	MADDR05	G18	MADDR10	H18	V_{DD}
E19	OV_{DD}	F19	MADDR06	G19	GND	H19	MADDR13
E20	MADDR03	F20	MADDR07	G20	MADDR11	H20	PLL_TUNE1
E21	GND	F21	MADDR08	G21	V_{DD}	H21	$\overline{P\_LOCK}$
E22	$\overline{IT1}$	F22	MADDR09	G22	P_ADL21	H22	P_ADL20
E23	V_{DD}	F23	PLL_RANGE1	G23	GND	H23	P_PAR
E24	$\overline{IT2}$	F24	$\overline{P\_IRDY}$	G24	$\overline{P\_MEMACK}$	H24	$\overline{P\_MEMREQ}$
E25	GND	F25	GPIO1	G25	OV_{DD}	H25	GPIO0
E26	TDI	F26	XCVR_RD	G26	XADR_LAT	H26	$\overline{FLASH\_WE}$
E27	OV_{DD}	F27	TDO	G27	$\overline{FLASH\_CE}$	H27	$\overline{FLASH\_OE}$

Signals Listed by Ball Assignment (Part 3 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
J01	V_{DD}	K01	G_ADL15	L01	GND	M01	G_ADH31
J02	G_ADL18	K02	G_ADL14	L02	G_ADL08	M02	G_ADH30
J03	GND	K03	G_ADL13	L03	V_{DD}	M03	G_ADH29
J04	G_ADL17	K04	G_ADL12	L04	G_ADL07	M04	G_ADH28
J05	OV_{DD}	K05	G_ADL11	L05	GND	M05	G_ADL03
J06	G_ADL16	K06	G_ADL10	L06	G_ADL06	M06	G_ADL02
J07	GND	K07	G_ADL09	L07	OV_{DD}	M07	G_ADL01
J08	$\overline{\text{G\_TRDY}}$	K08	V_{DD}	L08	G_ADL05	M08	GND
J09	BS1	K09	$\overline{\text{G\_IRDY}}$	L09	G_ADL04	M09	G_ADL00
J10	BS0	K10	Reserved	L10	Reserved	M10	Reserved
J11	MDATA68	K11	Reserved	L11	Reserved	M11	Reserved
J12	MDATA69	K12	Reserved	L12	Reserved	M12	Reserved
J13	Reserved	K13	Reserved	L13	Reserved	M13	Reserved
J14	MDATA70	K14	Reserved	L14	Reserved	M14	Reserved
J15	Reserved	K15	Reserved	L15	Reserved	M15	Reserved
J16	MDATA71	K16	Reserved	L16	Reserved	M16	Reserved
J17	$\overline{\text{MUX\_CLKEN1B}}$	K17	Reserved	L17	Reserved	M17	Reserved
J18	$\overline{\text{MUX\_CLKEN2B}}$	K18	Reserved	L18	Reserved	M18	Reserved
J19	Reserved	K19	P_ADL28	L19	P_ADL29	M19	P_ADL30
J20	PLL_TUNE5	K20	V_{DD}	L20	P_ADL27	M20	GND
J21	GND	K21	P_ADL22	L21	OV_{DD}	M21	P_ADL23
J22	P_ADL19	K22	P_ADL18	L22	P_ADL17	M22	P_ADL16
J23	OV_{DD}	K23	P_ADL13	L23	GND	M23	P_ADL14
J24	P_ADL12	K24	P_ADL11	L24	P_ADL10	M24	P_ADL09
J25	GND	K25	P_ADL05	L25	V_{DD}	M25	P_ADL06
J26	$\overline{\text{CHKSTOP}}$	K26	P_ADL04	L26	P_ADL03	M26	P_ADL02
J27	V_{DD}	K27	PLL_RANGE0	L27	GND	M27	$\overline{\text{P\_TRDY}}$

Signals Listed by Ball Assignment (Part 4 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
N01	G_ADH27	P01	OV_{DD}	R01	G_ADH19	T01	G_ADH16
N02	G_ADH26	P02	G_ADH21	R02	G_ADH18	T02	G_ADH15
N03	GND	P03	G_ADH20	R03	GND	T03	G_ADH14
N04	G_ADH25	P04	V_{DD}	R04	G_ADH17	T04	G_ADH13
N05	G_ADH24	P05	$\overline{\text{G\_CBE7}}$	R05	$\overline{\text{G\_CBE4}}$	T05	$\overline{\text{G\_INTD}}$
N06	G_ADH23	P06	GND	R06	$\overline{\text{G\_ACK64}}$	T06	$\overline{\text{G\_INTC}}$
N07	G_ADH22	P07	$\overline{\text{G\_CBE6}}$	R07	$\overline{\text{G\_CBE3}}$	T07	$\overline{\text{G\_INTB}}$
N08	$\overline{\text{G\_STOP}}$	P08	OV_{DD}	R08	G_PAR	T08	GND
N09	Reserved	P09	$\overline{\text{G\_CBE5}}$	R09	Reserved	T09	$\overline{\text{G\_INTA}}$
N10	Reserved	P10	Reserved	R10	Reserved	T10	Reserved
N11	Reserved	P11	Reserved	R11	Reserved	T11	Reserved
N12	Reserved	P12	Reserved	R12	Reserved	T12	Reserved
N13	GND	P13	V_{DD}	R13	GND	T13	Reserved
N14	V_{DD}	P14	GND	R14	V_{DD}	T14	Reserved
N15	GND	P15	V_{DD}	R15	GND	T15	Reserved
N16	Reserved	P16	Reserved	R16	Reserved	T16	Reserved
N17	Reserved	P17	Reserved	R17	Reserved	T17	Reserved
N18	Reserved	P18	Reserved	R18	Reserved	T18	Reserved
N19	Reserved	P19	P_ADL31	R19	Reserved	T19	$\overline{\text{SYS\_BR2}}$
N20	P_ADL26	P20	OV_{DD}	R20	$\overline{\text{SYS\_DBG3}}$	T20	GND
N21	P_ADL24	P21	P_ADL25	R21	$\overline{\text{SYS\_DBG2}}$	T21	$\overline{\text{SYS\_DBG0}}$
N22	P_ADL15	P22	GND	R22	$\overline{\text{P\_DEVSEL}}$	T22	$\overline{\text{P\_FRAME}}$
N23	CE0_TEST	P23	PLL_LOCK	R23	PLL_TUNE4	T23	PLL_TUNE2
N24	P_ADL08	P24	V_{DD}	R24	$\overline{\text{P\_CBE0}}$	T24	$\overline{\text{P\_CBE1}}$
N25	GND	P25	P_ADL07	R25	GND	T25	$\overline{\text{P\_CBE2}}$
N26	P_ADL01	P26	P_ADL00	R26	TMS	T26	$\overline{\text{P\_CBE3}}$
N27	$\overline{\text{P\_RST}}$	P27	OV_{DD}	R27	PLL_TUNE3	T27	$\overline{\text{P\_GNT3}}$

Signals Listed by Ball Assignment (Part 5 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
U01	GND	V01	G_ADH11	W01	V_{DD}	Y01	G_ADH07
U02	G_ADH12	V02	G_ADH10	W02	G_ADH08	Y02	G_ADH06
U03	V_{DD}	V03	G_ADH09	W03	GND	Y03	$\overline{\text{G\_GNT3}}$
U04	$\overline{\text{G\_GNT7}}$	V04	$\overline{\text{G\_GNT6}}$	W04	$\overline{\text{G\_GNT4}}$	Y04	$\overline{\text{G\_GNT2}}$
U05	GND	V05	$\overline{\text{G\_GNT5}}$	W05	OV_{DD}	Y05	$\overline{\text{G\_GNT1}}$
U06	$\overline{\text{G\_REQ0}}$	V06	$\overline{\text{G\_REQ1}}$	W06	$\overline{\text{G\_REQ3}}$	Y06	$\overline{\text{G\_REQ4}}$
U07	OV_{DD}	V07	$\overline{\text{G\_REQ2}}$	W07	GND	Y07	$\overline{\text{G\_REQ5}}$
U08	$\overline{\text{G\_CBE2}}$	V08	V_{DD}	W08	PCG_CLK	Y08	SYS_DATA00
U09	$\overline{\text{G\_CBE1}}$	V09	$\overline{\text{G\_CBE0}}$	W09	Reserved	Y09	$\overline{\text{G\_REQ6}}$
U10	Reserved	V10	Reserved	W10	$\overline{\text{SYS\_AACK}}$	Y10	V_{DD}
U11	Reserved	V11	Reserved	W11	$\overline{\text{SYS\_ARTRY}}$	Y11	$\overline{\text{SYS\_GBL}}$
U12	Reserved	V12	Reserved	W12	$\overline{\text{SYS\_MCP2}}$	Y12	GND
U13	Reserved	V13	Reserved	W13	Reserved	Y13	$\overline{\text{SYS\_MCP3}}$
U14	Reserved	V14	Reserved	W14	$\overline{\text{SYS\_MCP0}}$	Y14	OV_{DD}
U15	Reserved	V15	Reserved	W15	Reserved	Y15	$\overline{\text{SYS\_MCP1}}$
U16	Reserved	V16	Reserved	W16	SYS_TT4	Y16	GND
U17	Reserved	V17	Reserved	W17	SYS_TT2	Y17	SYS_TT3
U18	Reserved	V18	Reserved	W18	SYS_TT1	Y18	V_{DD}
U19	$\overline{\text{SYS\_BR1}}$	V19	$\overline{\text{SYS\_BR0}}$	W19	Reserved	Y19	TCK
U20	$\overline{\text{SYS\_BR3}}$	V20	V_{DD}	W20	$\overline{\text{SYS\_DBG1}}$	Y20	$\overline{\text{SYS\_BG1}}$
U21	OV_{DD}	V21	SYS_ADDRP3	W21	GND	Y21	SYS_ADDRP0
U22	Reserved	V22	SYS_ADDRP2	W22	SYS_ADDRP1	Y22	SYS_ADDR01
U23	GND	V23	$\overline{\text{P\_SERR}}$	W23	OV_{DD}	Y23	SYS_ADDR02
U24	$\overline{\text{P\_STOP}}$	V24	$\overline{\text{P\_REQ3}}$	W24	SYS_ADDR00	Y24	SYS_ADDR03
U25	V_{DD}	V25	$\overline{\text{P\_REQ2}}$	W25	GND	Y25	$\overline{\text{SYS\_BG2}}$
U26	$\overline{\text{P\_PERR}}$	V26	$\overline{\text{P\_REQ1}}$	W26	$\overline{\text{P\_GNT2}}$	Y26	$\overline{\text{SYS\_TS}}$
U27	GND	V27	$\overline{\text{P\_REQ0}}$	W27	V_{DD}	Y27	$\overline{\text{P\_GNT1}}$

Signals Listed by Ball Assignment (Part 6 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AA01	G_ADH05	AB01	G_ADH03	AC01	OV_{DD}	AD01	$\overline{\text{G\_RESETOUT}}$
AA02	G_ADH04	AB02	$\overline{\text{G\_SERR}}$	AC02	G_ADH02	AD02	G_ADH00
AA03	OV_{DD}	AB03	$\overline{\text{G\_REQ64}}$	AC03	GND	AD03	G_IDSEL
AA04	$\overline{\text{G\_GNT0}}$	AB04	$\overline{\text{G\_DEVSEL}}$	AC04	$\overline{\text{G\_LOCK}}$	AD04	SYS_TBE
AA05	GND	AB05	G_PAR64	AC05	V_{DD}	AD05	SYS_DATAP5
AA06	$\overline{\text{G\_REQ7}}$	AB06	$\overline{\text{SYS\_TEA}}$	AC06	$\overline{\text{SYS\_TA\_HIT}}$	AD06	SYS_DATAP6
AA07	V_{DD}	AB07	SYS_DATAP7	AC07	GND	AD07	SYS_DATA27
AA08	SYS_DATA01	AB08	SYS_DATA08	AC08	SYS_DATA19	AD08	SYS_DATA28
AA09	GND	AB09	SYS_DATA09	AC09	OV_{DD}	AD09	SYS_DATA29
AA10	SYS_DATA02	AB10	SYS_DATA10	AC10	SYS_DATA20	AD10	SYS_DATA30
AA11	OV_{DD}	AB11	SYS_DATA11	AC11	GND	AD11	SYS_DATA31
AA12	SYS_DATA03	AB12	SYS_DATA12	AC12	SYS_DATA21	AD12	SYS_DATA32
AA13	SYS_DATA04	AB13	SYS_DATA13	AC13	SYS_DATA22	AD13	SYS_DATA33
AA14	SYS_DATA05	AB14	GND	AC14	SYS_DATA23	AD14	V_{DD}
AA15	SYS_DATA06	AB15	SYS_DATA14	AC15	SYS_DATA24	AD15	SYS_DATA34
AA16	SYS_DATA07	AB16	SYS_DATA15	AC16	SYS_DATA25	AD16	SYS_DATA35
AA17	OV_{DD}	AB17	SYS_DATA16	AC17	GND	AD17	SYS_DATA36
AA18	SYS_TT0	AB18	SYS_DATA17	AC18	SYS_DATA26	AD18	SYS_DATA37
AA19	GND	AB19	SYS_DATA18	AC19	OV_{DD}	AD19	$\overline{\text{SYS\_HRESET3}}$
AA20	$\overline{\text{SYS\_SRESET3}}$	AB20	$\overline{\text{SYS\_SRESET2}}$	AC20	$\overline{\text{SYS\_HRESET1}}$	AD20	$\overline{\text{SYS\_HRESET0}}$
AA21	V_{DD}	AB21	$\overline{\text{SYS\_SRESET1}}$	AC21	GND	AD21	$\overline{\text{SYS\_SRESET0}}$
AA22	SYS_ADDR04	AB22	SYS_ADDR06	AC22	SYS_ADDR11	AD22	SYS_ADDR14
AA23	GND	AB23	SYS_ADDR07	AC23	V_{DD}	AD23	SYS_ADDR15
AA24	SYS_ADDR05	AB24	SYS_ADDR08	AC24	SYS_ADDR12	AD24	SYS_ADDR16
AA25	OV_{DD}	AB25	SYS_ADDR09	AC25	GND	AD25	SYS_ADDR17
AA26	$\overline{\text{SYS\_BG3}}$	AB26	SYS_ADDR10	AC26	SYS_ADDR13	AD26	SYS_ADDR18
AA27	$\overline{\text{P\_GNT0}}$	AB27	PCI_CLK	AC27	OV_{DD}	AD27	SYS_ADDR19

Signals Listed by Ball Assignment (Part 7 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AE01	GND	AF01	$\overline{\text{SYS\_BG0}}$	AG01	$\overline{\text{SYS\_TA}}$		
AE02	G_ADH01	AF02	SYS_$\overline{\text{L2_HIT}}$	AG02	SYS_TSIZ2		
AE03	V_{DD}	AF03	SYS_DATAP1	AG03	GND		
AE04	SYS_DATAP4	AF04	SYS_DATAP2	AG04	SYS_DATAP0		
AE05	GND	AF05	$\overline{\text{SYS\_SHD}}$	AG05	OV_{DD}		
AE06	$\overline{\text{SYS\_TBST}}$	AF06	SYS_DATAP3	AG06	POWERGOOD		
AE07	OV_{DD}	AF07	SYS_DATA44	AG07	SYS_DATA56		
AE08	SYS_DATA38	AF08	SYS_DATA45	AG08	SYS_DATA57		
AE09	GND	AF09	SYS_DATA46	AG09	V_{DD}		
AE10	SYS_DATA39	AF10	SYS_DATA47	AG10	SYS_DATA58		
AE11	V_{DD}	AF11	SYS_DATA48	AG11	GND		
AE12	SYS_DATA40	AF12	SYS_DATA49	AG12	SYS_DATA59		
AE13	GND	AF13	SYS_DATA50	AG13	SYS_DATA60		
AE14	SYS_DATA41	AF14	SYS_DATA51	AG14	OV_{DD}		
AE15	GND	AF15	SYS_DATA52	AG15	SYS_DATA61		
AE16	SYS_DATA42	AF16	SYS_DATA53	AG16	SYS_DATA62		
AE17	V_{DD}	AF17	SYS_DATA54	AG17	GND		
AE18	SYS_DATA43	AF18	SYS_DATA55	AG18	SYS_DATA63		
AE19	GND	AF19	SYS_TSIZ0	AG19	V_{DD}		
AE20	$\overline{\text{SYS\_HRESET2}}$	AF20	SYS_TSIZ1	AG20	SYS_ADDR30		
AE21	OV_{DD}	AF21	SYS_ADDR23	AG21	SYS_ADDR31		
AE22	SYS_ADDR20	AF22	SYS_ADDR24	AG22	Reserved		
AE23	GND	AF23	SYS_ADDR25	AG23	OV_{DD}		
AE24	SYS_ADDR21	AF24	SYS_ADDR26	AG24	Reserved		
AE25	V_{DD}	AF25	SYS_ADDR27	AG25	GND		
AE26	SYS_ADDR22	AF26	SYS_ADDR28	AG26	Reserved		
AE27	GND	AF27	SYS_ADDR29	AG27	Reserved		

Signal Descriptions

The CPC710 embedded controller is packaged in a 728-ball flip-chip plastic ball grid array (FC-PBGA). The following tables describe the package level pinout.

Pin Summary

Group	No. of Pins
Nonmultiplexed signals	466
Multiplexed signals	10
Total Signal Pins	**476**
OV_{DD}	40
V_{DD}	44
Gnd	81
Total Power Pins	**165**
Reserved	87
Total Pins	**728**

In the table “Signal Functional Description” on page 36, each external signal is listed along with a short description of the signal function. Some signals are multiplexed on the same package pin (ball) so that the pin can be used for different functions. In cases where the multiplexed signals are functionally related, they are shown as a default signal followed by the alternate signal in square brackets (for example, G_GNT5[P_GNT4]). To see all of the signals that are multiplexed on a single pin, see “Signals Listed Alphabetically” on page 8. Active-low signals (for example, $\overline{IT1}$) are marked with an overline.

It is expected that in any single application a particular pin will always be programmed to serve the same function. The flexibility of multiplexing allows a single chip to offer a richer pin selection than would otherwise be possible.

The Type column in “Signal Functional Description” on page 36 describes the I/O circuit type. If more detailed information is needed, please refer to the IBM ASIC SA-12E Databook.

Signal Functional Description (Part 1 of 9)

Notes:
1. Receiver input has hysteresis
2. Must pull up
3. Must pull down
4. If not used, must pull up
5. If not used, must pull down
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
60x Interface				
$\overline{\text{CHKSTOP}}$	Check stop. Indicates that the CPC710 has detected a non-recoverable error condition and has entered check stop state.	O	2.5V CMOS	
$\overline{\text{DLK}}$	Deadlock ($\overline{\text{DLK}}$). Asserted when processor range of address is out of the non-deadlock zone. An address SYS_ARTRY is sent to the PowerPC when $\overline{\text{DLK}}$ is set.	O	3.3V LVTTL	
GPIO0:2	General purpose I/O signals.	I/O	5V tolerant 3.3 V PCI	
$\overline{\text{IT1}}$	Interrupt 1. Generated after writing 1 in the PCIC1_ITADDSET interrupt register. This interrupt can be used by an external interrupt controller. The writing can be made from the CPU in configuration mode or from the PCI-64 bus. Only the PowerPC CPU can reset the interrupt by writing 1 in the PCIL1_ITADDRESET interrupt reset register.	O	5V tolerant 3.3 V PCI	2
$\overline{\text{IT2}}$	Interrupt 2. Indicates the end of the DMA data transfer. Corresponds to assertion of bit 4 in the DMA0_GSCRx status register.	O	5V tolerant 3.3 V PCI	2
$\overline{\text{NODLK}}$	Deadlock Disable (NODLK). Used only when the deadlock address range checking is programmed: Asserted (0), deadlock checking is disabled. If tied high (1), deadlock checking can be performed.	I	3.3V LVTTL w/pull-up	
POWERGOOD	Normal operation when up (1). General system reset when down (0).	I	3.3V LVTTL w/pull-up	
$\overline{\text{SYS\_AACK}}$	Address Acknowledge. Indicates the address tenure is complete and the ARTRY sampling window ends on the following bus cycle. Address bus and transfer attribute signals must go to tri-state on the next bus cycle.	O	2.5V CMOS	
SYS_ADDR00:31	Address Bus. **Output:** Represents the physical address of a cache operation that should be snooped by devices on the 60x bus. A[0] is the most significant address bit. **Input:** Represents the physical address for the current transaction.	I/O	2.5V CMOS w/pull-up	
SYS_ADDRP0:3	Address Parity. **Output:** Represents one bit of odd parity for each of the four bytes of the address bus. Odd parity means that an odd number of bits, including the parity bit, are driven high. The signals are assigned as follows: SYS_ADDRP0 – SYS_ADDR00:07 SYS_ADDRP1 – SYS_ADDR08:15 SYS_ADDRP2 – SYS_ADDR16:23 SYS_ADDRP3 – SYS_ADDR24:31 **Input:** Represents one bit of *odd* parity for each of the four bytes of the address bus. A checkstop is generated if bad parity is detected and bit 8 is 1 in the error control register.	I/O	2.5V CMOS w/pull-up	

Signal Functional Description (Part 2 of 9)

Notes:
1. Receiver input has hysteresis
2. Must pull up
3. Must pull down
4. If not used, must pull up
5. If not used, must pull down
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
$\overline{\text{SYS\_ARTRY}}$	Address Retry. **Output:** indicates that the CPC710 detects a condition that requires an address tenure to be retried. **Input:** When asserted in response to a CPC710 cache operation, the CPC710 assumes the cache line is modified and/or present in a CPU or L2 cache. The CPC710 then retries the operation on the PCI bus and address tenure is not rerun until the device on the PCI bus reruns its transfer. The pre-charge logic is always signaled to initiate the pre-charge sequence.	I/O	2.5V CMOS	
$\overline{\text{SYS\_BR0:3}}$	Bus Request. Indicates the device on the 60x bus associated with this signal is requesting ownership of the address bus.	I	2.5V CMOS w/pull-up	4
$\overline{\text{SYS\_BG0:3}}$	Bus Grant. Indicates the master associated with this signal may, with proper qualification, assume mastership of the address bus.	O	2.5V CMOS	
SYS_DATA00:63	Data Bus. Byte 0: D[0:7] - DH[0:7] Byte 1: D[8:15] - DH[8:15] Byte 2: D[16:23] - DH[16:23] Byte 3: D[24:31] - DH[24:31] Byte 4: D[32:39] - DL[0:7] Byte 5: D[40:47] - DL[8:15] Byte 6: D[48:55] - DL[16:23] Byte 7: D[56:63] - DL[24:31]	I/O	2.5V CMOS w/pull-up	
SYS_DATAP0:7	Data Parity Bus. Represents one bit of odd parity for each of the eight bytes of the data bus. Odd parity means that an odd number of bits, including the parity bit, are driven high. The signal assignments correspond to the following: DP[0]: Data[0:7] DP[4]: Data[32:39] DP[1]: Data[8:15] DP[5]: Data[40:47] DP[2]: Data[16:23] DP[6]: Data[48:55] DP[3]: Data[24:31] DP[7]: Data[56:63]	I/O	2.5V CMOS w/pull-up	
$\overline{\text{SYS\_DBG0:3}}$	Data Bus Grant. Indicates the device associated with this signal may, with the proper qualification, assume mastership of the data bus.	O	2.5V CMOS	
$\overline{\text{SYS\_GBL}}$	Global. Always asserted by the CPC710 for transactions that it initiates to indicate that all devices on the 60x bus must snoop the transaction. Since the CPC710 asserts this signal only when it is PowerPC bus address master, no contention is possible with PowerPC 750 or 7400 input/output GBL signal connected to $\overline{\text{SYS\_GBL}}$.	O.D	2.5V CMOS w/pull-up	
$\overline{\text{SYS\_HRESET0:3}}$	Hard Reset. Indicates the device or card associated with this signal must initiate a complete hard reset. All outputs should be released to tri-state. Duration of reset, except for device hardware system reset, is controlled by software.	O	2.5V CMOS	
$\overline{\text{SYS\_L2\_HIT}}$	L2 Hit. Indicates an external slave has been addressed by the current master. The CPC710 arbiter uses this signal to confirm positive selection of an address tenure on the 60x bus. **Warning:** This signal is subject to timing constraints.	I	3.3V tolerant 2.5V CMOS	4

Signal Functional Description (Part 3 of 9)

Notes:
1. Receiver input has hysteresis
2. Must pull up
3. Must pull down
4. If not used, must pull up
5. If not used, must pull down
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
SYS_MCP0:3	Machine Check. Indicates that the CPC710 has detected an error condition and a machine check exception is desired. **Notes:** 1. SYS_MCP0 and SYS_MCP2 have same shape signal 2. SYS_MCP1 and SYS_MCP3 have same shape signal.	O	2.5V CMOS	2
SYS_SHD	Shared. **Output:** Not applicable; The CPC710 only pre-charges the signal. **Input:** Instructs the pre-charge logic to initiate a pre-charge sequence.	I/O	2.5V CMOS	
SYS_SRESET0:3	Soft Reset. Indicates the processor connected to this signal will take a reset exception. Occurs following a write to the CPU soft reset register (CPC0_SRST) that has the appropriate bit set.	O	2.5V CMOS	
SYS_TA	Transfer Acknowledge. **Output:** Indicates a single beat of data transfer between the CPC710 and a master on the 60x bus. For read transfers, indicates the data bus is valid with read data and the master must latch it in. For writes, indicates that the CPC710 has latched in write data from the data bus. The CPC710 asserts the signal for each beat in a burst transfer. **Input:** Indicates a single beat of data transfer has occurred. The CPC710 arbiter uses this signal and the address transfer attribute signals to determine the end of the data bus tenure.	I/O	2.5V CMOS w/pull-up	
SYS_TA_HIT	External Transfer Acknowledge Hit. A transition from high to low of this signal results in the generation of the SYS_TA output signal in the following system clock cycle.	I	3.3V LVTTL	2
SYS_TBE	Time Base Enable. Indicates the processor time bases should continue counting. Reflects bit 12 of the CPC0_UCTL register.	O	2.5V CMOS	
SYS_TBST	Transfer Burst. **Output signal and the TSIZ signals:** Indicate the data transfer size of the operation. The CPC710 sets this signal according to the bit in the CPC0_ATAS register for operations it initiates. **Input signal:** For normal memory accesses, indicates a burst transfer is in progress. For DMA instructions **eciwx** and **ecowx**, the input signal and the TSIZ signals indicate the 4-bit Resource ID (RID) of the DMA operation (TBST || TSIZ0-TSIZ2).	I/O	2.5V CMOS w/pull-up	
SYS_TEA	Transfer Error Acknowledge. **Output:** Indicates that the CPC710 has detected an error condition and that a machine check exception is desired. Assertion of this signal terminates the current data bus tenure. The CPC710 can be set up to transform any SYS_TEA to normal SYS_TA with machine check condition signaling on SYS_MCP0, SYS_MCP1, SYS_MCP2, or SYS_MCP3. **Input:** Informs the CPC710 60x bus arbiter that the current data bus tenure has been terminated.	I/O	2.5V CMOS w/pull-up	

Signal Functional Description (Part 4 of 9)

Notes:
1. Receiver input has hysteresis
2. Must pull up
3. Must pull down
4. If not used, must pull up
5. If not used, must pull down
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
$\overline{\text{SYS\_TS}}$	Transfer Start. **Output:** Indicates that the CPC710 has started an address tenure and the address bus and transfer attribute signals are valid. Only address-only operations and snoop operation with programmable TT code are performed. **Input:** Indicates a master on the 60x has started an address tenure and the address bus and transfer attribute signals are valid. For address tenures that require a data transfer, this signal also indicates a request for the data bus.	I/O	2.5V CMOS	
SYS_TSIZ0:2	Transfer Size. **Output signals and the TBST signal:** Indicate the data transfer size of the operation. The CPC710 sets these signals to a value stored in the CPC0_ATAS register for the operations it initiates. **Input signals and the TBST signal:** For normal memory accesses, indicate the data transfer size of the operation. For the DMA instructions **eciwx** and **ecowx**, they indicate the 4-bit Resource ID (RID) of the DMA operation ($\overline{\text{TBST}}$ || TSIZ0-TSIZ2).	I/O	2.5V CMOS w/pull-up	
SYS_TT0:4	Transfer Type. **Output:** Indicates the type of transfer in progress. The values are programmable according to the PowerPC type and stored in the CPC0_ATAS register. **Input:** Indicates the type of transfer in progress.	I/O	2.5V CMOS w/pull-up	
SDRAM Interface				
BS1:0	Internal Bank Select.	O	3.3V LVTTL	
MADDR0_EVEN	Memory Address bit 0 for even DIMMs.	O	3.3V LVTTL	
MADDR0_ODD	Memory Address bit 0 for odd DIMMs.	O	3.3V LVTTL	
MADDR13:1	Memory Address bits 13 to 1 (13 is msb).	O	3.3V LVTTL	
MDATA00:63	Memory Data.	I/O	3.3V LVTTL	
MDATA64:71	Memory Data ECC bits.	I/O	3.3V LVTTL	
$\overline{\text{MUX\_CLKEN1B}}$ $\overline{\text{MUX\_CLKEN2B}}$	Clock Enable of Data sent to the Memory (two signals with same shape for buffering issues).	O	3.3V LVTTL	
$\overline{\text{MUX\_CLKENA1}}$ $\overline{\text{MUX\_CLKENA2}}$	Clock Enable of Data sent to the CPC710. On Clock A1 the first part of the data is stored in the external MUX controller, and on clock A2 full transfer is done.	O	3.3V LVTTL	
$\overline{\text{MUX\_OEA:B}}$	Output Enable of Data to Port A or B.	O	3.3V LVTTL	
$\overline{\text{MUX\_SEL}}$	Control the MUX circuit of the external MUX controller.	O	3.3V LVTTL	
$\overline{\text{SDCAS0:1}}$	SDRAM Column Address Strobe (two signals with same shape for buffering issues). $\overline{\text{SDCAS1}}$ can be converted to a Chip Data Mask (SDDQM) by setting bit 14 of the SDRAM0_MCCR register.	O	3.3V LVTTL	
SDCKE0:9	SDRAM Clock Enable. Ten signals with same shape for buffering issues.	O	3.3V LVTTL	
$\overline{\text{SDCS00:11}}$	SDRAM Chip Select.	O	3.3V LVTTL	

Signal Functional Description (Part 5 of 9)

Notes:
1. Receiver input has hysteresis
2. Must pull up
3. Must pull down
4. If not used, must pull up
5. If not used, must pull down
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
[SDDQM]	Data Output Mask: Same shape signal available on I/Os SDCAS1, SDRAS1, WE1, or G_ARB after setting bits 14 and 15 of the SDRAM0_MCCR register.	O	3.3V LVTTL	
SDRAS0:1	SDRAM Row Address Strobe (two signals with same shape for buffering issues). SDRAS1 can be converted to a Chip Data Mask (SDDQM) by setting bit 14 of the SDRAM0_MCCR register.	O	3.3VLVTTL	
WE0:1	Memory Write Enable (two signals with same shape for buffering issues). WE1 can be converted to a Chip Data Mask (SDDQM) by setting bit 14 of the SDRAM0_MCCR register.	O	3.3V LVTTL	
PCI-32 Interface				
P_ADL31:00	32-bit Multiplexed Address/Data. A write operation is defined as the transfer of data from the PCI bus master to a PCI slave device on the PCI Bus.	I/O	5V tolerant 3.3V PCI	
P_CBE3:0	Bus Command/Byte Enable.	I/O	5V tolerant 3.3V PCI	
P_DEVSEL	Device Select.	I/O	5V tolerant 3.3V PCI	
P_FRAME	Cycle Frame. Driven by the current master to indicate the beginning and duration of an access.	I/O	5V tolerant 3.3V PCI	
P_GNT0:3 [P_GNT4:6]G_GNT5:7	PCI-32 Bus Grants.	O	5V tolerant 3.3V PCI	
P_IRDY	Initiator Ready.	I/O	5V tolerant 3.3V PCI	
P_LOCK	Lock. Used to establish, maintain, and release resource locks on PCI-32. Reserved for future use. Tying up this signal is recommended.	I	5V tolerant 3.3V PCI	
P_MEMACK	Memory Acknowledge. Indicates that the CPC710 has flushed all CPU to PCI-32 bus buffers and any CPU access to PCI is being SYS_ARTRYed.	O	3.3V LVTTL	
P_MEMREQ	Memory Request. Indicates a PCI device accessing system memory has a potential deadlock and requests the CPC710 to flush all posted CPU to PCI buffers and ARTRY all PCI-32 bus transfers from the 60x bus.	I	3.3V LVTTL	
P_PAR	Parity Bit.	I/O	5V tolerant 3.3V PCI	
P_PERR	PCI-32 Data Parity Error.	I/O	5V tolerant 3.3V PCI	
P_REQ0:3 [P_REQ4:6]G_REQ5:7	PCI-32 Bus Requests. P_REQ2 is sampled at Reset, to select arbitration on the PCI-32 bus. The arbitration can be made by the CPC710 (P_REQ2 = 1) or by external circuit (P_REQ2 = 0). In case of external arbitration, the request is send to PCI from P_GNT1 and the grant from the external arbiter is received on pin P_REQ1. Extended Flash is available only when the CPC710 is the PCI-32 arbiter.	I	5V tolerant 3.3V PCI	

Signal Functional Description (Part 6 of 9)

Notes:
1. Receiver input has hysteresis
2. Must pull up
3. Must pull down
4. If not used, must pull up
5. If not used, must pull down
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
P_RST	PCI-32 Bus Reset.	O	5V tolerant 3.3V PCI	
P_SERR	PCI-32 System Parity Error. Reports parity errors on address, special cycle data, or systems.	I/O	5V tolerant 3.3V PCI	
P_STOP	Stop. Asserted by the target to request the master to stop current transaction.	I/O	5V tolerant 3.3V PCI	
P_TRDY	Target Ready. Asserted by the target when ready to receive data.	I/O	5V tolerant 3.3V PCI	
PCI_CLK	Main clock input for the PCI-32 bit bridge (maximum 33 MHz).	I	3.3V LVTTL	1
PCI-64 Interface				
G_ACK64	Acknowledge 64-bit transfer.	I/O	3.3V PCI	
G_ADH31:00	32-bit Multiplexed Address/Data Higher Part. In the address phase when G_REQ64 is asserted, these bits are the upper part of the 64 bit address AD63:00. During data phase an additional 32-bits of data are transferred when G_REQ64 and G_ACK64 are both asserted.	I/O	3.3V PCI	
G_ADL31:00	32-bit Multiplexed Address/Data Lower Part. A write operation is defined as the transfer of data from the PCI bus master to a PCI slave device on the PCI Bus.	I/O	3.3V PCI	
G_ARB	Arbiter. Asserted when the CPC710 is the PCI-64 arbiter. Can be converted to a Chip Data Mask (SDDQM) by setting bit 15 of the SDRAM0_MCCR register.	O	3.3V LVTTL	
G_CBE7:0	Bus Command/Byte Enable.	I/O	3.3V PCI	
G_DEVSEL	Device Select.	I/O	3.3V PCI	
G_FRAME	Cycle Frame	I/O	3.3V PCI	
G_GNT0:4 G_GNT5:7[P_GNT4:6]	Bus Grants.	O	5V tolerant 3.3V PCI	
G_IDSEL	Initialization Device Select. Used as chip select during configuration.	I	3.3V PCI	
G_INTA:D	Interrupts A:D.	O	5V tolerant 3.3V PCI	2
G_IRDY	Initiator Ready	I/O	3.3V PCI	
G_LOCK	Lock. Used to establish, maintain and release resource locks on PCI-64. Reserved for future usage. It is recommended to tie up this signal.	I	3.3V PCI	
G_PAR	Parity bit.	I/O	3.3V PCI	
G_PAR64	Parity upper double word.	I/O	3.3V PCI	
G_PERR	Data Parity Error.	I/O	3.3V PCI	

Signal Functional Description (Part 7 of 9)

Notes:
1. Receiver input has hysteresis
2. Must pull up
3. Must pull down
4. If not used, must pull up
5. If not used, must pull down
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
G_REQ64	Request 64-bit transfer. External pull-up required	I/O	3.3V PCI	
G_REQ0:4 G_REQ5:7[P_REQ4:6]	Bus Requests. G_REQ2 is sampled at Reset, to select arbitration on the PCI-64 bus. The arbitration can be made by the CPC710 (G_REQ2 = 1) or by external circuit (G_REQ2 = 0). The input G_REQ2 must be held low in order to deselect the internal arbiter. External logic must hold this input low for at least four (4) PCI 64 clock cycles after the rising edge of PLL_RESET. Holding G_REQ2 low until the positive going edge of POWERGOOD is also acceptable. In case of external arbitration, the request is sent to PCI from G_GNT1 and the grant from the external arbiter is received on pin G_REQ1. G_REQ5:7 are programmed by setting bits 21:23 of the CPC0_PGCHP register	I	5V tolerant 3.3V PCI	
G_RESETOUT	Local Reset. Asserted by PCI-64 reset and special conditions.	O.D	5V tolerant 3.3V PCI	
G_RST	Reset PCI-64 Bus. **Input:** Replicated on G_RESETOUT when programmed (no internal use). **Output:** Activated by the CPC710 at power up or by programming.	I/O	5V tolerant 3.3V PCI	2
G_SERR	System Parity Error.	I/O	3.3V PCI	
G_STOP	Stop. Asserted by the target to request the master to stop the current transaction.	I/O	3.3V PCI	
G_TRDY	Target Ready. Asserted by the target when ready to receive data.	I/O	3.3V PCI	
PCG_CLK	Main clock input for the PCI-64 bit bridge (maximum 66 MHz).	I	3.3V LVTTL	
SIO Interface				
FLASH_CE	Extended Flash Chip Enable. This signal goes to 0 after the CPC710 has decoded an access to the Extended Flash address range. 1: Boot Flash Enabled. 0: Extended Flash Enable. This signal must be used on card to insure that Boot Flash and Extended Flash cannot be accessed at the same time.	O	3.3V LVTTL	
FLASH_OE	Output Enable. Flash ROM.	O	3.3V LVTTL	
FLASH_WE	Write Enable. Flash ROM.	O	3.3V LVTTL	
PRES_OE0:1	Output Enable. Presence detect (PD) buffer 0 or buffer 1.	O	3.3V LVTTL	
XADR_LAT	Latch Signal. For SIO address register.	O	3.3V LVTTL	
XCVR_RD	Address Direction. SIO address bus.	O	3.3V LVTTL	

Signal Functional Description (Part 8 of 9)

Notes:
1. Receiver input has hysteresis
2. Must pull up
3. Must pull down
4. If not used, must pull up
5. If not used, must pull down
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
JTAG Interface				
TCK	Test Clock.	I	3.3V LVTTL w/pull-up	
TDI	Test Data In.	I	3.3V LVTTL w/pull-up	
TDO	Test Data Out.	O	3.3V LVTTL	
TMS	Test Mode Select.	I	3.3V LVTTL w/pull-up	
$\overline{\text{TRST}}$	Reset.	I	3.3V LVTTL w/pull-up	
System Interface				
$\overline{\text{CE0\_TEST}}$	Reserved	I	3.3VLVTTL w/pull-down	
PLL_LOCK	Output indicating the PLL is locked.	O	3.3VLVTTL	
PLL_RANGE1:0	PLL frequency range selector for the System Clock. 00: 50 to 100 MHz 01: 58 to 114 MHz 10: 66 to 134 MHz 11: 80 to 160 MHz	I	3.3V LVTTL	
$\overline{\text{PLL\_RESET}}$	Reset and Bypass mode enable of the PLL	I	3.3V LVTTL w/pull-up	
PLL_TUNE5:0	Loop stability tuning control of the PLL. Recommended values: 010101 if range is 50 to 100 MHz 010011 if range is 58 to 114 MHz 010011 if range is 66 to 134 MHz 010011 if range is 80 to 160 MHz	I	3.3V LVTTL	

Signal Functional Description (Part 9 of 9)

Notes:
1. Receiver input has hysteresis
2. Must pull up
3. Must pull down
4. If not used, must pull up
5. If not used, must pull down
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
SYS_CLK	System Reference Clock. Used as: 1. 60X bus clock 2. Attached processor clock 3. Synchronous SDRAM signals This clock is not synchronized with the PCI-32 and the PCI-64 clocks.	I	3.3V LVTTL	
Power				
AV_{DD}	Analog voltage—2.5V. Filtered supply for PLL circuits.	n/a	n/a	
GND	Ground.	n/a	n/a	
OV_{DD}	Output driver voltage—3.3V.	n/a	n/a	
V_{DD}	Logic voltage—2.5V.	n/a	n/a	
Other pins				
Reserved	Do not connect signals, voltage, or ground to these pins.	n/a	n/a	

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device

Characteristic	Symbol	Value	Unit
Supply Voltage (Internal Logic)	V_{DD}	0 to 2.56	V
Supply Voltage (I/O Interface)	OV_{DD}	0 to 3.6	V
PLL Supply Voltage	AV_{DD}	0 to 2.5	V
Input Voltage (3.3V LVTTL receivers)	V_{IN}	0 to 3.6	V
Storage Temperature Range	T_{STG}	- 65 to +150	°C

Package Thermal Specifications

Parameter	Symbol	Value	Airflow ft/min (m/sec)	Unit
Junction-to-case thermal resistance	θ_{JC}	1	n/a	°C/W
Junction-to-air thermal resistance	θ_{JA}	16	0 (0)	°C/W
		12.6	100 (0.51)	
		11.4	200 (1.02)	

Note: These specifications are calculated estimates based on the following:

1. CFD Flotherm™ computer model results
2. 101.5 x 114.5 JEDEC 2S2P thermal test card based on Document JC-15-98-69 (dated Feb. 10, 1998)
3. Power dissipation of 1.26W at sea level
4. No heat sink

Module should be used in accordance with 05L3625 “FC-PBGA Packaging Applications Specifications.” Heat sink should be attached in accordance with 05L3630 “Bonding heat sinks to cover plates of FC-PBGA modules.”

Recommended DC Operating Conditions

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Notes:

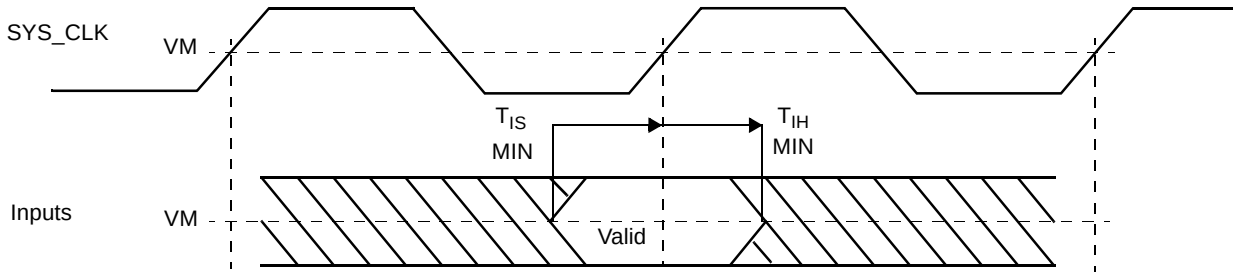
1. PCI drivers meet PCI specifications.
2. It is recommended that your system design derive the V_{DD} supply from the OV_{DD} supply so as to minimize the possibility of V_{DD} being present in the absence of OV_{DD}.
3. V_{OH} and V_{OL} specified at OV_{DD} = 3V, V_{DD} = 2.3V, T_J = 100°C

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Logic Supply Voltage—133MHz	V_{DD}	2.44	2.5	2.56	V	
Logic Supply Voltage—100MHz	V_{DD}	2.38	2.5	2.63	V	
I/O Supply Voltage	OV_{DD}	3.14	3.3	3.46	V	
PLL Supply Voltage	AV_{DD}	2.44	2.5	2.56	V	
Input Logic High (3.3V LVTTL receivers)	V_{IH3}	2		OV_{DD}	V	
Input Logic High (5V LVTTL receivers)	V_{IH5}	2		5	V	
Input Logic Low	V_{IL}	0		0.8	V	
Output Logic High (3.3V LVTTL)	V_{OH3}	2.4		OV_{DD}	V	3
Output Current High (3.3V LVTTL)	I_{OH3}			11	mA	3
Output Logic Low (3.3V LVTTL)	V_{OL3}	0		0.4	V	3
Output Current Low (3.3V LVTTL)	I_{OL3}			7	mA	3
Output Logic High (2.5V CMOS)	V_{OH2}	2		V_{DD}	V	3
Output Current High (2.5V CMOS)	I_{OH2}		5.3	5.3	mA	3
Output Logic Low (2.5V CMOS)	V_{OL2}	0		0.4	V	3
Output Current Low (2.5V CMOS)	I_{OL2}			7	mA	3
Input Leakage Current	I_{IL1}		<1	10	µA	
Input Max Allowable Overshoot (3.3V LVTTL receivers)	V_{IMAO3}			V_{DD} + 0.6	V	
Input Max Allowable Overshoot (5V LVTTL receivers)	V_{IMAO5}			5.5	V	
Input Max Allowable Undershoot (3.3V or 5.0V receivers)	V_{IMAU}	-0.6			V	
Output Max Allowable Overshoot (3.3V receivers)	V_{OMAO3}			V_{DD} + 0.6	V	
Output Max Allowable Overshoot (5V receivers)	V_{OMAO5}			5.5	V	
Output Max Allowable Undershoot (3.3V receivers)	V_{OMAU3}	-0.6			V	
Die Junction Temperature—133MHz	T_J	-40		+85	°C	
Die Junction Temperature—100MHz	T_J	-40		+105	°C	

AC Timing Specifications

Parameter	OV_{DD}	V_{DD}	T_J
Nominal operating conditions at 133MHz	3.3 V ± 5%	2.5 V ± 2.5%	-40°C to +85°C
Slow case: Input Setup (T_{IS}) and Output Maximum Arrival time	3.14 V	2.44 V	+85°C
Fast case: Input Hold (T_{IH}) and Output Minimum Arrival time	3.46 V	2.56 V	-40°C
Nominal operating conditions at 100 MHz	3.3 V ± 5%	2.5 V ± 5%	-40°C to +105°C
Slow case: Input Setup (T_{IS}) and Output Maximum Arrival time	3.14 V	2.38 V	+105°C
Fast case: Input Hold (T_{IH}) and Output Minimum Arrival time	3.46 V	2.63 V	-40°C

AC Input Timing Waveform



VM (Voltage Midpoint):
SYS_CLK = 0.8V
60x bus inputs = 0.9V
All other inputs = 1.5V

Clock Timing

Notes:
1. Cycle-to-cycle
2. SYS_CLK (Min) specified for PLL_RANGE1:0 = 0b00. SYS_CLK (Max) specified for PLL_RANGE1:0 = 0b11.

Parameter	Min	Max	Units	Notes
SYS_CLK clock input frequency	50	133	MHz	
SYS_CLK pulse width	1	–	ns	
SYS_CLK jitter	–	± 0.15	ns	1
SYS_CLK slew rate	1	4	V/ns	
PCI_CLK frequency	TBD	33.3	MHz	
PCI_CLK duty cycle	40	60	%	
PCG_CLK duty cycle	40	60	%	
PCG_CLK jitter	–	TBD	ns	

I/O Specifications—133 MHz (Part 1 of 2)

Notes:
1. Output Valid from SYS_CLK
2. Output Hold from SYS_CLK
3. All inputs are referenced to the rising edge of SYS_CLK.

Signal	Input (ns)		Output (ns)				Notes
			Valid		Hold		
	Setup (T_{IS} min)	Hold (T_{IH} min)	Max	Load (pf)	Min	Load (pf)	
60x Bus Interface							
SYS_ADDR0:31 SYS_ADDRP0:3	2.7	0	5	30	0.2	6	
SYS_DATA0:63 SYS_DATP0:7	2.3	0.2	4.5	30	0.3	6	
SYS_ARTRY	4.2	0.1	3.9	30	0.4	6	
SYS_SHD	2.2	0	4.3	30	0.3	6	
SYS_TA SYS_TEA	3.1	0	4.3	30	0.3	6	
SYS_TBE	na	na	4.3	30	0.3	6	
SYS_TBST	1.8	0	4.3	30	0.3	6	
SYS_TSIZ0:2	2.3	0.1	4.3	30	0.3	6	
SYS_TT0:4	3.7	0	4.3	30	0.3	6	
SYS_TS	3.7	0	4.3	30	0.3	6	
SYS_L2_HIT	4.2	0.1	na	na	na	na	
SYS_BR0:3	3.7	0	na	na	na	na	
SYS_AACK	na	na	3.9	30	0.4	6	
SYS_BG0:3 SYS_DBG0:3	na	na	5	15	0.5	6	
SYS_GBL	na	na	4.3	30	0.3	6	
SYS_MACHK0:1 SYS_HRESET0:1 SYS_SRESET0:1	na	na	4.8	25	0.6	5	
CHKSTOP	na	na	6.4	25	1.6	5	
SDRAM Interface							
MDATA00:71	1.78	0.5	4.3	15	0.5	5	1, 2
SDCS0:11	na	na	4.4	30	1	15	1, 2
SDCKE0:9	na	na	4.4	30	1	15	1, 2
SDRAS0:1 SDCAS0:1 WE0:1	na	na	7.9	70			1, 2
MADDR13:1 MADDR0_ODD MADDR0_EVEN BS1:0	na	na	7.1	30	0.5	10	1, 2
MUX_CLKEN1B MUX_CLKEN2B	na	na	5	35	0.5	10	1, 2
MUX_CLKENA1	na	na	4.8	35	0.5	10	1, 2
MUX_CLKENA2	na	na	4.7	35	0.5	10	1, 2
MUX_OEA	na	na	5	35	0.5	10	1, 2
MUX_OEB	na	na	5.2	35	0.5	10	1, 2
MUX_SEL	na	na	5.4	35	1	10	1, 2

I/O Specifications—133 MHz (Part 2 of 2)

Notes:
1. Output Valid from SYS_CLK
2. Output Hold from SYS_CLK
3. All inputs are referenced to the rising edge of SYS_CLK.

Signal	Input (ns)		Output (ns)				Notes
			Valid		Hold		
	Setup (T_{IS} min)	Hold (T_{IH} min)	Max	Load (pf)	Min	Load (pf)	
SIO Interface							
$\overline{\text{FLASH\_CE}}$ $\overline{\text{FLASH\_OE}}$ $\overline{\text{FLASH\_WE}}$	na	na	8.1	80	0.8	5	1, 2
$\overline{\text{PRES\_OE0:1}}$	na	na	5.4	20	1	5	1, 2
XADR_LAT	na	na	6.9	25	1	5	1, 2
XCVR_RD	na	na	6.2	25	1	5	1, 2
Note: Refer to P_ADL31:0 signals in the PCI-32 section for FLASH address and data signal I/O timing.							
PCI Interface (See “PCI I/O Specifications—133 MHz” on page 52)							

I/O Specifications—100 MHz (Part 1 of 2)

Notes:
1. Output Valid from SYS_CLK
2. Output Hold from SYS_CLK
3. All inputs are referenced to the rising edge of SYS_CLK.

Signal	Input (ns)		Output (ns)				Notes
			Valid		Hold		
	Setup (T_{IS} min)	Hold (T_{IH} min)	Max	Load (pf)	Min	Load (pf)	
60x Bus Interface							
SYS_ADDR0:31 SYS_ADDRP0:3	2.9	0	5.2	30	0.2	6	
SYS_DATA0:63 SYS_DATP0:7	2.5	0.2	4.7	30	0.3	6	
SYS_ARTRY	4.4	0.1	4.1	30	0.4	6	
SYS_SHD	2.4	0	4.5	30	0.3	6	
SYS_TA SYS_TEA	3.3	0	4.5	30	0.3	6	
SYS_TBE	na	na	4.5	30	0.3	6	
SYS_TBST	2	0	5	25	0.6	5	
SYS_TSIZ0:2	2.5	0.1	5	25	0.6	5	
SYS_TT0:4	3.9	0	5	25	0.6	5	
SYS_TS	3.9	0	4.5	30	0.3	6	
SYS_L2_HIT	4.5	0.1	na	na	na	na	
SYS_BR0:3	3.9	0	na	na	na	na	
SYS_AACK	na	na	4.1	30	0.4	6	
SYS_BG0:3 SYS_DBG0:3	na	na	5.2	15	0.5	6	
SYS_GBL	na	na	5	25	0.6	5	
SYS_MACHK0:1 SYS_HRESET0:1 SYS_SRESET0:1	na	na	5	25	0.6	5	
CHKSTOP	na	na	6.6	25	1.6	5	
SDRAM Interface							
MDATA00:71	2	0.5	4.5	15	0.5	5	1, 2
SDCS0:11	na	na	4.6	30	1	15	1, 2
SDCKE0:9	na	na	4.6	30	1	15	1, 2
SDRAS0:1 SDCAS0:1 WE0:1	na	na	8.2	70			1, 2
MADDR13:1 MADDR0_ODD MADDR0_EVEN BS1:0	na	na	7.3	30	0.5	10	1, 2
MUX_CLKEN1B MUX_CLKEN2B	na	na	5.2	35	0.5	10	1, 2
MUX_CLKENA1	na	na	5.8	35	0.5	10	1, 2
MUX_CLKENA2	na	na	4.9	35	0.5	10	1, 2
MUX_OEA	na	na	5.2	35	0.5	10	1, 2
MUX_OEB	na	na	5.4	35	0.5	10	1, 2
MUX_SEL	na	na	5.6	35	1	10	1, 2

I/O Specifications—100 MHz (Part 2 of 2)

Notes:
1. Output Valid from SYS_CLK
2. Output Hold from SYS_CLK
3. All inputs are referenced to the rising edge of SYS_CLK.

Signal	Input (ns)		Output (ns)				Notes
	Setup (T_{IS} min)	Hold (T_{IH} min)	Valid		Hold		
			Max	Load (pf)	Min	Load (pf)	
SIO Interface							
$\overline{\text{FLASH\_CE}}$ $\overline{\text{FLASH\_OE}}$ $\overline{\text{FLASH\_WE}}$	na	na	8.1	80	0.8	5	1, 2
$\overline{\text{PRES\_OE0:1}}$	na	na	5.4	20	1	5	1, 2
XADR_LAT	na	na	6.9	25	1	5	1, 2
XCVR_RD	na	na	6.2	25	1	5	1, 2
Note: Refer to P_ADL31:0 signals in the PCI-32 section for FLASH address and data signal I/O timing.							
PCI Interface (See “PCI I/O Specifications—133 MHz” on page 52)							

PCI I/O Specifications—133 MHz

Notes:

1. Output Valid from PCI_CLK
2. Input Setup to PCI_CLK
3. Input Hold from PCI_CLK
4. Output Valid from PCG_CLK
5. Input Setup to PCG_CLK
6. Input Hold from PCG_CLK

Signal	Input (ns)		Output Valid (ns)			Notes
	Setup (T_{IS} min)	Hold (T_{IH} min)	Min	Max	Load (pf)	
PCI-32 Interface @ 33 MHz						
P_ADL31:00 P_CBE3:0 P_DEVSEL P_FRAME P_IRDY P_PAR P_PERR P_SERR P_STOP P_TRDY	7	0.5	2.6	11	50	1, 2, 3
P_LOCK	na	na	na	na	50	
P_GNT0:3	na	na	3.2	12	50	1
P_MEMACK	na	na	4.4	5	30	1
P_REQ0:6	12	0.5	na	na	na	2, 3
P_MEMREQ	na	na	na	na	na	2, 3
PCI-64 Interface @ 66 MHz						
G_ADH31:0 G_ADL31:0	1.8	0	2	7.4	10	4, 5, 6
G_CBE7:0	3	0	2	6.9	10	4, 5, 6
G_ACK64	3.8	0	2	6.4	10	4, 5, 6
G_REQ64	2.1	0	2	7.2	10	4, 5, 6
G_DEVSEL	3.8	0	2	6	10	4, 5, 6
G_FRAME	3.4	0	2	6.4	10	4, 5, 6
G_IRDY	4.3	0	2	6	10	4, 5, 6
G_LOCK	na	na	na	na	10	
G_PAR	2.8	0	na	na	10	4, 5, 6
G_PAR64	2.1	0	2	6.6	10	4, 5, 6
G_PERR	1	0	2	6.3	10	4, 5, 6
G_SERR	1.8	0	2	6.5	10	4, 5, 6
G_STOP	3	0	2	6.6	10	4, 5, 6
G_TRDY	3.6	0	2	6.5	10	4, 5, 6
G_GNT0:2 G_GNT4:7	na	na	2	6.4	10	4
G_GNT3	na	na	2	6	10	4
G_IDSEL	1.8	0	na	na	na	5, 6
G_REQ0:7	4.3	0	na	na	na	5, 6

PCI I/O Specifications—100 MHz

Notes:
1. Output Valid from PCI_CLK
2. Input Setup to PCI_CLK
3. Input Hold from PCI_CLK
4. Output Valid from PCG_CLK
5. Input Setup to PCG_CLK
6. Input Hold from PCG_CLK

Signal	Input (ns)		Output Valid (ns)			Notes
	Setup (T_{IS} min)	Hold (T_{IH} min)	Min	Max	Load (pf)	
PCI-32 Interface @ 33 MHz						
P_ADL31:00 P_CBE3:0 P_DEVSEL P_FRAME P_IRDY P_PAR P_PERR P_SERR P_STOP P_TRDY	7	0.5	2	11.2	50	1, 2, 3
P_LOCK	na	na	na	na	50	
P_GNT0:3	na	na	2	12.2	50	1
P_MEMACK	na	na	na	11.2	50	1
P_REQ0:6	12	0.5	na	na	na	2, 3
P_MEMREQ	na	na	na	na	na	2, 3
PCI-64 Interface @ 66 MHz						
G_ADH31:0 G_ADL31:0	2	0	2	7.6	10	4, 5, 6
G_CBE7:0	3.2	0	2	7.1	10	4, 5, 6
G_ACK64	4	0	2	6.6	10	4, 5, 6
G_REQ64	2.3	0	2	7.4	10	4, 5, 6
G_DEVSEL	4	0	2	6.2	10	4, 5, 6
G_FRAME	3.6	0	2	6.6	10	4, 5, 6
G_IRDY	4.5	0	2	6.2	10	4, 5, 6
G_LOCK	na	na	na	na	10	
G_PAR	3	0	2	6.6	10	4, 5, 6
G_PAR64	2.3	0	2	6.8	10	4, 5, 6
G_PERR	1.2	0	2	6.5	10	4, 5, 6
G_SERR	2	0	2	6.7	10	4, 5, 6
G_STOP	3.2	0	2	6.8	10	4, 5, 6
G_TRDY	3.8	0	2	6.7	10	4, 5, 6
G_GNT0:2 G_GNT4:7	na	na	2	6.6	10	4
G_GNT3	na	na	2	6.2	10	4
G_IDSEL	2	0	na	na	na	5, 6
G_REQ0:7	4.5	0	na	na	na	5, 6

Printed in the United States of America March 2002

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SA14-2572-05