

IDT QDR™ IIPC Foreign Object Model for Microengine **Development Environment** Intel® IXA SDK 3.0

Product IDT75K134FOM

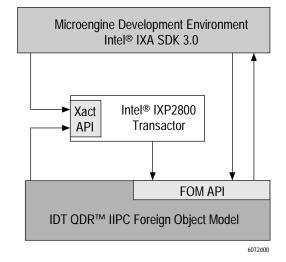
Introduction

Evolving network speeds require critical functions, such as forwarding and classification, to migrate towards dedicated hardware devices. IDT has introduced a family of IP Co-Processors with a QDR™ (Quad Data Rate) interface that will connect seamlessly to network processors conforming to the NPF2001.114.14 (LA-1) specification, such as Intel's new network processors. These devices accelerate search functions required for applications such as Access Control Lists (ACL), Flow Caching and Forwarding.

To further accelerate time to market, IDT's Foreign Object Model (FOM), a cycle- and data-accurate C simulation model, allows customers to evaluate packet-processing solutions in a simulation environment prior to system availability.

The FOM, supplied as a DLL (dynamic-link library), fits into the Microengine Development Environment of the Intel® Internet Exchange Architecture (IXA) Software Development Kit 3.0, as shown in the Simulation System Block Diagram.

Figure 1.0 Simulation System Block Diagram



Features List

- The IDT75K134FOM (Foreign Object Model) is a full C simulation model of IDT's 75K52134/75K62134, an IP Co-Processor with a seamless QDR[™] interface to Intel's new network processors. The FOM implementation is both cycle- and data-accurate.
- The QDR™ interface conforms to Intel's Foreign Object Model interface for the IXP2800 and IXP2400 Microengine Development Environment in the Intel® IXA SDK 3.0
- The FOM simulates all of the QDR™ IIPC's internal registers & Ternary Content Addressable Memory (CAM) core
- The FOM supports all 75K52134/75K62134 commands, including:
 - Standard Lookup
 - Multi-Hit Lookup
 - Multi-Database Lookup
 - Re-Issue Multi-Database Lookup
 - Multi-Hit Invalidate
 - Learn (per Database)
 - Read/Write internal resources
- The FOM supports the following additional features:
 - **Multiple contexts**
 - Database configuration
 - A pool of 72-bit Global Mask registers
 - Indirection SRAM™
 - Aaina
 - Error and warning messages for illegal or improper instruction combinations
 - Debug option, which allows the logging of events and error messages
- FOM initialization module allows model customization
 - System hardware configuration
 - Search machine device cascade depth
 - Indirection SRAM[™] support
 - Debug on/off and verbosity settings
- **System Requirements**
 - Microsoft Windows™ 2000
 - 128 MB of Ram



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