IBM11M32845CB

PRELIMINARY

32M x 72 Chipkill Correct DRAM Module

Features

- 168-Pin JEDEC Standard, 8-Byte Dual In-line Memory Module
- 32M x 72 (Dual Bank) Chipkill Correct EDO DIMM
- Performance:

		-5R
t_{RAC}	$\overline{RAS}$ Access Time	50ns
t_{CAC}	$\overline{CAS}$ Access Time	19ns
t_{AA}	Access Time From Address	34ns
t_{RC}	Cycle Time	101ns
t_{HPC}	EDO Mode Cycle Time	22ns

- All inputs and outputs are LVTTL compatible
- Single 3.3V ± 0.15V Power Supply
- Gold contacts
- Optimized for ECC applications
- System Performance Benefits:
  - Buffered inputs (except $\overline{RAS}$)
  - Reduced noise (32 V_{SS}/V_{DD} pins)
  - Buffered PDs
- Extended Data Out (EDO) Mode, Read-Modify-Write Cycles
- Refresh Modes: $\overline{RAS}$-Only, CBR, and Hidden Refresh
- 8192 refresh cycles distributed across 128ms
- Card sizes: 5.25" x 1.90" x 0.320"
- DRAMs in TSOJ Package

Description

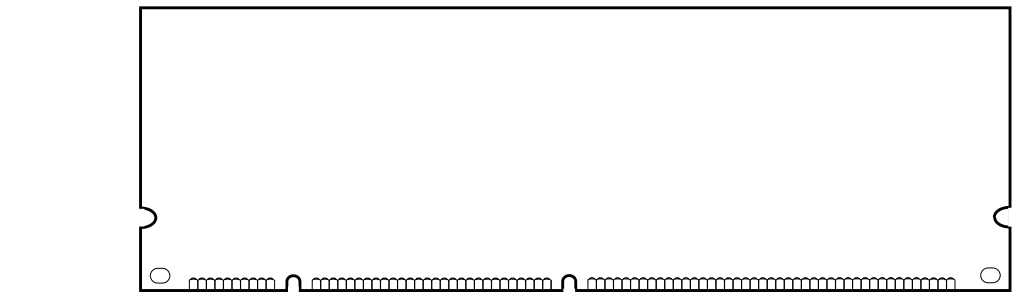
IBM11M32885B/C is an industry-standard 168-pin 8-byte Dual In-line Memory Module (DIMM) for ECC applications which is organized as a 32M x 72 high-speed memory array and is configured as two 16M x 72 banks. The DIMM uses additional checkbit DRAMs and an ASIC to provide chipkill correction when deployed in existing single-error-correct ECC systems.

Improved system performance is provided by the on-DIMM buffering of selected input signals. The specified timings include all buffer, net, and skew delays, which simplifies the memory subsystem design analysis. The $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 50ns.

Presence Detect (PD) and Identification Detect (ID) bits provide information about the DIMM density, addressing, performance, and features. PD bits can be dotted at the system level and activated for each DIMM position using the PD enable ($\overline{PDE}$) signal. ID bits also allow detection of card features, and may be dot-or'ed at the system level to provide information for the entire DIMM bank.

All IBM 168-pin DIMMs provide a high-performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products are the x64 and x72 parity (5V) DIMMs and ECC DIMMs (5V and 3.3V).

Card Outline



Discontinued (7/00 - last order; 9/00 - last ship)

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32M x 72 Chipkill Correct DRAM Module

Pin Description

$\overline{RAS}0$, $\overline{RAS}1$, $\overline{RAS}2$, $\overline{RAS}3$	Row Address Strobe
$\overline{CAS}0$, $\overline{CAS}1$, $\overline{CAS}4$, $\overline{CAS}5$	Column Address Strobe (Buffered)
$\overline{WE}0$, $\overline{WE}2$	Read/write Input (Buffered)
$\overline{OE}0$, $\overline{OE}2$	Output Enable (Buffered)
A0 - A12	Address Inputs (Buffered)
DQx	Data Input/Output
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connect
DU	Do Not Use
PD1 - PD8	Presence Detects (Buffered)
$\overline{PDE}$	Presence Detect Enable
ID0 - ID1	ID Bits

Pinout

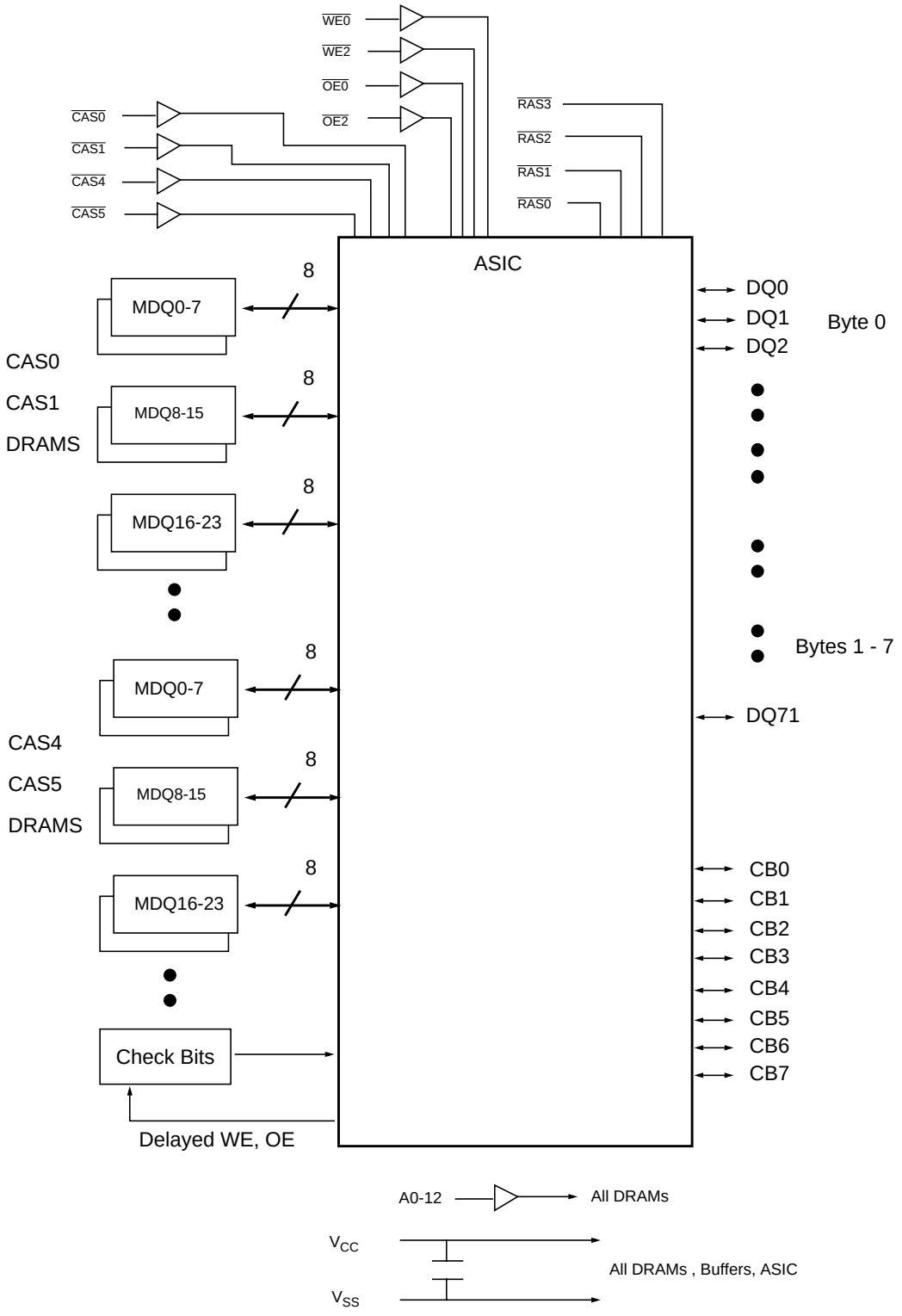
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	43	V_{SS}	127	V_{SS}
2	DQ0	86	DQ36	44	$\overline{OE}2$	128	NC
3	DQ1	87	DQ37	45	$\overline{RAS}2$	129	$\overline{RAS}3$
4	DQ2	88	DQ38	46	$\overline{CAS}4$	130	$\overline{CAS}5$
5	DQ3	89	DQ39	47	NC	131	NC
6	V_{CC}	90	V_{CC}	48	$\overline{WE}2$	132	$\overline{PDE}$
7	DQ4	91	DQ40	49	V_{CC}	133	V_{CC}
8	DQ5	92	DQ41	50	DU	134	NC
9	DQ6	93	DQ42	51	NC	135	NC
10	DQ7	94	DQ43	52	DQ18	136	DQ54
11	DQ8	95	DQ44	53	DQ19	137	DQ55
12	V_{SS}	96	V_{SS}	54	V_{SS}	138	V_{SS}
13	DQ9	97	DQ45	55	DQ20	139	DQ56
14	DQ10	98	DQ46	56	DQ21	140	DQ57
15	DQ11	99	DQ47	57	DQ22	141	DQ58
16	DQ12	100	DQ48	58	DQ23	142	DQ59
17	DQ13	101	DQ49	59	V_{CC}	143	V_{CC}
18	V_{CC}	102	V_{CC}	60	DQ24	144	DQ60
19	DQ14	103	DQ50	61	NC	145	NC
20	DQ15	104	DQ51	62	NC	146	NC
21	DQ16	105	DQ52	63	NC	147	NC
22	DQ17	106	DQ53	64	NC	148	NC
23	V_{SS}	107	V_{SS}	65	DQ25	149	DQ61
24	DU	108	NC	66	DQ26	150	DQ62
25	DU	109	NC	67	DQ27	151	DQ63
26	V_{CC}	110	V_{CC}	68	V_{SS}	152	V_{SS}
27	$\overline{WE}0$	111	NC	69	DQ28	153	DQ64
28	$\overline{CAS}0$	112	$\overline{CAS}1$	70	DQ29	154	DQ65
29	NC	113	NC	71	DQ30	155	DQ66
30	$\overline{RAS}0$	114	$\overline{RAS}1$	72	DQ31	156	DQ67
31	$\overline{OE}0$	115	NC	73	V_{CC}	157	V_{CC}
32	V_{SS}	116	V_{SS}	74	DQ32	158	DQ68
33	A0	117	A1	75	DQ33	159	DQ69
34	A2	118	A3	76	DQ34	160	DQ70
35	A4	119	A5	77	DQ35	161	DQ71
36	A6	120	A7	78	V_{SS}	162	V_{SS}
37	A8	121	A9	79	PD1	163	PD2
38	A10	122	A11	80	PD3	164	PD4
39	A12	123	NC	81	PD5	165	PD6
40	V_{CC}	124	V_{CC}	82	PD7	166	PD8
41	NC	125	NC	83	ID0	167	ID1
42	NC	126	NC	84	V_{CC}	168	V_{CC}

Note: All pin assignments are consistent for all 8 Byte versions.

Ordering Information

Part Number	Organization	Speed	Addr.	Leads	Dimension	Power
IBM11M32885CB-5RY	32M x 72	5Rns	13/11	Gold	5.25” x 1.65” x 0.320”	3.3V

x 72 ECC DIMM Block Diagram (2 Banks, x4 DRAMs)



Truth Table

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Column Address	$\overline{PDE}$	DQx
Standby		H	H→X	X	X	X	X	X	High Impedance
Read		L	L	H	L	Row	Col	X	Valid Data Out
Early-Write		L	L	L	X	Row	Col	X	Valid Data In
Late-Write		L	L	H→L	H	Row	Col	X	Valid Data In
RMW		L	L	H→L	L→H	Row	Col	X	Valid Data Out, Valid Data In
EDO Page Mode - Read 1st Cycle		L	H→L	H	L	Row	Col	X	Valid Data Out
Subsequent Cycles		L	H→L	H	L	N/A	Col	X	Valid Data Out
EDO Page Mode - Write 1st Cycle		L	H→L	L	X	Row	Col	X	Valid Data In
Subsequent Cycles		L	H→L	L	X	N/A	Col	X	Valid Data In
EDO Page Mode - RMW 1st Cycle		L	H→L	H→L	L→H	Row	Col	X	Valid Data Out, Valid Data In
Subsequent Cycles		L	H→L	H→L	L→H	N/A	Col	X	Valid Data Out, Valid Data In
$\overline{RAS}$-Only Refresh		L	H	X	X	Row	N/A	X	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh		H→L	L	H	X	X	X	X	High Impedance
Hidden Refresh	Read	L→H→L	L	H	L	Row	Col	X	Data Out
	Write	L→H→L	L	H	X	Row	Col	X	Data In
Read Presence Detects		X	X	X	X	X	X	L	Not Affected (PD Bits Valid)

Presence Detect

Pin	-5R	Special
PD1 (PD1 - PD4: Addressing/Density)	1	1
PD2	0	0
PD3	0	0
PD4	0	0
PD5 (EDO Detection)	1	1
PD6 (PD6 - PD7: Speed)	0	1
PD7	0	0
PD8 (Parity/ECC Designator)	0	0
ID0 (DIMM Type/Width)	0	0
ID1 (Refresh Mode)	0	0

1. PD1-8 are buffered outputs (0 = driven to V_{OL}, 1 = open)
2. ID0-1 are unbuffered outputs (0 = V_{SS}, 1 = open)
3. $\overline{PDE}$ should be tied high or low at system level if not used

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to 4.6	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} + 0.5, 4.6)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5, 4.6)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	TBD	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1
I_{OUTPD}	Short Circuit Output Current (PD)	60	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.
2. Maximum power occurs when all banks are active (refresh cycle).

Recommended DC Operating Conditions (T_A = 0 to 65°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	3.15	3.3	3.45	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.3	V	1, 2
V_{IL}	Input Low Voltage	-0.3	—	0.8	V	1, 2

1. All voltages referenced to V_{SS}.
2. V_{IH} may overshoot to V_{CC} + 1.2V for pulse widths of ≤ 4.0ns. Additionally, V_{IL} may undershoot to -2.0V for pulse widths ≤ 4.0ns (or -1.0V for ≤ 8.0ns). Pulse widths measured at 50% points with amplitude measured peak to DC reference.

Capacitance (T_A = 0 to +65°C, V_{CC} = 3.3V ± 0.15V)

Symbol	Parameter	Max	Units
C_{I1}	Input Capacitance (A0 - A12)	18	pF
C_{I2}	Input Capacitance ($\overline{RAS}$)	100	pF
C_{I3}	Input Capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	18	pF
C_{I4}	Input Capacitance ($\overline{PDE}$)	18	pF
C_{I01}	Input/Output Capacitance (DQx)	18	pF
C_{01}	Output Capacitance (PD)	15	pF
C_{02}	Output Capacitance (ID)	5	pF

DC Electrical Characteristics (T_A = 0 to +65°C, V_{CC} = 3.3V ± 0.15V)

Symbol	Parameter		13/11 Addressing Min	13/11 Addressing Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)		—	1804	ma	1, 2, 3
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	88	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)		—	3520	ma	1, 3, 4
I_{CC4}	EDO Page Mode Current Average Power Supply Current, EDO (Hyper) Page Mode ($\overline{RAS}$ ≤ V_{IL}, $\overline{CAS}$, Address Cycling: t_{HPC} = t_{HPC} min)		—	1749	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	44	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)		—	2794	mA	1, 3, 4
$I_{I(L)}$	Input Leakage Current (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)), All Other Pins Not Under Test = 0V	$\overline{RAS}$	-34	+34	µA	
		DQx	-10	+10		
		CAS, WE, OE, A1-A12	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output “H” Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low level Output “L” Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.
4. Refresh current is specified for 1 bank active and 1 bank standby.

AC Characteristics (T_A = 0 to +65°C, V_{CC} = 3.3V ± 0.15V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200ms is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delay adders: 2ns minimum, 5ns maximum delay, no pulse shrinkage to the DRAM device timings. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specification of 60ns.
4. AC measurements assume t_T = 2ns.

Read, Write, Read-Modify-Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-5R		Unit	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	89	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	35	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	8	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	50	100K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	8	100K	ns	
t_{ASR}	Row Address Setup Time	5	—	ns	
t_{RAH}	Row Address Hold Time	8	—	ns	
t_{ASC}	Column Address Setup Time	2	—	ns	
t_{CAH}	Column Address Hold Time	7	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	12	32	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	10	20	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	13	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	43	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	18	—	ns	3
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	-2	—	ns	4
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	-2	—	ns	4
t_T	Transition Time (Rise and Fall)	1	30	ns	

1. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by $t_{CAC.}$
2. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RAD}(max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by $t_{AA.}$
3. Either t_{CDD} or t_{ODD} must be satisfied.
4. Either t_{DZC} or t_{DZO} must be satisfied.

Write Cycle

Symbol	Parameter	-5R		Unit	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	ns	1
t_{WCH}	Write Command Hold Time	9	—	ns	
t_{WP}	Write Command Pulse Width	7	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	12	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	9	—	ns	
t_{DS}	D_{IN} Setup Time	-2	—	ns	2
t_{DH}	D_{IN} Hold Time	15	—	ns	2

1. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-5R		Unit	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	50	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	19	ns	1, 2
t_{AA}	Access Time from Address	—	34	ns	1, 2
t_{OEA}	Access Time from $\overline{OE}$	—	18	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	2	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	ns	
t_{OES}	$\overline{OE}$ setup time prior to $\overline{CAS}$	7	—	ns	
t_{ORD}	$\overline{OE}$ setup time prior to $\overline{RAS}$ (Hidden Refresh)	2	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	18	—	ns	5
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	2	18	ns	4
t_{OFF}	Output Buffer Turn-off Delay	2	18	ns	4, 6

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, $t_{AA,}$ t_{OEA}.
3. Either t_{RCH} or t_{RRH} must be satisfied.
4. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
5. Either t_{CDD} or t_{ODD} must be satisfied.
6. t_{OFF} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever is last.

Read-Modify-Write Cycle

Symbol	Parameter	-5R		Unit	Notes
		Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	123	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	70	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	40	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	50	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	7	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

EDO Mode Cycle

Symbol	Parameter	-5R		Units	Notes
		Min.	Max.		
t_{HCAS}	$\overline{CAS}$ Pulse Width (EDO Page Mode)	8	10K	ns	
t_{HPC}	EDO Page Mode Cycle Time (Read/Write)	20	—	ns	
t_{HPRWC}	EDO Page Mode Read Modify Write Cycle Time	63	—	ns	
t_{DOH}	Data-out Hold Time from $\overline{CAS}$	10	—	ns	
t_{WHZ}	Output buffer Turn-Off Delay from $\overline{WE}$	2	15	ns	
t_{WPZ}	$\overline{WE}$ Pulse Width to Output Disable at $\overline{CAS}$ High	10	—	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	ns	1
t_{RASP}	EDO Page Mode $\overline{RAS}$ Pulse Width	50	200K	ns	
t_{OEP}	$\overline{OE}$ High Pulse Width	10	—	ns	
t_{OEHC}	$\overline{OE}$ High Hold Time from $\overline{CAS}$ High	10	—	ns	

1. Measured with the specified current load and 100pF at V_{OL} = 0.8V and V_{OH} = 2.0V.

Refresh Cycle

Symbol	Parameter	-5R		Unit	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	3	—	ns	
t_{REF}	Refresh Period	—	128	ms	1
		—	64	ms	2

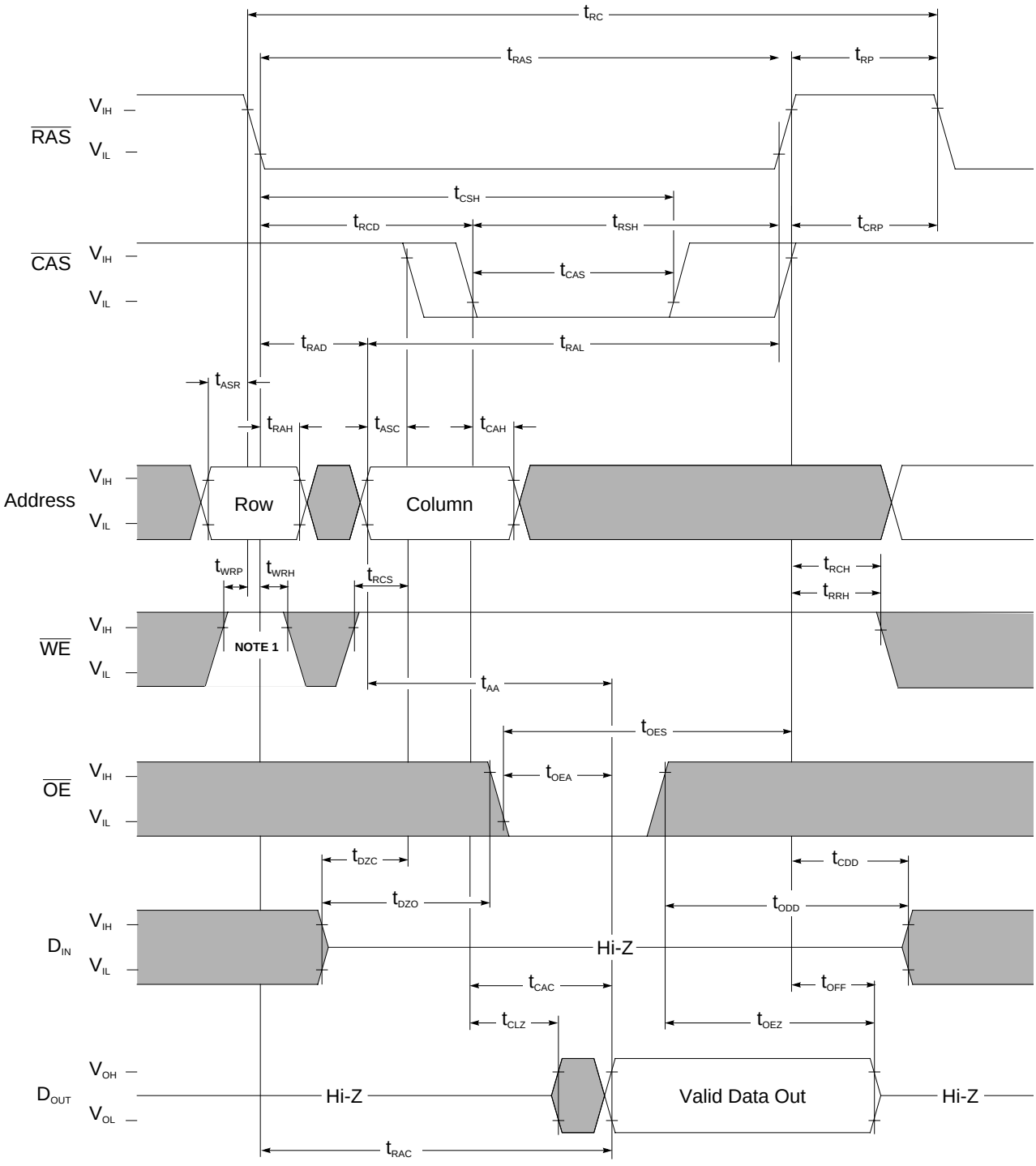
1. 13/11 addressing: 8096 refreshes for RAS Only Refresh.
2. 13/11 addressing: 4096 refreshes for CBR.

Presence Detect Read Cycle

Symbol	Parameter	-5R		Unit	Notes
		Min	Max		
t_{PD}	$\overline{PDE}$ to Valid Presence Detect Data	—	10	ns	1
t_{PDOFF}	$\overline{PDE}$ Inactive to Presence Detects Inactive	0	10	ns	2

1. Measured with the specified current load and 100pF.
2. t_{PDOFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

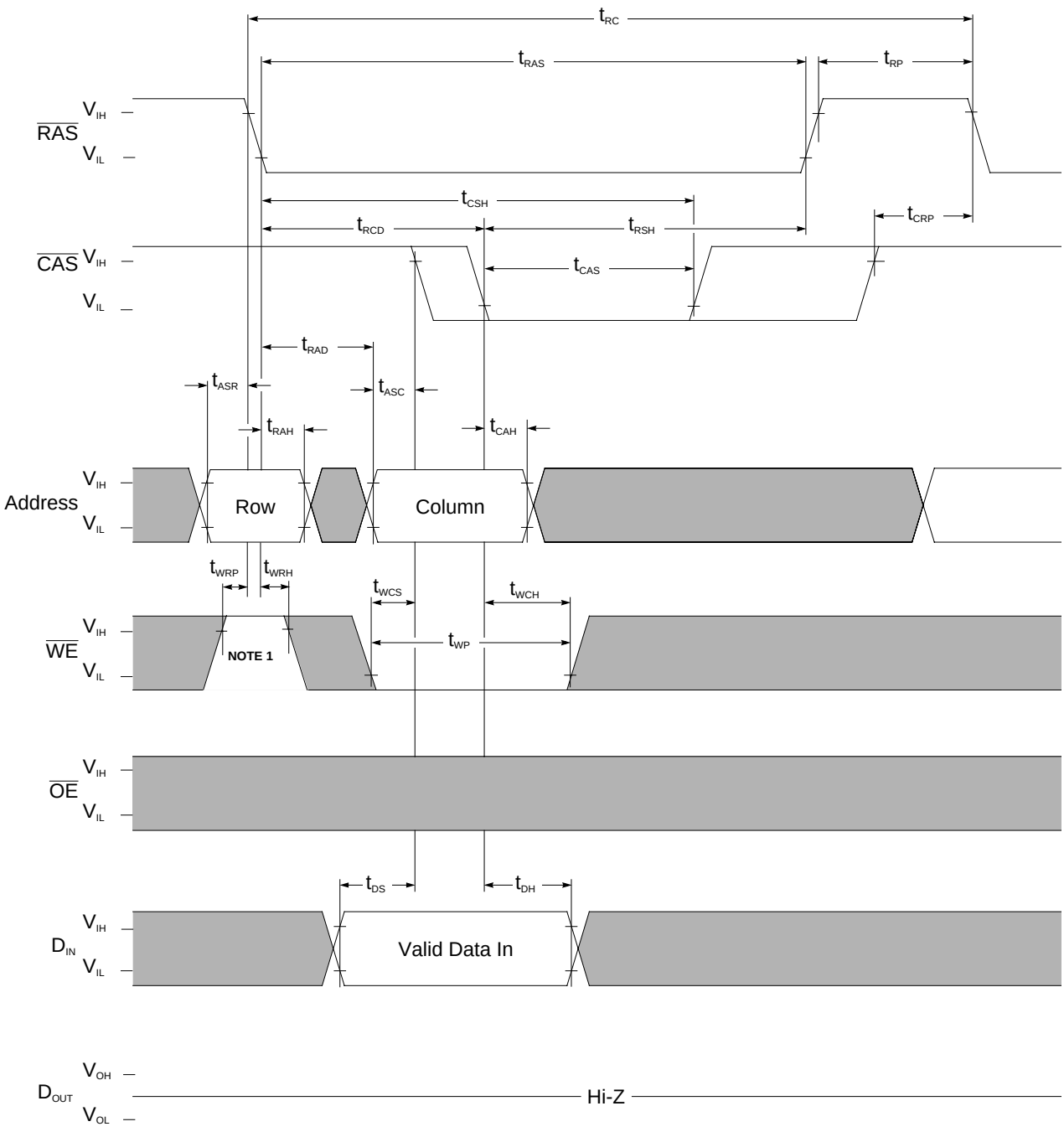
Read Cycle



: "H": or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

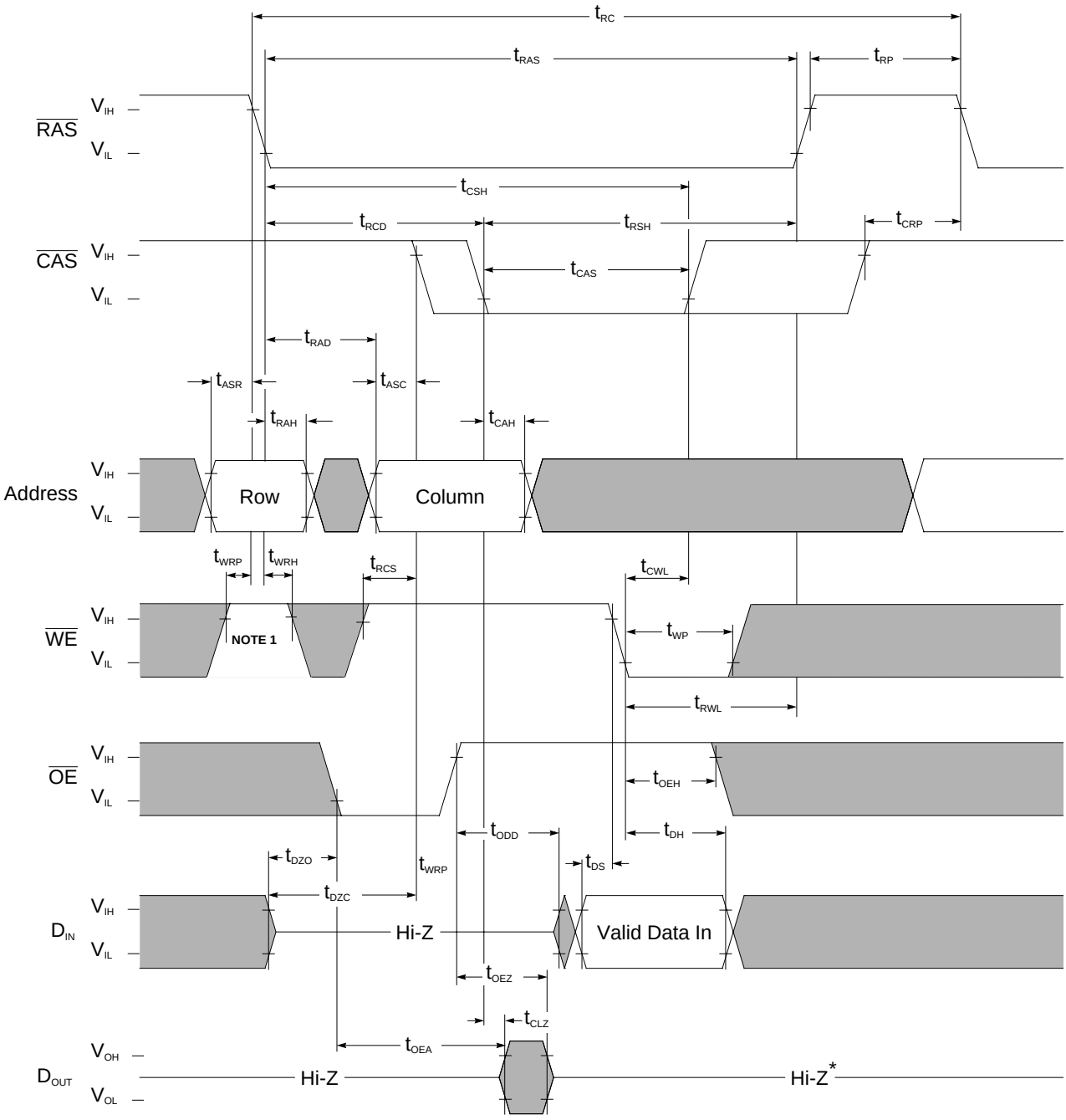
Write Cycle (Early Write)



: “H” or “L”

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

Write Cycle (Late Write)

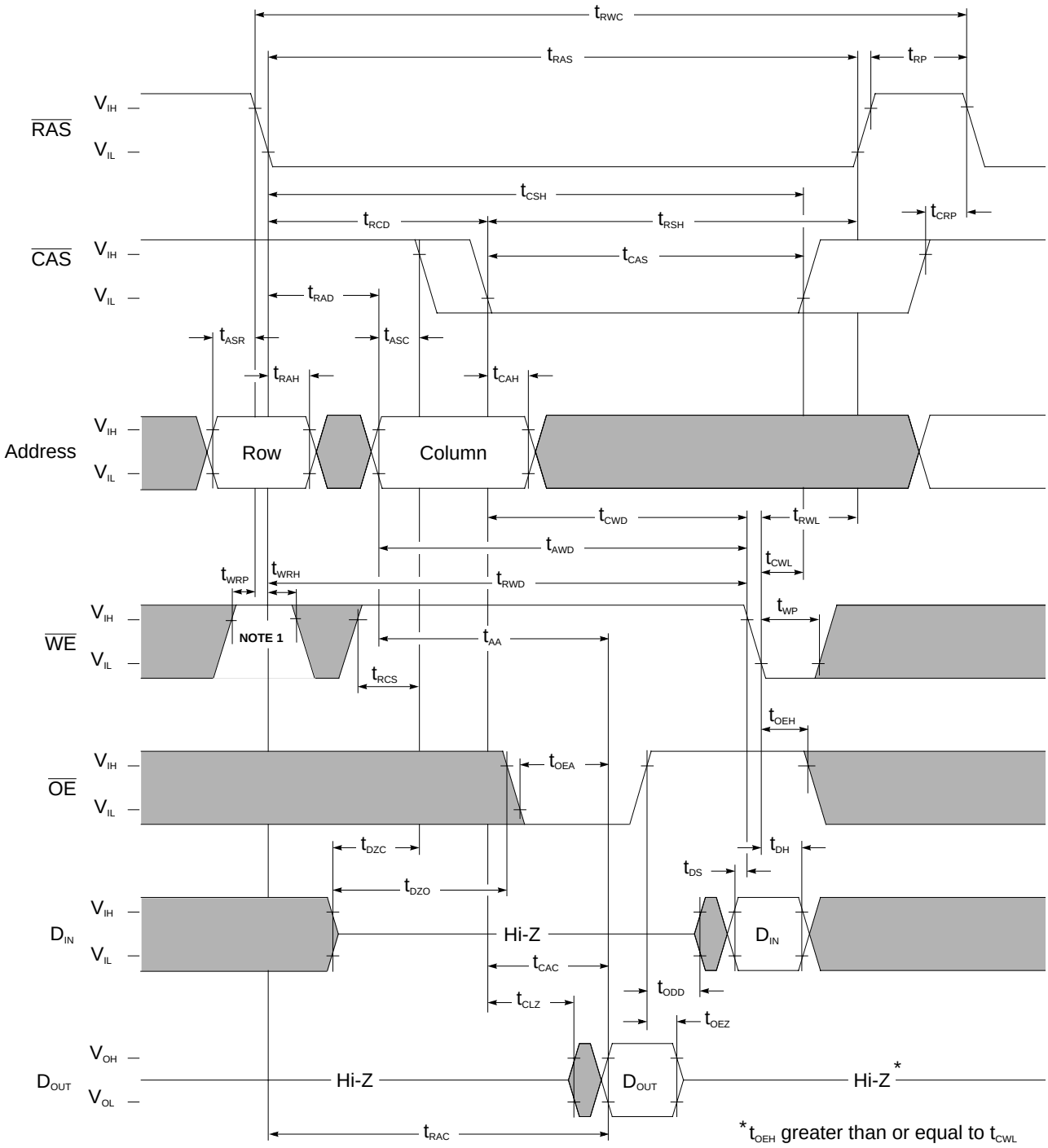


: "H" or "L"

* t_{OEH} greater than or equal to t_{CWL}

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

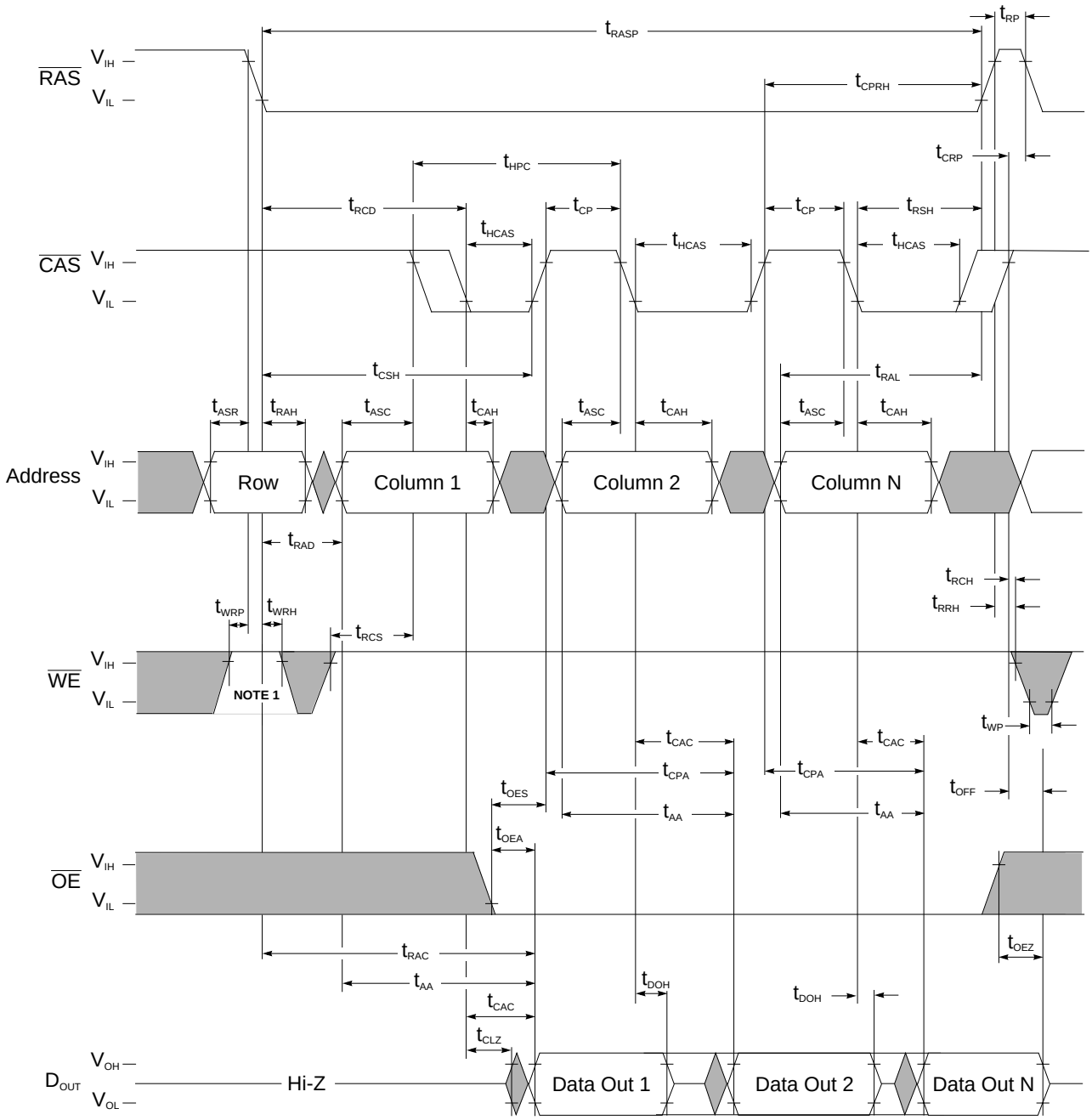
Read-Modify-Write-Cycle



: “H” or “L”

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

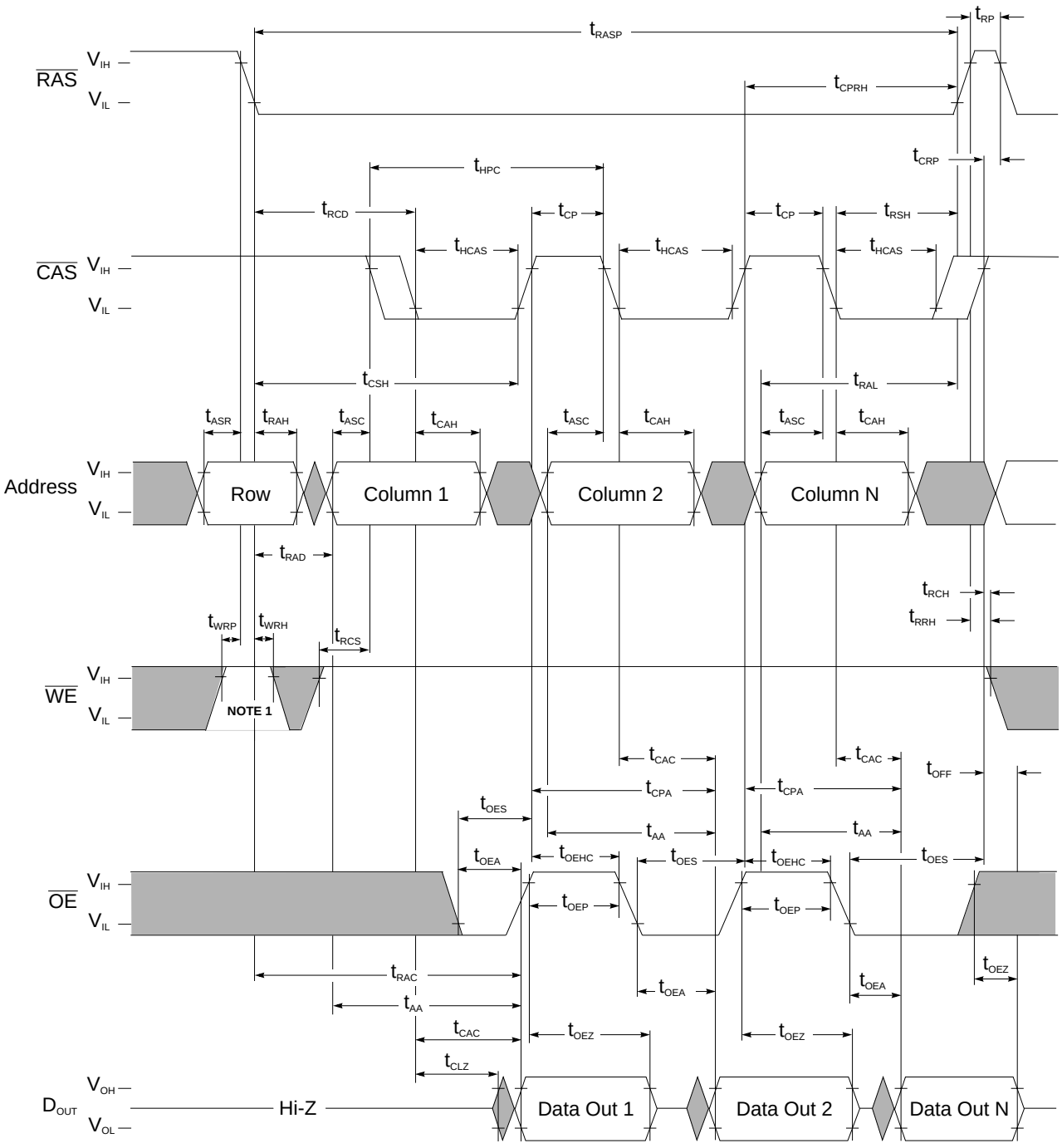
EDO Page Mode Read Cycle



: “H” or “L”

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

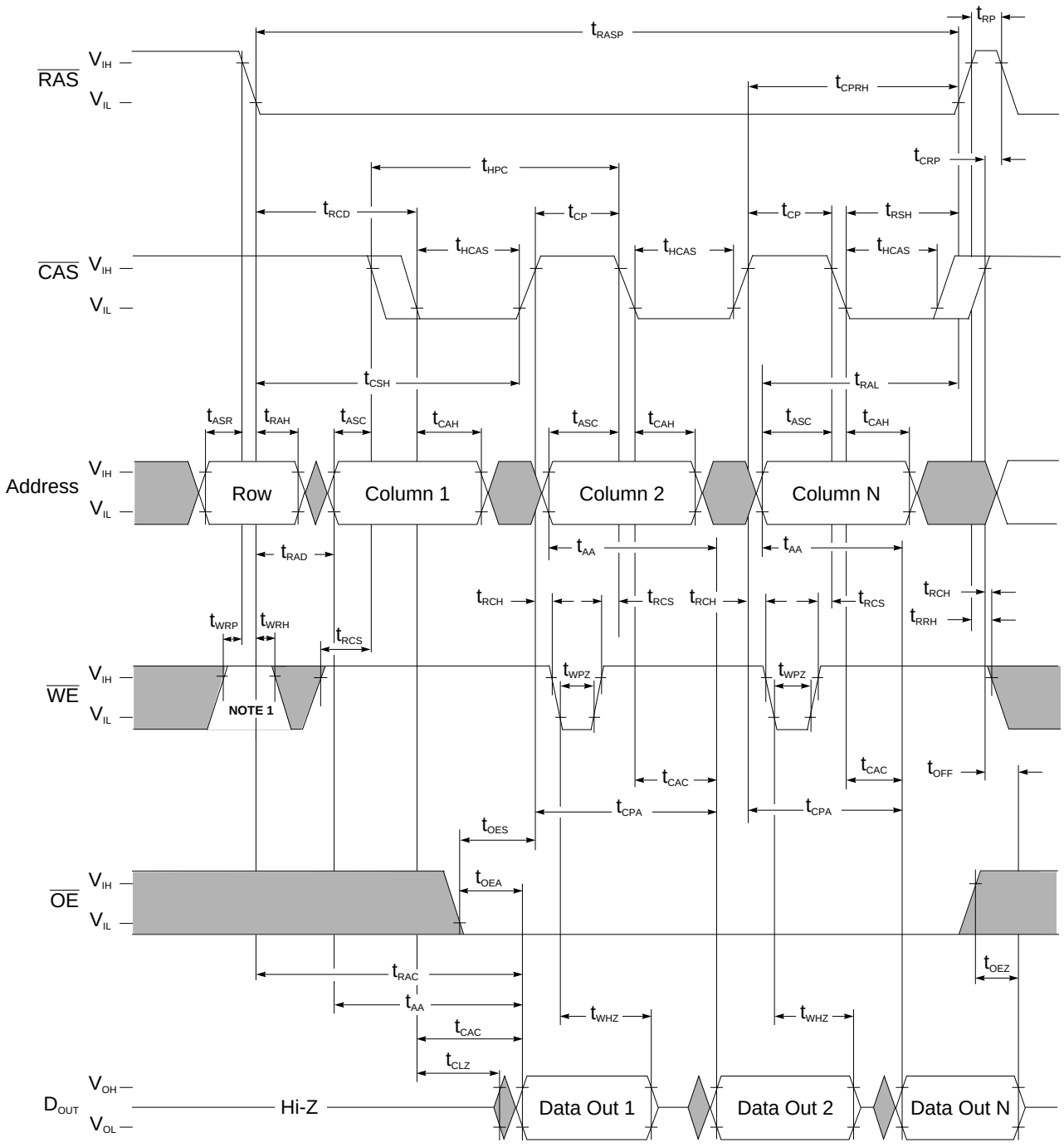
EDO Page Mode Read Cycle ($\overline{OE}$ Control)



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

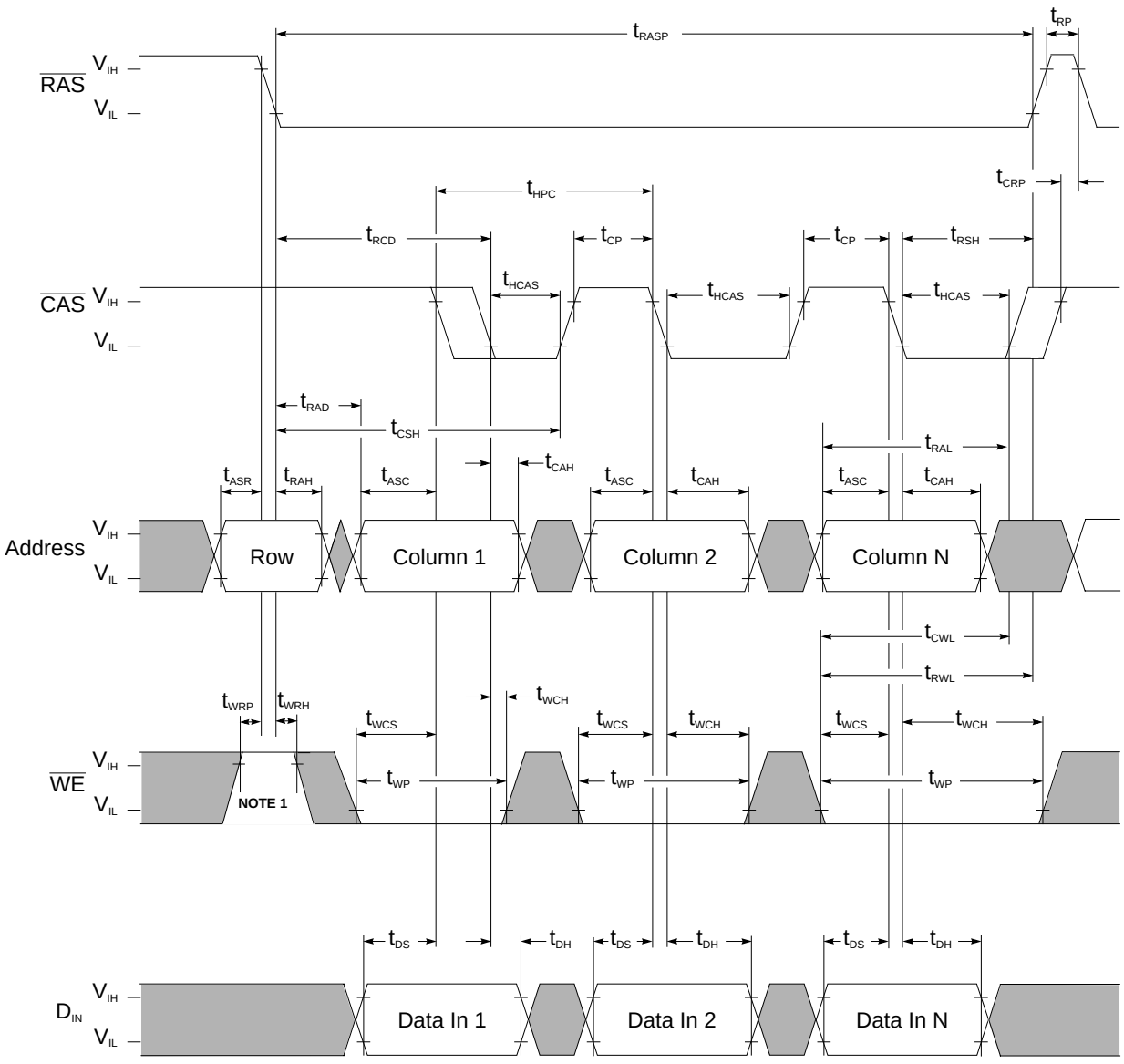
EDO Page Mode Read Cycle ($\overline{WE}$ Control)



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

EDO Page Mode Early Write Cycle

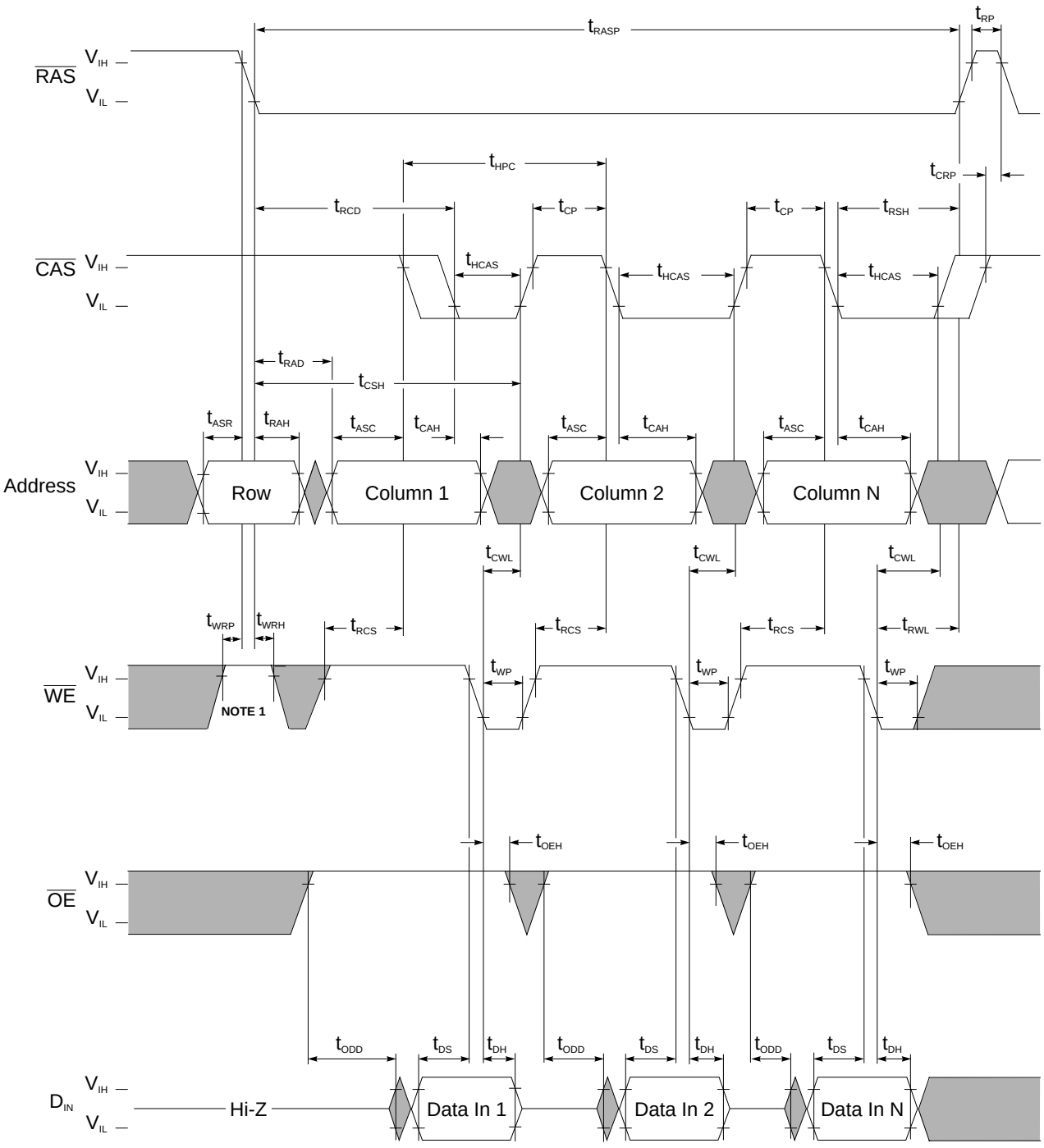


: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

$\overline{OE}$ = Don't care

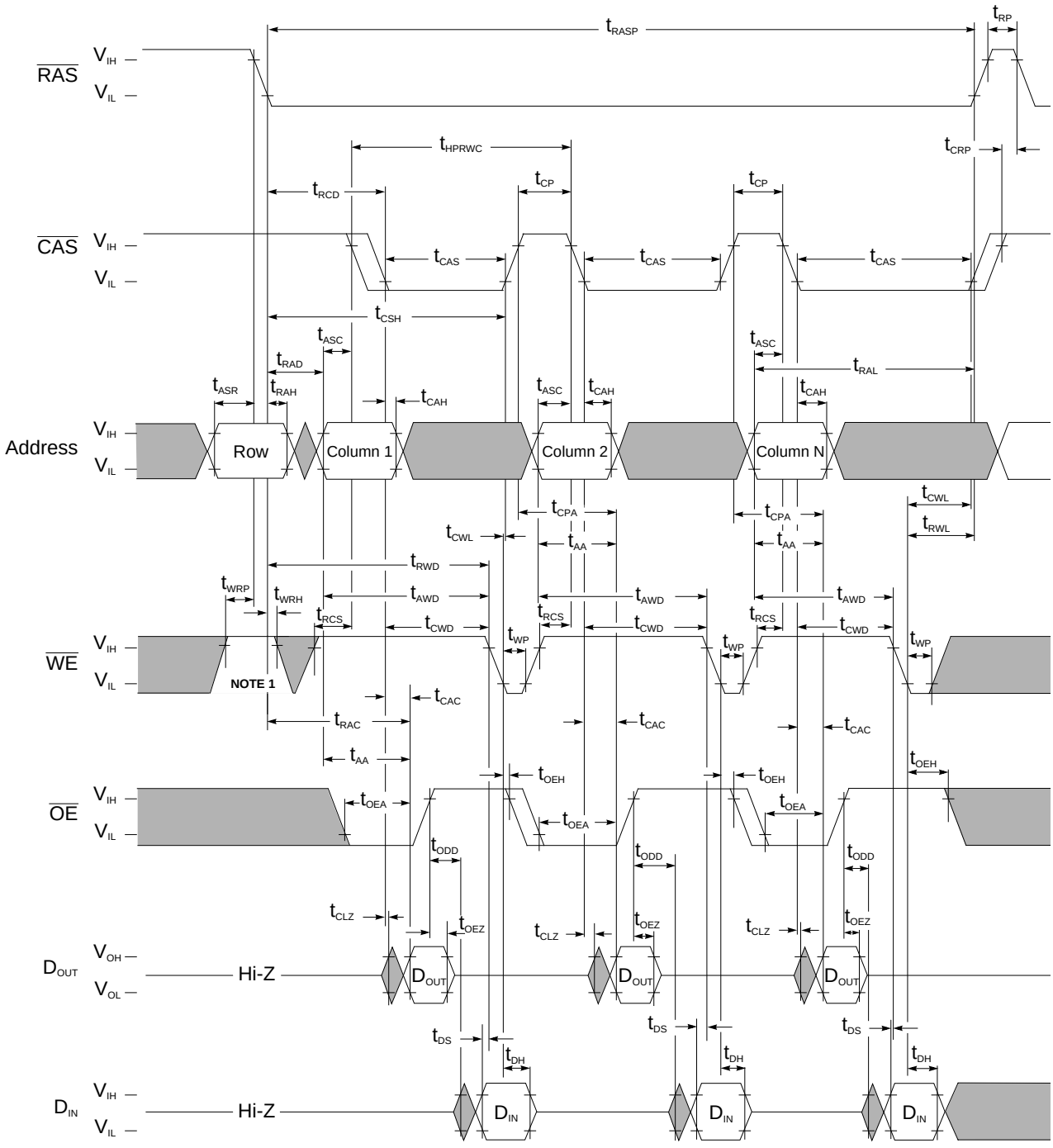
EDO Page Mode Late Write Cycle



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

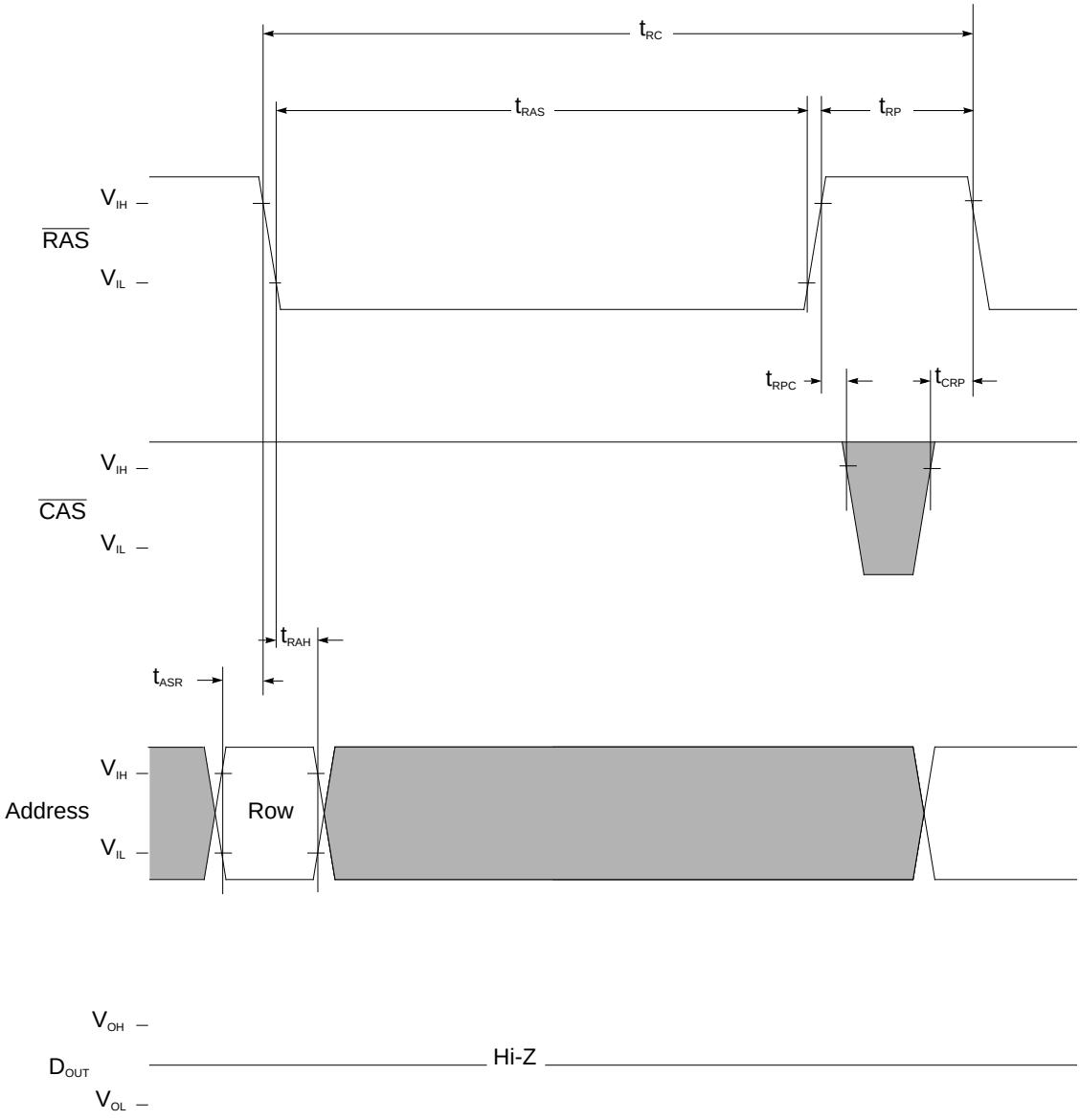
EDO Page Mode Read Modify Write Cycle



: “H” or “L”

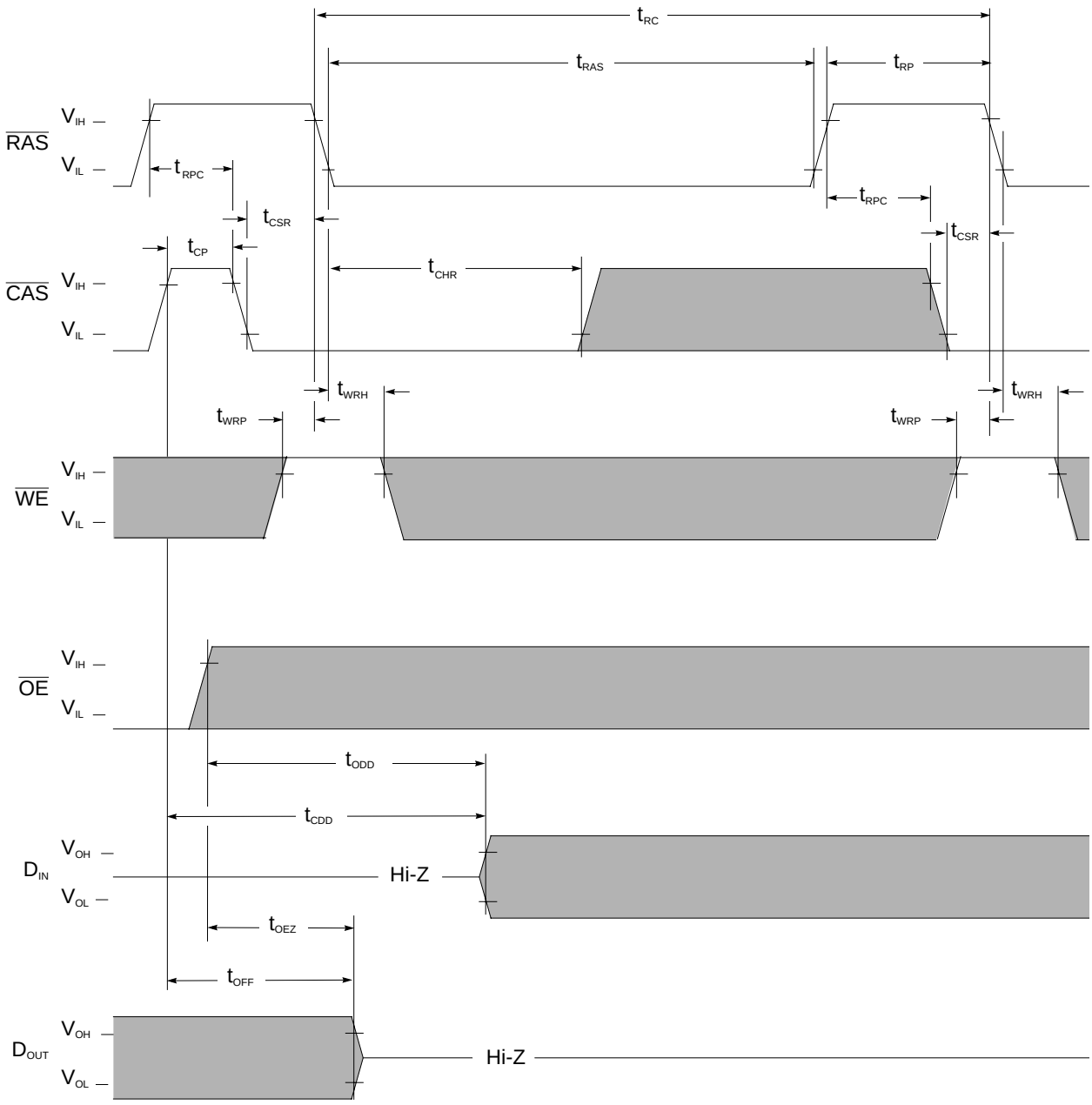
NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

$\overline{\text{RAS}}$ Only Refresh Cycle



Note: $\overline{\text{WE}}$, $\overline{\text{OE}}$, D_{IN} are “H” or “L”

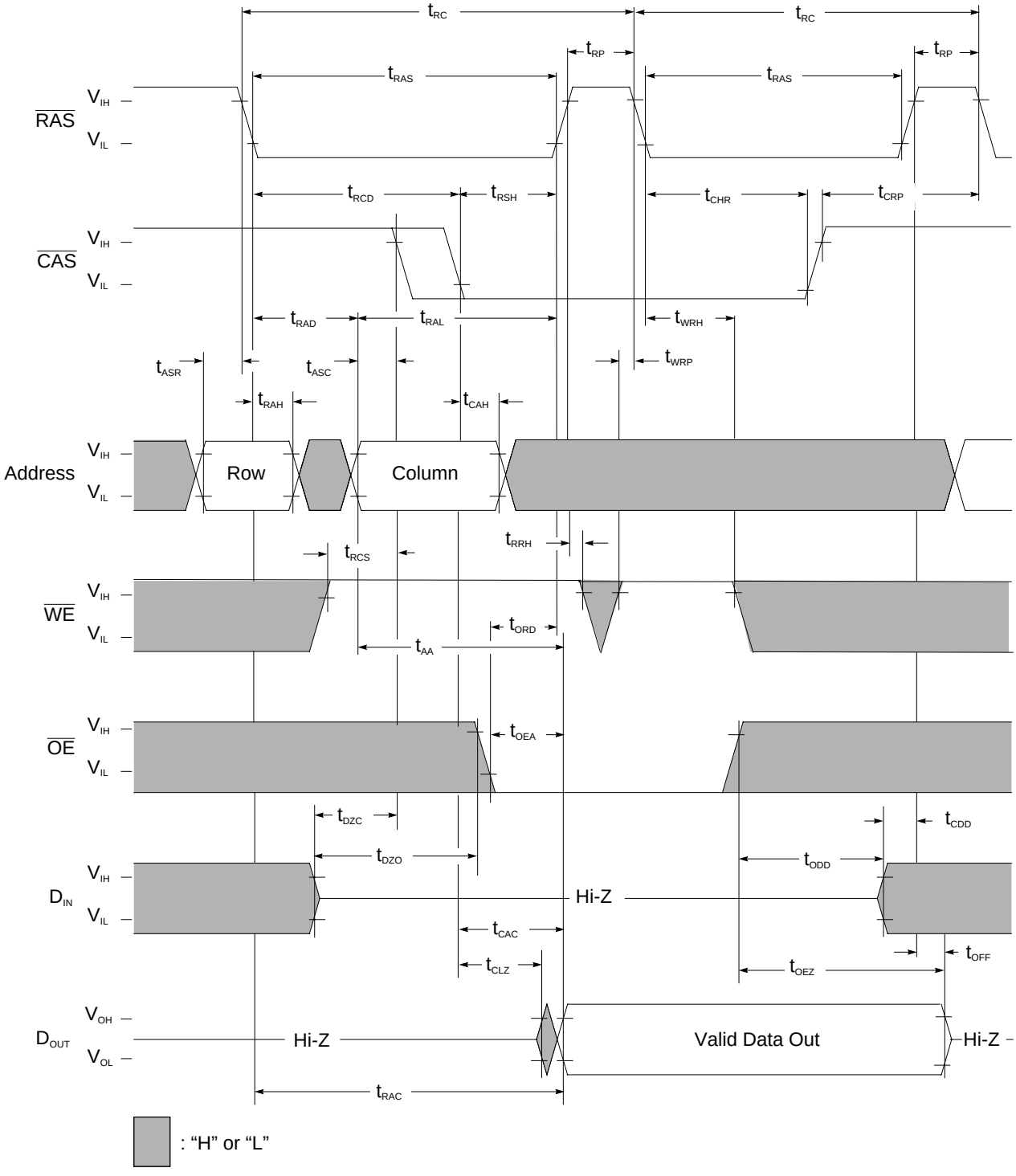
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



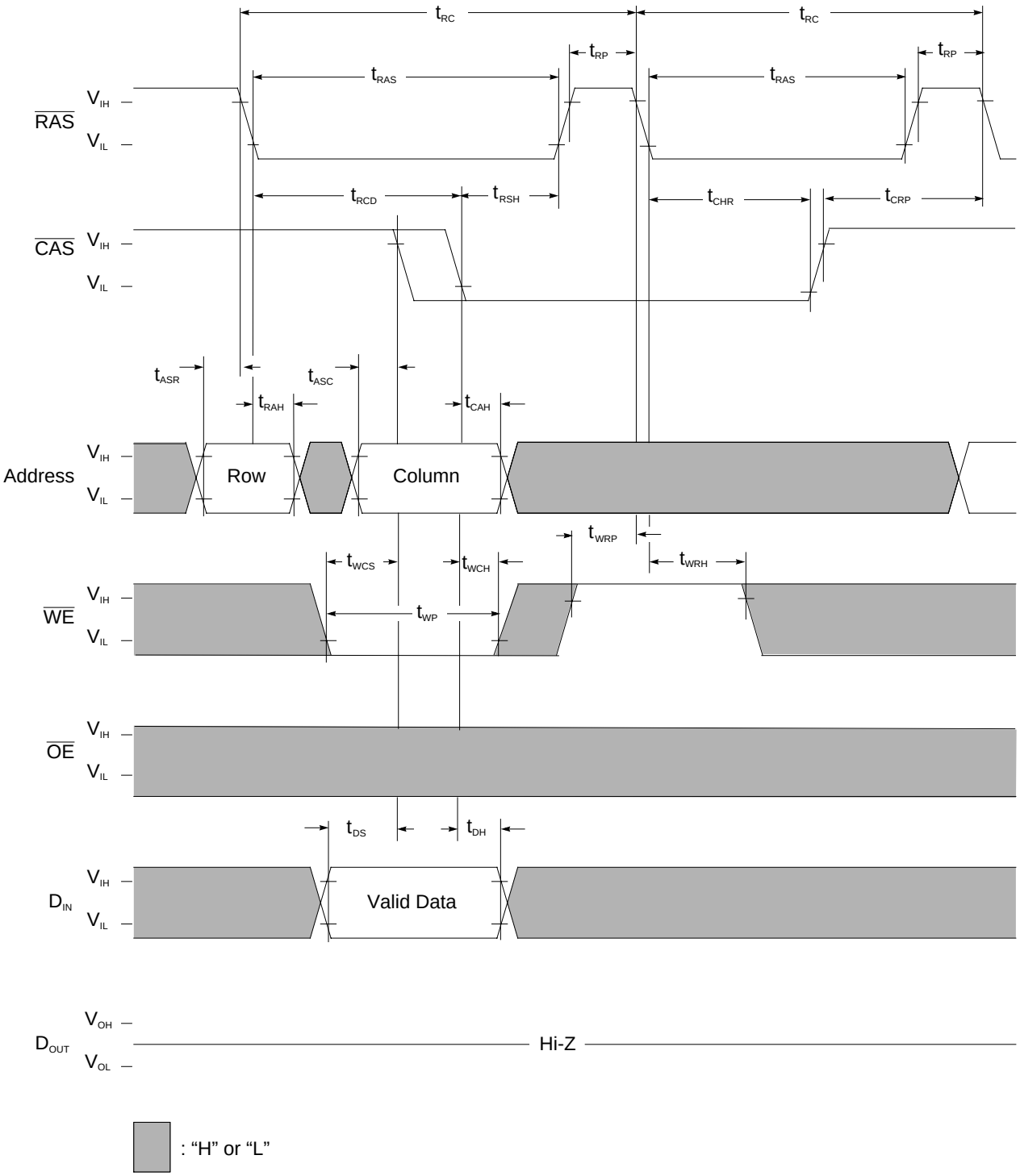
: “H” or “L”

NOTE: Address is “H” or “L”

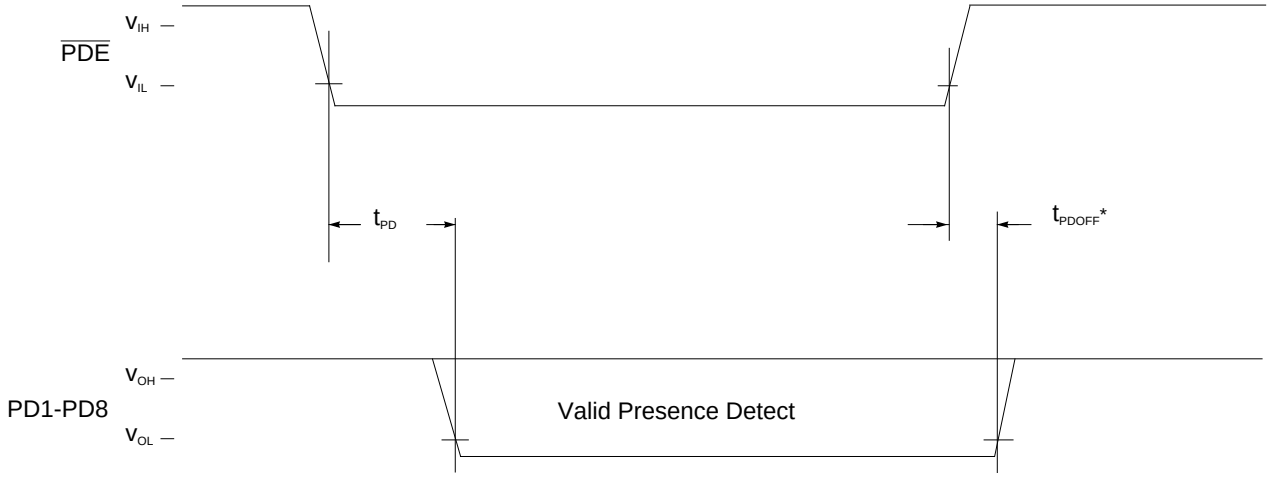
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)

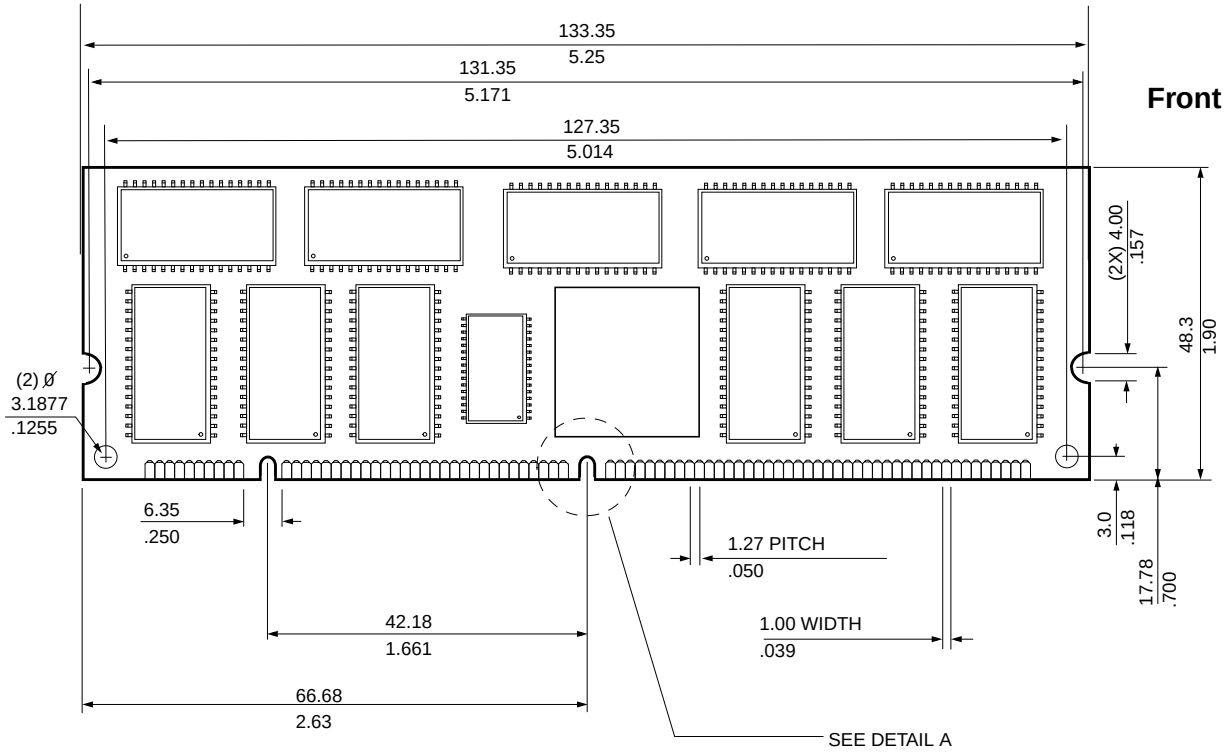


Presence Detect Read Cycle

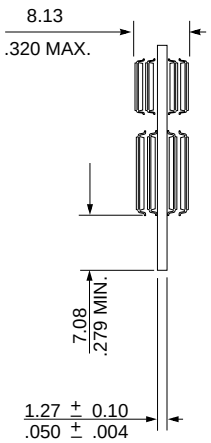


*PD pins must be pulled high at next level of assembly

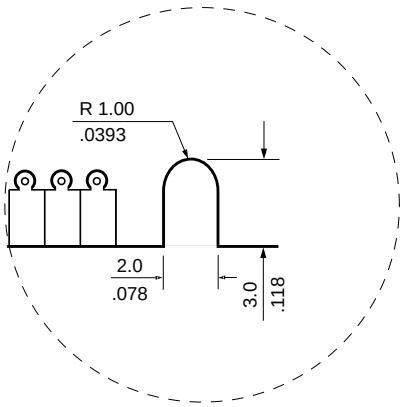
Layout Drawing



Side



Detail A
SCALE 4/1



Note: All dimensions are typical unless otherwise stated. Millimeters / Inches

Revision Log

Rev	Contents of Modification
8/98	Initial release.

Discontinued (7/00 - last order; 9/00 - last ship)

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