PRELIMINARY

Integrated Circuit Systems, Inc.

ICS8431-01
CLOCK SYNTHESIZER

GENERAL DESCRIPTION

The ICS8431-01 is a general purpose clock frequency synthesizer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8431-01 consists of one independent low bandwidth PLL timing channel. A 16.666MHz crystal is used as the input to the on-chip oscillator. The M and N dividers are configured to produce a fixed output frequency of 200MHz.

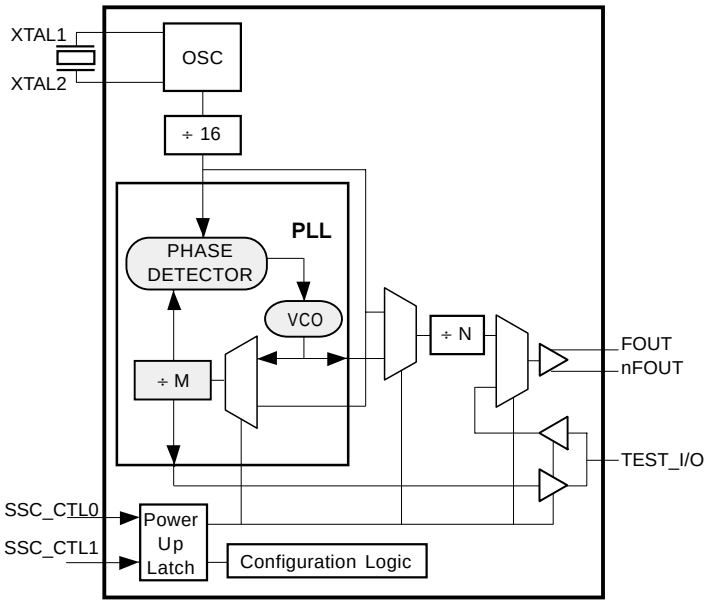
Programmable features of the ICS8431-01 support four operational modes. The four modes are spread spectrum clocking (SSC), non-spread spectrum clock and two test modes and are controlled by the Power Up Latch. After power up the latch is disabled and the initial programmed values can only be overwritten by removing all power to the device.

In SSC mode the output clock is modulated in order to achieve a reduction in EMI. In one of the PLL bypass test modes the PLL is disconnected as the source to the differential output allowing an external source to be connnected to the TEST_I/O pin. This is useful for in-circuit testing and allows the differential output to be driven at a lower frequency throughout the system clock tree. In the other PLL bypass mode the oscillator divider is used as the source to both the M and N dividers. In this configuration the frequency at FOUT, nFOUT equals the crystal frequency divide by 16 divided by N. The frequency at TEST I/O equals the crystal frequency divide by 16 divided by M. This is useful for characterizing the oscillator and internal dividers.

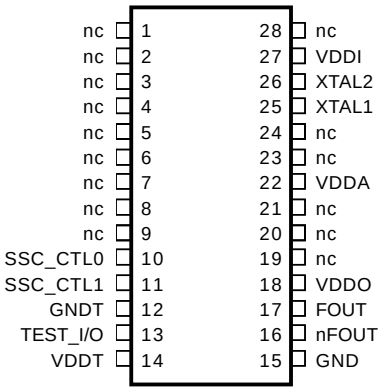
FEATURES

- Fully integrated PLL
- Differential 3.3V LVPECL output
- 200MHz output frequency
- Crystal oscillator interface
- Spread Spectrum Clocking (SSC) fixed at 1/2% modulation for environments requiring ultra low EMI
- LVTTL / LVCMOS control inputs
- PLL bypass modes supporting in-circuit testing and on-chip functional block characterization
- 28 lead SOIC

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS8431-01

28-Lead SOIC
M Package
Top View

CONFIGURATION PROGRAMMING INTERFACE

Programming the Spread Spectrum Clocking (SSC) feature is accomplished by configuring the internal PUL register. The input to this register is encoded by the SSC_CTL[1:0] pins which define all functional states after power is applied. Figure 1 shows the timing relationship of the latched SSC_CTL[1:0] in relationship to the PLL power-on condition.

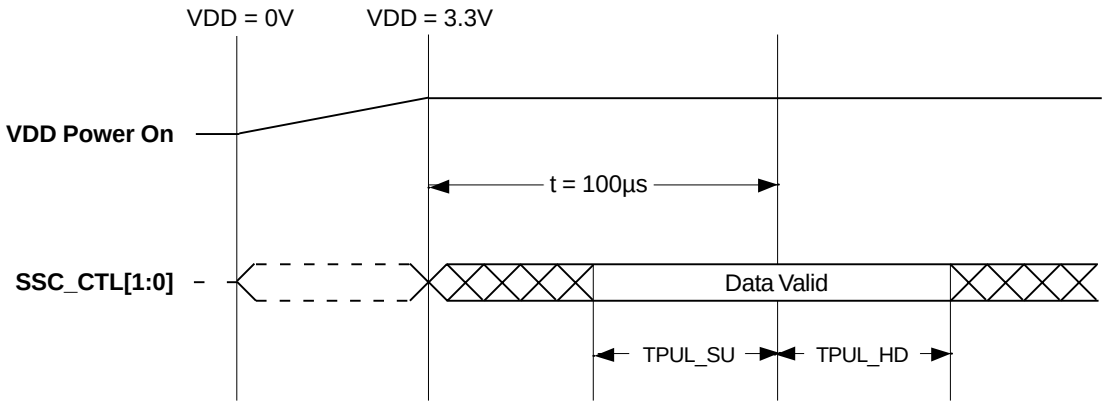


FIGURE 1. POWER-UP CONFIGURATION TIMING

After power is applied, the control bits SSC_CTL0 and SSC_CTL1 are latched after approximately 100µs. TPUL_SU is the time during which the data on the control bits is required to be valid before being latched. TPUL_HD is the time after the data is latched that the control bits are required to remain valid. The configuration latch can only be overwritten by removing the power and applying data to the inputs that meet the setup and hold time requirment during power-on, as defined in Figure 1. Table 3, Input Function Table defined the valid commands for SSC_CTL[1:0] lines.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1 -9, 19, 20, 21, 23, 24, 28	nc	Unused		No connection.
10, 11	SSC CTL 0, SSC CTL 1	Input	Pullup	These LVCMOS / LVTTL pins are sampled during power-up to configure the SSC control. After power-up inputs have no effect on the latched configuration register.
12	GNDT	Power		Ground pin for core and test output.
13	TEST I/O	Input / Output		Programmed asdefined in Table 3, Function Table.
14	VDDT	Power		Power supply pin for test output.
15	GND	Power		Ground pin for output.
16, 17	nFOUT, FOUT	Output		These differential outputs are main output drivers for the synthesizer. They are compatible with terminated positive referenced LVPECL logic.
18	VDDO	Power		Power supply pin for output.
22	VDDA	Power		PLL power supply pin.
27	VDDI	Power		Power supply pin for core.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
RPULLUP	Input Pullup Resistor			51		KΩ
RPULLDOWN	Input Pulldown Resistor			51		KΩ

TABLE 3. FUNCTION TABLE

Inputs		TEST_I/O Source	SSC	Outputs		Operational Modes
SSC_CTL1	SSC_CTL0			FOUT, nFOUT	TEST_I/O	
0	0	Internal	Disabled	fXTAL ÷ 16 ÷ N	fXTAL ÷ 16 ÷ M	PLL bypass; Oscillator, oscillator, M and N dividers test mode. NOTE 1
0	1	PLL	Enabled	200MHz	Hi-Z	Default SSC; Modulation Factor = ½ Percent
1	0	External	Disabled	Test Clk	Input	PLL Bypass Mode, (1MHz ≤ Test Clk ≤ 200MHz)
1	1	PLL	Disabled	200MHz	Hi-Z	No SSC Modulation

NOTE 1: Used for in house debug and characterization.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	4.6V
Inputs	-0.5V to VDD + 0.5V
Outputs	-0.5V to VDDO + 0.5V
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of product at these condition or any conditions beyond those listed in the *DC Electrical Characteristics* or *AC Electrical Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. LVTTL, LVCMOS DC ELECTRICAL CHARACTERISTICS, VDDA, VDDI=VDDO=VDDT=3.3V±5%, T_A=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VDDA, VDDI, VDDO, VDDT	Power Supply Voltage			3.135	3.3	3.465	V
VIH	Input High Voltage	SSC_CTL0, SSC_CTL1	VDDI = 3.465V	2		3.765	V
		TEST_I/O	VDDI = 3.465V	2		3.765	V
VIL	Input Low Voltage	SSC_CTL0, SSC_CTL1	VDDI = 3.135V	-0.3		0.8	V
		TEST_I/O	VDDI = 3.135V			1.3	V
IIH	Input High Current	SSC_CTL0, SSC_CTL1	VDDI = VIN = 3.465V			50	µA
		TEST_I/O	VDDI = VIN = 3.465V			50	µA
IIL	Input Low Current	SSC_CTL0, SSC_CTL1	VDDI = 3.465V, VIN = 0V	-150			µA
		TEST_I/O	VDDI = 3.465V, VIN = 0V	-50			µA

TABLE 4B. LVPECL DC ELECTRICAL CHARACTERISTICS, VDDA, VDDI=VDDO=VDDT=3.3V±5%, T_A=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VOH	Output High Voltage; NOTE 1, 2	VDDI = VDDO = 3.3V	2.1		2.2	V
VOL	Output Low Voltage; NOTE 1, 2	VDDI = VDDO = 3.3V	1.4		1.5	V
VSWING	Common Mode Voltage Range		600	700	800	mV
IOH	Output High Current		16		18	mA
IOL	Output Low Current		2		4	mA

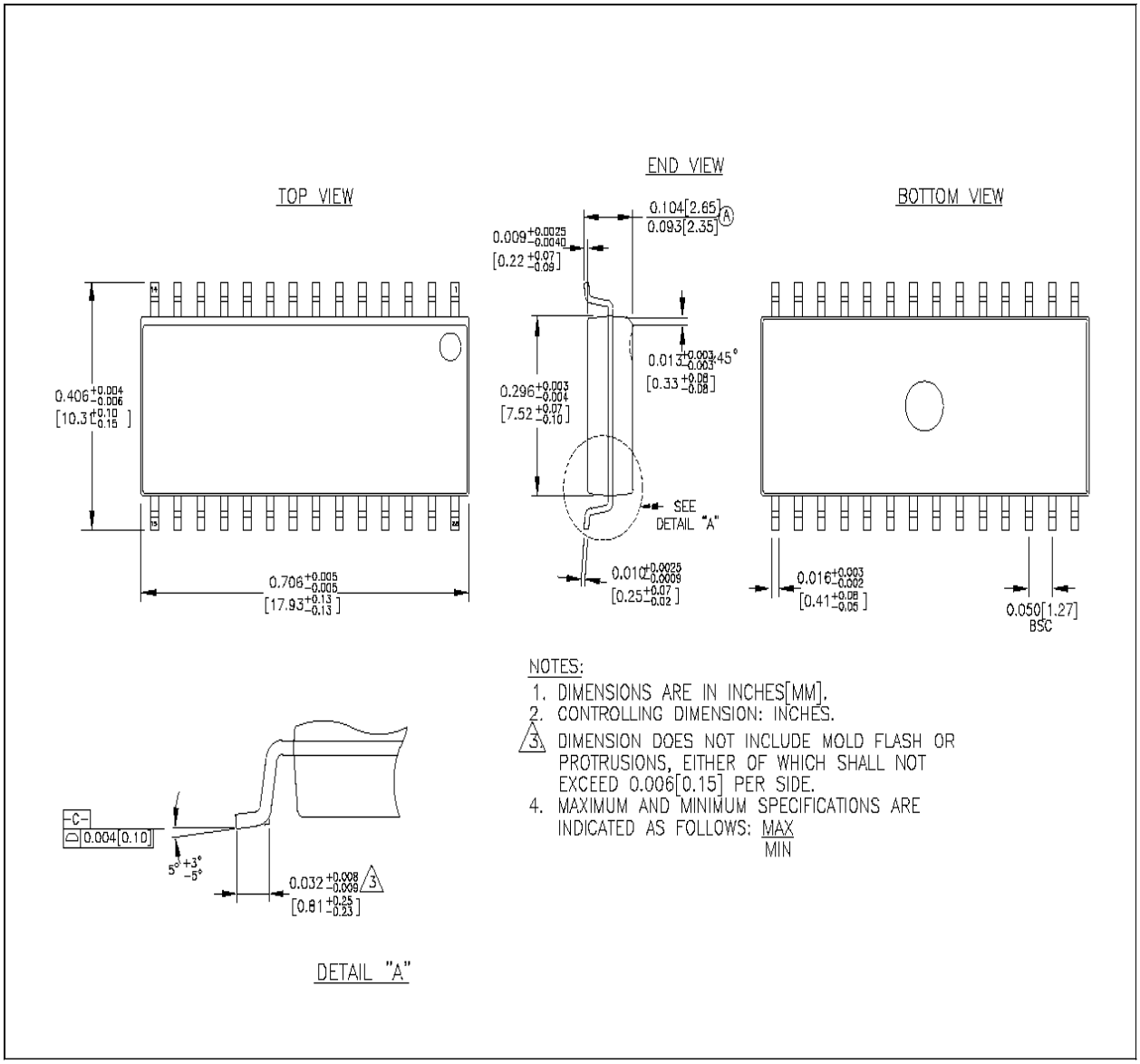
NOTE 1: These values are for VDDO equal to 3.3V. Output levels will vary 1:1 with VDDO.
NOTE 2: Output terminated with 50Ω to VDDO - 2V.

TABLE 5. AC ELECTRICAL CHARACTERISTICS, VDDI=VDDO=3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
tPERIOD	Output Period; NOTE 1	fout = 200MHz	4995		5005	ps
tjit	Peak Jitter (Short Cycle); NOTE 1	fout = 200MHz			50	ps
tDC	Output Duty Cycle; NOTE 1	fout = 200MHz	47		53	%
tR	Output Rise Time	20% to 80%	300		800	ps
tF	Output Fall Time	20% to 80%	300		800	ps
Fxtal	Crystal Input Range		14		18	MHz
Fm	SSC Modulation Frequency		30		33.33	KHz
Fmf	SSC Modulation Factor		0.5			%
tSTABLE	Power-up to Stable Clock Output				TBD	µs
tPUL_SU	Configuration Latch Setup Time		10			ns
tPUL_HD	Configuration Latch Hold Time		0			ns

NOTE 1: Spread spectrum clocking enabled

PACKAGE OUTLINE AND DIMENSIONS - M SUFFIX



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.15] PER SIDE.
4. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX / MIN

ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8431AM-01	ICS8431AM-01	28 Lead SOIC		0°C to 70°C
ICS8431AM-01T	ICS8431AM-01	28 LeadSOIC on Tape and Reel		0°C to 70°C