MICROCLOCK

ICS504

Intel i740™ Graphics Clock Source

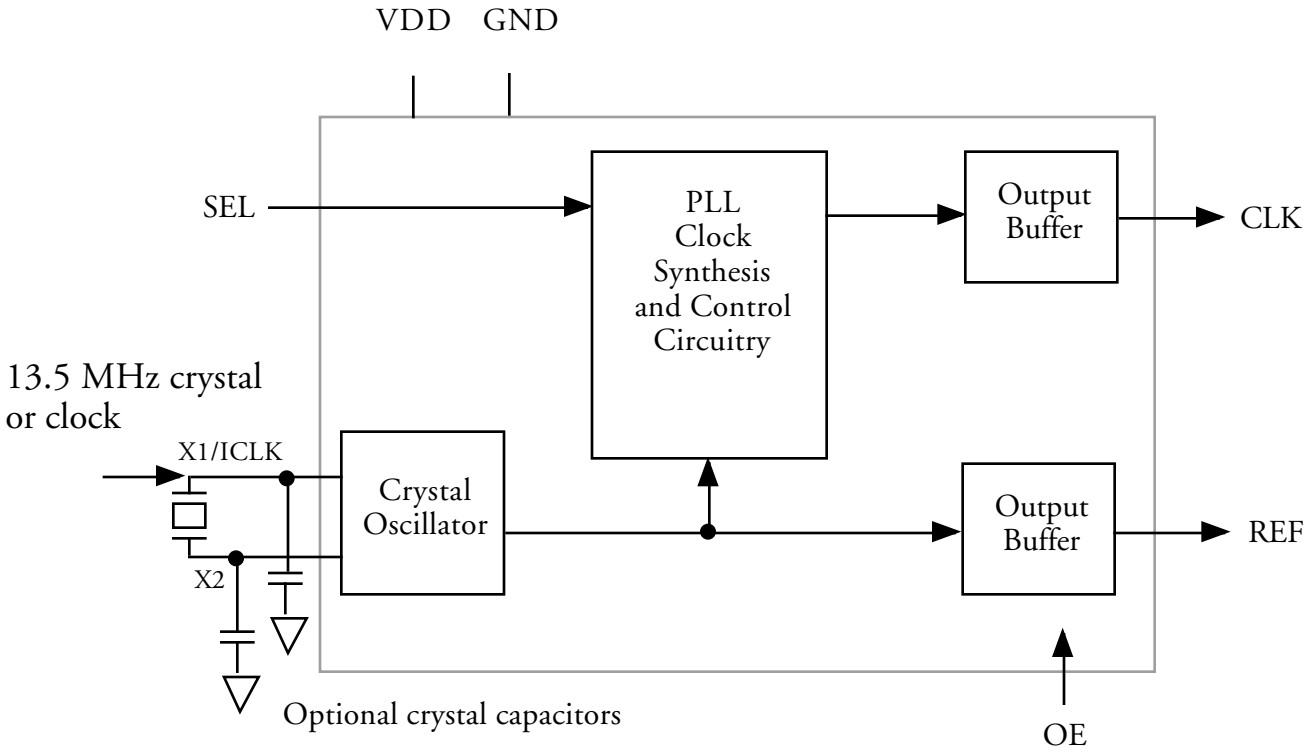
Description

The ICS504 is the most cost effective way to generate a high quality, high frequency clock for Intel's i740 graphics controller. It also provides a 13.5 MHz clock output for the video encoder. Using Phase-Locked-Loop (PLL) techniques, the device uses a standard fundamental mode, inexpensive crystal to produce a selectable output clock.

Features

- Packaged as 8 pin SOIC or die
- Compatible with Intel i740 graphics controller
- ICS' lowest cost PLL clock plus reference
- Zero ppm synthesis error
- Input frequency of 13.5 MHz
- Output clock frequencies of 48 or 66.67 MHz plus 13.5 MHz Reference output
- Low jitter - 50 ps one sigma
- Operating voltages of 3.0 to 5.5V
- Full CMOS-level outputs with 25mA drive capability at TTL levels
- Advanced, low power CMOS process

Block Diagram



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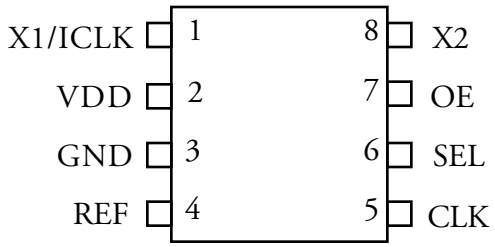
Pin Assignment



Clock Decoding Table (MHz)

SEL	CLK
0	48 MHz
1	66.67 MHz

0 = connect directly to ground.
1 = connect directly to VDD.

Pin Descriptions

Number	Name	Type	Description
1	X1/ICLK	I	Crystal connection for 13.50 MHz crystal, or clock input.
2	VDD	P	Connect to +3.3V or +5V.
3	GND	P	Connect to ground.
4	REF	O	Buffered crystal oscillator output clock.
5	CLK	O	48.0 or 66.667 MHz clock output per Table above.
6	SEL	I	Select pin for output clock on pin 5. Connect to GND or VDD. Internal pull-up.
7	OE	I	Output Enable. Tri-states CLK and REF outputs when low. Internal pull-up.
8	X2	O	Crystal connection for 13.50 MHz crystal. Leave unconnected for clock input.

Key: I = Input, O = output, P = power supply connection

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Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (note 1)					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	-0.5		VDD+0.5	V
Clock Output	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 3.3 V unless otherwise noted)					
Operating Voltage, VDD		3		5.5	V
Input High Voltage, VIH, ICLK only	ICLK (Pin 1)	(VDD/2)+1	VDD/2		V
Input Low Voltage, VIL, ICLK only	ICLK (Pin 1)		VDD/2	(VDD/2)-1	V
Input High Voltage, VIH	Pins 6 and 7	2			V
Input Low Voltage, VIL	Pins 6 and 7			0.8	V
Input High Voltage, VOH	IOH = -4 mA	VDD-0.5			V
Output High Voltage, VOH	IOH=-25mA	2.4			V
Output Low Voltage, VOL	IOL=25mA			0.4	V
IDD Operating Supply Current	No load		15		mA
Short Circuit Current	CLK output		±40		mA
On-Chip Pull-up Resistor, SEL and OE	Pins 6 and 7		270		kΩ
Input Capacitance, SEL and OE	Pins 6 and 7		4		pF
AC CHARACTERISTICS (VDD = 3.3 V unless otherwise noted)					
Input Frequency, crystal input			13.5		MHz
Input Frequency, clock input			13.5		MHz
Actual mean frequency error vs target	48.0, 66.667 MHz			0	ppm
Output Clock Rise Time	0.8 to 2.0V		1		ns
Output Clock Fall Time	2.0 to 0.8V		1		ns
Output Clock Duty Cycle	at VDD/2	40		60	%
Absolute Clock Period Jitter	Deviation from mean		±120		ps
One Sigma Clock Period Jitter			50		ps

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
2. Typical values are at 25°C.

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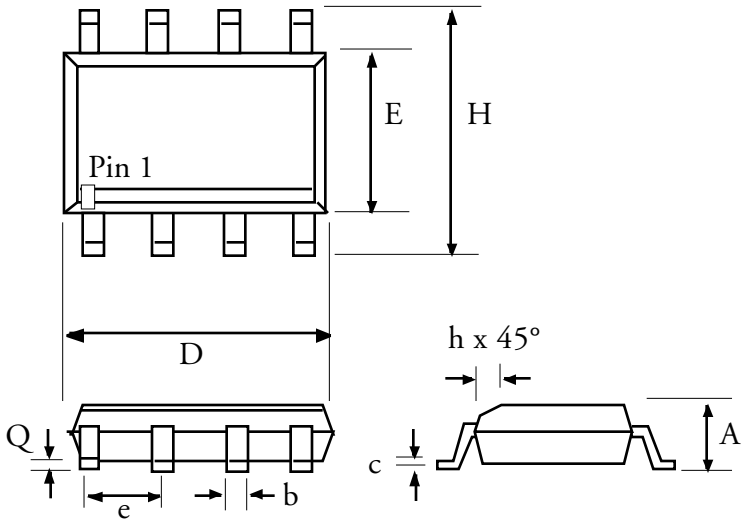
External Components / Crystal Selection

The ICS504 requires a 0.01µF decoupling capacitor to be connected between VDD and GND. It must be connected close to the ICS504 to minimize lead inductance. No external power supply filtering is required for this device. A 33Ω terminating resistor can be used next to the CLK pin. The total on-chip crystal capacitance is approximately 13 pF, and a parallel resonant, fundamental mode crystal should be used. For crystals with a specified load capacitance greater than 13 pF, crystal capacitors should be connected from each of the pins X1 and X2 to Ground as shown in the Block Diagram on page 1. The value (in pF) of these crystal caps should be = $(C_L-13)*2$, where C_L is the crystal load capacitance in pF. These external capacitors are only required for applications where the exact frequency is critical. For a clock input, connect to X1 and leave X2 unconnected (no capacitors on either).

Package Outline and Package Dimensions



8 pin SOIC

	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.055	0.068	1.397	1.7272
b	0.013	0.019	0.330	0.483
D	0.185	0.200	4.699	5.080
E	0.150	0.160	3.810	4.064
H	0.225	0.245	5.715	6.223
e	.050 BSC		1.27 BSC	
h		0.015		0.381
Q	0.004	0.01	0.102	0.254

Ordering Information

Part/Order Number	Marking	Package	Temperature
ICS504M	ICS504M	8 pin SOIC	0-70°C
ICS504MT	ICS504M	8 pin SOIC on tape and reel	0-70°C