



**Integrated  
Circuit  
Systems, Inc.**

## ICS8520 Low SKEW 1-TO-16 LVHSTL FANOUT BUFFER

### GENERAL DESCRIPTION



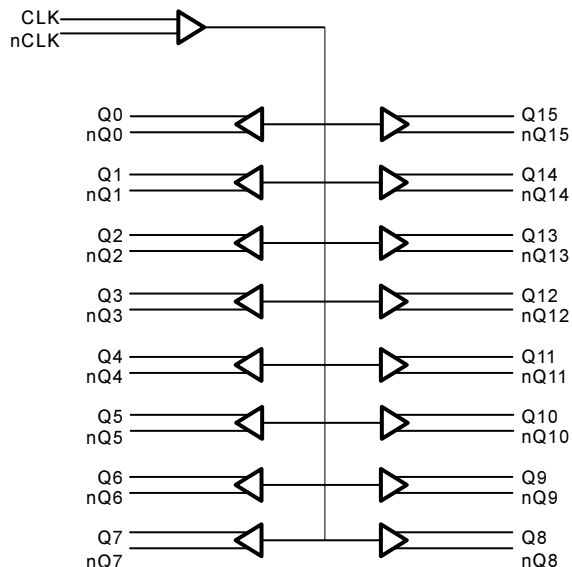
The ICS8520 is a very low skew, 1-to-16 LVHSTL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8520 is designed to translate any differential signal levels to LVHSTL (Low Voltage High Speed Transceiver Logic) levels.

Guaranteed output skew, part-to-part skew and crossover voltage characteristics make the ICS8520 ideal for interfacing to today's most advanced microprocessor and static RAMs.

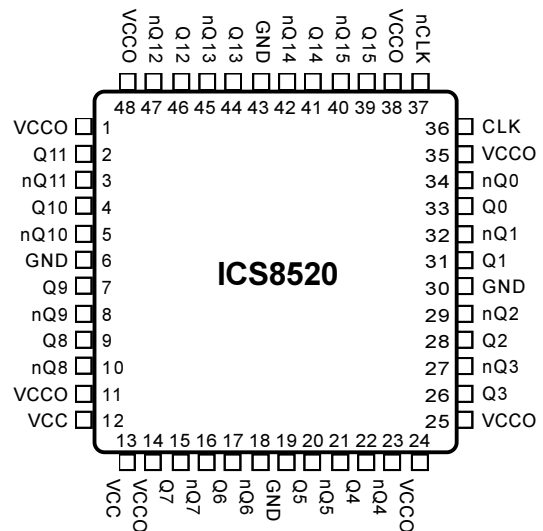
### FEATURES

- 16 LVHSTL outputs each with the ability to drive 50Ω to ground
- Differential clock input
- Translates any differential input signal (PECL, SSTL, LVDS) to LVHSTL levels without external bias networks
- Translates single ended input levels to LVHSTL levels with resistor bias nCLK input
- Translates single ended input levels to inverted LVHSTL levels with resistor bias CLK input
- $V_{oh(max)} = 1.2V$
- $40\% \text{ of } V_{oh} \leq V_{crossover} \leq 60\% \text{ of } V_{oh}$
- Output frequency up to 500MHz
- 25ps output skew, typical
- 3.3V core, 1.8V output operating supply voltages
- 48 lead low-profile QFP (LQFP), 7mm x 7mm x 1.4mm package body, 0.5mm package lead pitch
- 0°C to 70°C ambient operating temperature

### BLOCK DIAGRAM



### PIN ASSIGNMENT



**48-Lead LQFP  
Y Package  
Top View**

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.



**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1, 11, 14, 24, 25, 35, 38, 48	VCCO	Power		Output power supply pin. Connect to 1.8V.
2, 3	Q11, nQ11	Output		Differential output. LVHSTL interface levels.
4, 5	Q10, nQ10	Output		Differential output. LVHSTL interface levels.
6, 19, 30, 43	GND	Power		Power supply pin. Connect to ground.
7, 8	Q9, nQ9	Output		Differential output. LVHSTL interface levels.
9, 10	Q8, nQ8	Output		Differential output. LVHSTL interface levels.
12, 13	VCC	Power		Core power supply pin. Connect to 3.3V.
15, 16	Q7, nQ7	Output		Differential output. LVHSTL interface levels.
17, 18	Q6, nQ6	Output		Differential output. LVHSTL interface levels.
20, 21	Q5, nQ5	Output		Differential output. LVHSTL interface levels.
22, 23	Q4, nQ4	Output		Differential output. LVHSTL interface levels.
26, 27	Q3, nQ3	Output		Differential output. LVHSTL interface levels.
28, 29	Q2, nQ2	Output		Differential output. LVHSTL interface levels.
36	CLK	Input	Pulldown	Non inverting differential clock input. Any differential input interface levels.
37	nCLK	Input	Pullup	Inverting differential clock input. Any differential input interface levels.
39, 40	Q15, nQ15	Output		Differential output. LVHSTL interface levels.
41, 42	Q14, nQ14	Output		Differential output. LVHSTL interface levels.
44, 45	Q13, nQ13	Output		Differential output. LVHSTL interface levels.
46, 47	Q12, nQ12	Output		Differential output. LVHSTL interface levels.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Capacitance			TBD		pF
RPULLUP	Input Pullup Resistor			51		K $\Omega$
RPULLDOWN	Input Pulldown Resistor			51		K $\Omega$

**TABLE 3. FUNCTION TABLE**

Inputs		Outputs		Input to Output Mode	Polarity
CLK	nCLK	Q0 thru Q15	nQ0 thru nQ15		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Single ended use requires that one of the differential inputs be biased. The voltage at the biased input sets the switch point for the single ended input. For LVCMOS and LVTTTL levels the recommended input bias network is a resistor to VCC, a resistor of equal value to ground and a 0.1 $\mu$ F capacitor from the input to ground. The resulting switch point is approximately  $VCC/2 \pm 300mV$ .



**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage	4.6V
Inputs	-0.5V to VCC+0.5 V
Outputs	-0.5V to VCC+0.5V
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any conditions beyond those listed in the *DC Electrical Characteristics* or *AC Electrical Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4. DC ELECTRICAL CHARACTERISTICS, VCC = 3.3V±5%, VCCO = 1.8V±0.2V, TA = 0°C TO 70°C**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VCC	Core Operating Supply Voltage			3.135	3.3	3.465	V
VCCO	Output Operating Supply Voltage			1.6	1.8	2.0	V
VPP	Peak-to-Peak Input Voltage			0.31		1.3	V
VCMR	Common Mode Voltage Range; NOTE 1			0.9		2	V
IIH	Input High Current	CLK	VIN = VCC = 3.465V			150	μA
		nCLK	VIN = VCC = 3.465V			1	μA
IIL	Input Low Current	CLK	VIN = 0V, VCC = 3.465V	-1			μA
		nCLK	VIN = 0V, VCC = 3.465V	-150			μA
ICC	Input Operating Supply Current					TBD	mA
VOH	Output High Voltage		VCCO = 2.0V	1.0		1.2	V
VOL	Output Low Voltage		VCCO = 2.0V	0		0.4	V

NOTE 1: Common mode voltage for LVPECL is defined as the minimum VIH. Common mode voltage for HSTL, LVDS and SSTL is defined as the crossover voltage.

**TABLE 5. AC ELECTRICAL CHARACTERISTICS, VCC = 3.3V±5%, VCCO = 1.8V±0.2V, TA = 0°C TO 70°C**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Input Frequency				500	MHz
tpLH	Propagation Delay, Low-to-High	0 < f ≤ 250MHz	1		1.3	ns
tpHL	Propagation Delay, High-to-Low	0 < f ≤ 250MHz	1		1.3	ns
tsk(o)	Output Skew; NOTE 3			25	TBD	ps
tsk(pp)	Part-to-Part Skew; NOTE 4				TBD	ps
tR	Output Rise Time		300		700	ps
tF	Output Fall Time		300		700	ps
tPW	Output Pulse Width		tCYCLE/2 - TBD	tCYCLE/2	tCYCLE/2 + TBD	ns
VOX	Output Crossover Voltage		40% x (VOH-VOL) + VOL		60% x (VOH-VOL) + VOL	V

NOTE 1: All parameters measured at 250MHz unless noted otherwise.

NOTE 2: Outputs terminated with 50Ω resistor connected to ground.

NOTE 3: Defined as skew across outputs at the same supply voltages and with equal load conditions. Measure from the differential input crossing point to the differential output crossing point.

NOTE 4: Defined as skew at different outputs on different devices operating at the same supply voltages and with equal load conditions.



FIGURE 1A, 1B, 1C - INPUT CLOCK WAVEFORMS

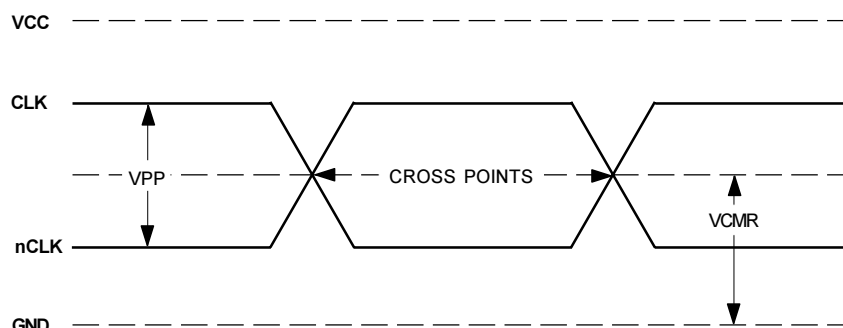


FIGURE 1A - LVDS, HSTL, SSTL DIFFERENTIAL INPUT LEVELS

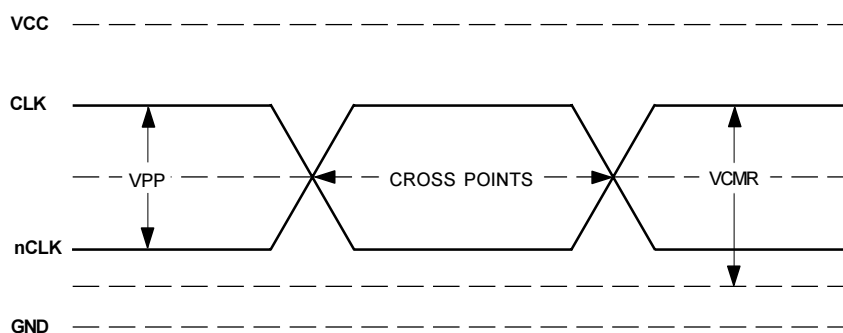


FIGURE 1B - LVPECL DIFFERENTIAL INPUT LEVEL

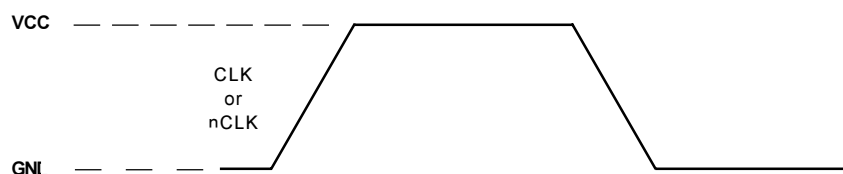
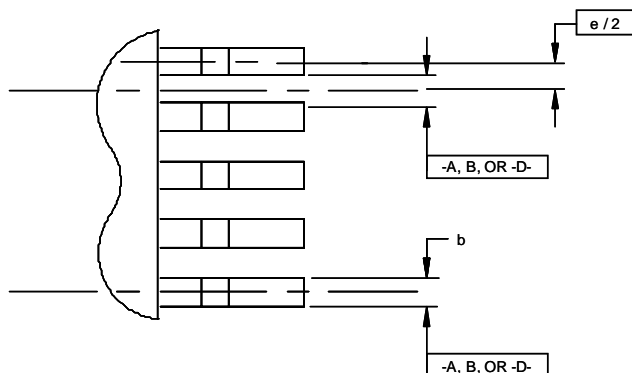
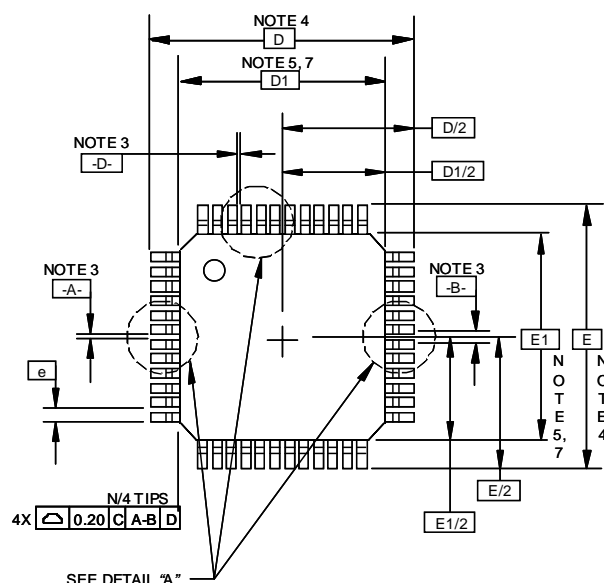


FIGURE 1C - LVCMOS AND LVTTTL SINGLE ENDED INPUT LEVEL

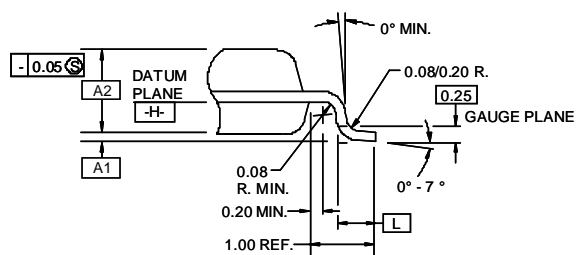
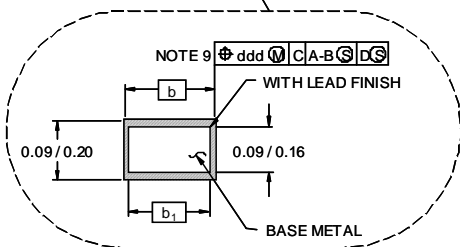
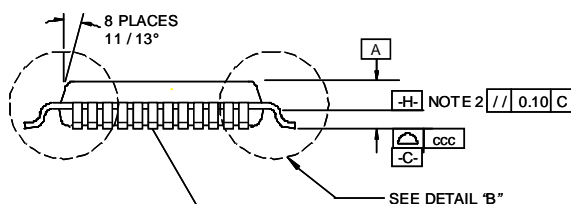


### PACKAGE OUTLINE AND DIMENSIONS - Y SUFFIX



#### NOTES:

- ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982
- DATUM PLANE -H- LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
- DATUMS -A- AND -B- TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC AT DATUM PLANE -H-.
- TO BE DETERMINED AT SEATING PLACE -C-.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
- "N" IS THE TOTAL NUMBER OF TERMINALS.
- THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H-.
- PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
- CONTROLLING DIMENSION: MILLIMETER.
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026, VARIATION BBC.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE.



SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			NOTE
	BBC			
	MIN.	NOM.	MAX.	
A			1.60	12
A <sub>1</sub>	0.05		0.15	
A <sub>2</sub>	1.35	1.40	1.45	
D	9.00 BSC.			4
D <sub>1</sub>	7.00 BSC.			7, 8
E	9.00 BSC.			4
E <sub>1</sub>	7.00 BSC.			7, 8
L	0.45	0.60	0.75	9
N		48		
e	0.5 BSC.			
b	0.17	0.22	0.27	
b <sub>1</sub>	0.17	0.20	0.23	
ccc			0.08	
ddd			0.08	



**Integrated  
Circuit  
Systems, Inc.**

# **ICS8520**

## **LOW SKEW 1-TO-16**

### **LVHSTL FANOUT BUFFER**

#### **ORDERING INFORMATION**

<b>Part/Order Number</b>	<b>Marking</b>	<b>Package</b>	<b>Count</b>	<b>Temperature</b>
ICS8520CY	ICS8520CY	48 Lead LQFP	250 per tray	0°C to 70°C
ICS8520CYT	ICS8520CY	48 Lead LQFP on Tape and Reel	2000	0°C to 70°C

While the information presented herein has been checked for both accuracy and reliability, Integrated Circuit Systems, Incorporated (ICS) assumes no responsibility for either its use or for infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by ICS. ICS reserves the right to change any circuitry or specifications without notice. ICS does not authorize or warrant any ICS product for use in life support devices or critical medical instruments.