PRELIMINARY

Integrated Circuit Systems, Inc.

ICS8516
LOW SKEW 1-TO-16 LVDS CLOCK DISTRIBUTION CHIP

GENERAL DESCRIPTION

The ICS8516 is a low skew, high performance Clock Distribution Chip and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. Utilizing Low Voltage Differential Signaling (LVDS) the ICS8516 provides a low power, low noise, point-to-point solution for distributing clock signals over controlled impedances of 100Ω.

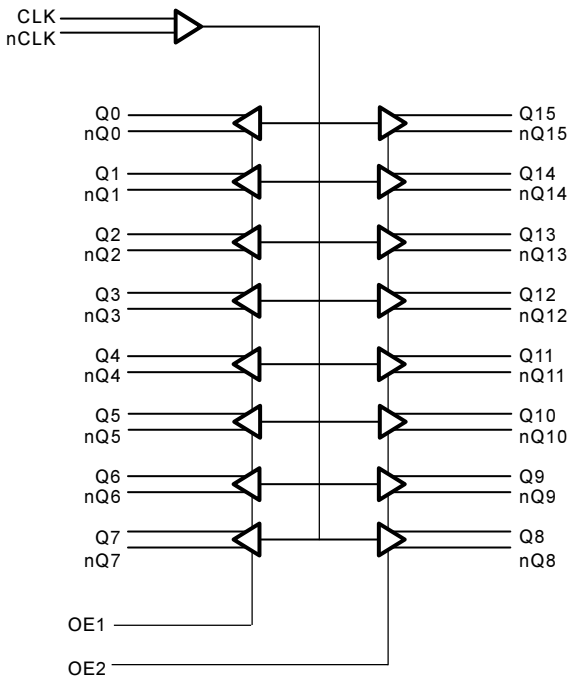
The ICS8516 accepts any differential input levels and translates them to 3V LVDS output levels. Dual output enable inputs allow the ICS8516 to be used in a 1-to-16 or 1-to-8 input/output mode.

Guaranteed output and part-to-part skew specifications make the ICS8515 ideal for those applications demanding well defined performance and repeatability.

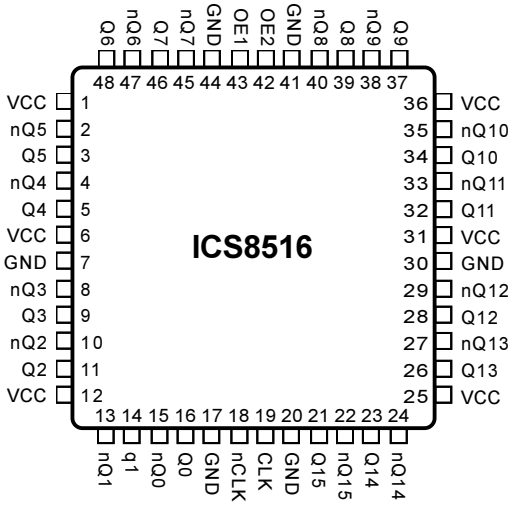
FEATURES

- 16 LVDS outputs
- Translates any differential input signal(PECL, HSTL, SSTL, DCM) to LVDS levels without external bias networks
- Translates any single-ended input signal to LVDS with resistor bias on nCLK input
- Translates single-ended input signal to inverted LVDS with resistor bias on CLK input
- Designed to meet or exceed the requirements of ANSI TIA/EIA-644
- 200ps output skew
- LVCMOS / LVTTL control inputs
- Multiple output enable inputs for disabling unused outputs in reduced fanout applications
- 3.3V operating supply
- 48 lead low-profile QFP(LQFP), 7mm x 7mm x 1.4mm package body, 0.5mm package lead pitch
- 0°C to 70°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



48-Lead LQFP
Y Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 7, 12, 25, 31, 36	VCC	Power		Power supply. Connect to 3.3V.
2, 3	nQ5, Q5	Output		Differential output pair. LVDS interface levels.
4, 5	nQ4, Q4	Output		Differential output pair. LVDS interface levels.
7, 17, 20 30, 41, 44	GND	Power		Power supply. Connect to ground.
8, 9	nQ3, Q3	Output		Differential output pair. LVDS interface levels.
10, 11	nQ2, Q2	Output		Differential output pair. LVDS interface levels.
13, 14	nQ1, Q1	Output		Differential output pair. LVDS interface levels.
15, 16	nQ0, Q0	Output		Differential output pair. LVDS interface levels.
18	nCLK	Input	Pullup	Inverting differential clock input.
19	CLK	Input	Pulldown	Non-inverting differential clock input.
21, 22	Q15, nQ15	Output		Differential output pair. LVDS interface levels.
23, 24	Q14, nQ14	Output		Differential output pair. LVDS interface levels.
26, 27	Q13, nQ13	Output		Differential output pair. LVDS interface levels.
28, 29	Q12, nQ12	Output		Differential output pair. LVDS interface levels.
32, 33	Q11, nQ11	Output		Differential output pair. LVDS interface levels.
34, 35	Q10, nQ10	Output		Differential output pair. LVDS interface levels.
37, 38	Q9, nQ9	Output		Differential output pair. LVDS interface levels.
39, 40	Q8, nQ8	Output		Differential output pair. LVDS interface levels.
42, 43	OE2, OE1	Input	Pullup	Output enable. OE2 controls outputs Q8, nQ8 thru Q15, nQ15; OE1 controls outputs Q0, nQ0 thru Q7, nQ7.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Capacitance			TBD		pF
COUT	Output Capacitance			TBD		pF

TABLE 3A. CONTROL INPUTS FUNCTION TABLE

Inputs		Outputs			
OE1	OE2	Q0 thru Q7	nQ0 thru nQ7	Q8 thru Q15	nQ8 thru nQ15
0	0	Hi Z	Hi Z	Hi Z	Hi Z
1	0	ACTIVE	ACTIVE	Hi Z	Hi Z
0	1	Hi Z	Hi Z	ACTIVE	ACTIVE
1	1	ACTIVE	ACTIVE	ACTIVE	ACTIVE

In the active mode the state of the output is a function of the CLK and nCLK inputs as described in Table 3B.

TABLE 3B. CLOCK INPUTS FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
CLK	nCLK	Q0 thru Q15	nQ0 thru nQ15		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Single ended use requires that one of the differential inputs be biased. The voltage at the biased input sets the switch point for the single ended input. For LVCMOS and LVTTL levels the recommended input bias network is a resistor to VCC, a resistor of equal value to ground and a 0.1µF capacitor from the input to ground. The resulting switch point is approximately VCC/2 ± 300mV.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	4.6V
Inputs	-0.5V to VDD + 0.5V
Outputs	-0.5V to VDDO + 0.5V
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of product at these condition or any conditions beyond those listed in the *DC Electrical Characteristics* or *AC Electrical Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4. DC ELECTRICAL CHARACTERISTICS, VCC=3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VTH	Differential Input High Threshold Voltage					100	mV
VTL	Differential Input Low Threshold Voltage			-100			mV
VPP	Peak-to-Peak Input Voltage						V
VCMR	Common Mode Voltage Range						V
IIH	Input High Current	CLK					µA
		nCLK, OE1, OE2					µA
IIL	Input Low Current	CLK					µA
		nCLK, OE1, OE2					µA
ICC	Operating Supply Current						mA
VOD	Differential Output Voltage						mV
Δ VOD	VOD Magnitude Change						mV
VOS	Offset Voltage						V
Δ VOS	VOS Magnitude Change						mV
IOZ	High Impedance Leakage Current						µA

TABLE 5. AC ELECTRICAL CHARACTERISTICS, VCC=3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Input Frequency				400	MHz
tpLH	Propagation Delay, Low-to-High	0 < f ≤ 400MHz	1.9		2.9	ns
tpHL	Propagation Delay, High-to-Low	0 < f ≤ 400MHz	1.9		2.9	ns
tsk(o)	Output Skew; NOTE 2				200	ps
tsk(pp)	Part-to-Part Skew; NOTE 3				TBD	ps
tR	Output Rise Time		TBD		TBD	ps
tF	Output Fall Time		TBD		TBD	ps
tPW	Output Pulse Width		tCYCLE/2 - TBD	tCYCLE/2	tCYCLE/2 + TBD	ns
tEN	Output Enable Time				TBD	ns
tDIS	Output Disnable Time				TBD	ns
VOX	Output Crossover Voltage		TBD		TBD	V

NOTE 1: All parameters measured at fMAX unless noted otherwise.
NOTE 2: Defined as skew across outputs at the same supply voltages and with equal load conditions. Measured from the differential input crossing point to the differential output crossing point.
NOTE 3: Defined as skew at different outputs on different devices operating at the same supply voltages and with equal load conditions. Measured from the differential input crossing point to the differential output crossing point.

FIGURE 1A, 1B, 1C - INPUT CLOCK WAVEFORMS

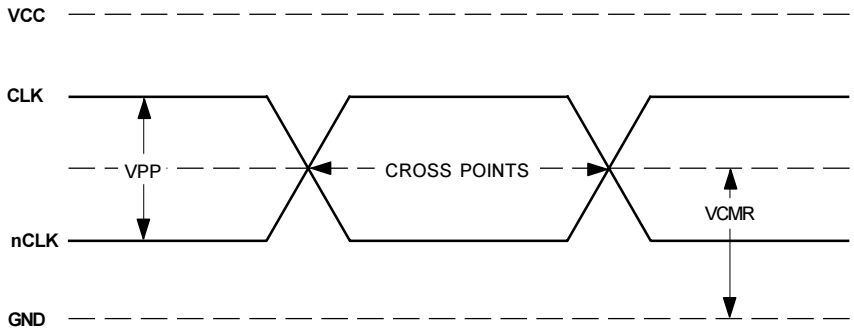


FIGURE 1A - DCM, LVDS, HSTL, SSTL DIFFERENTIAL INPUT LEVELS

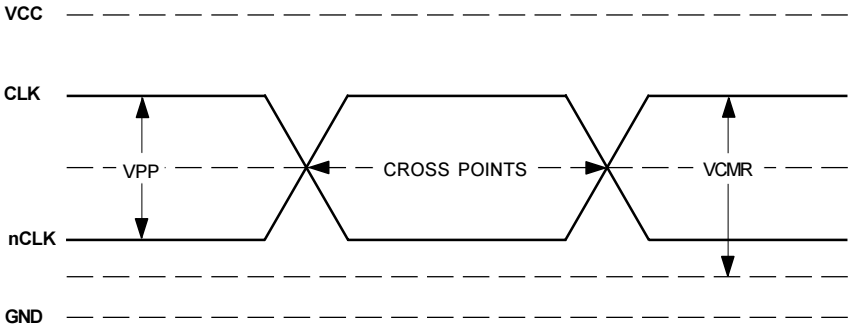


FIGURE 1B - LVPECL DIFFERENTIAL INPUT LEVEL

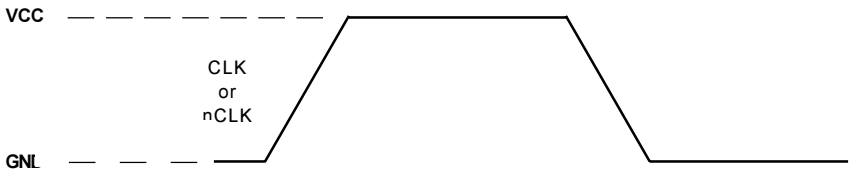
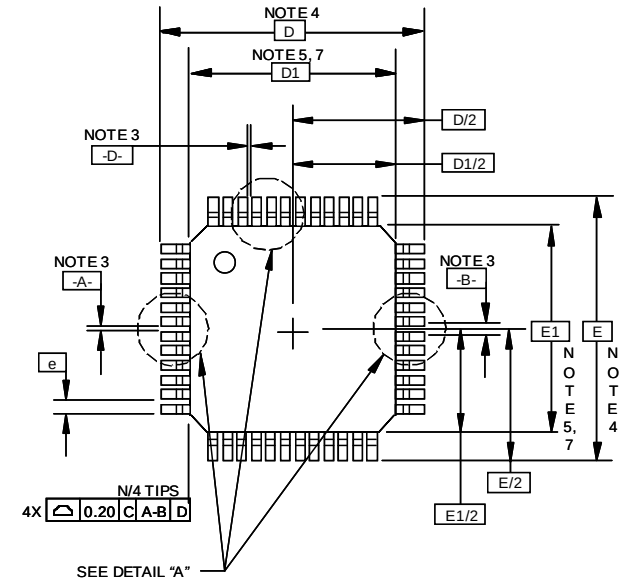
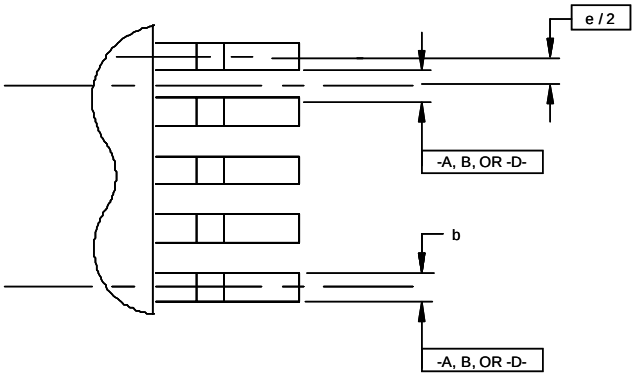
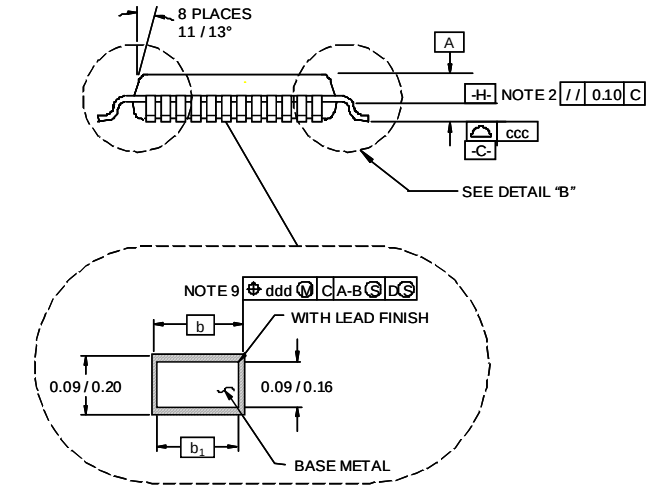


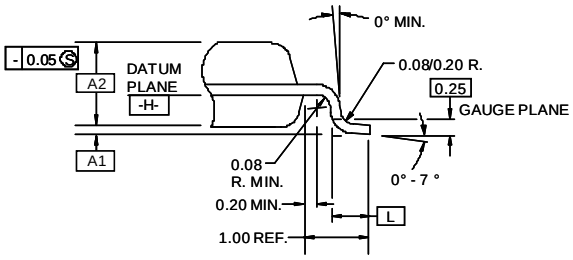
FIGURE 1C- LVCMOS AND LVTTL SINGLE ENDED INPUT LEVEL

PACKAGE OUTLINE AND DIMENSIONS - Y SUFFIX









NOTES:

1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982
2. DATUM PLANE -H- LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUMS A-B AND -D- TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC AT DATUM PLANE -H- .
4. TO BE DETERMINED AT SEATING PLACE -C- .
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
6. "N" IS THE TOTAL NUMBER OF TERMINALS.
7. THESE DIMENSIONS TO BE DETEREMINED AT DATUM PLANE -H-.
8. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.
9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
10. CONTROLLING DIMENSION: MILLIMETER.
11. THIS OUTLINE CONFORMS TO JEDEC PUBLIBCATION 95 REGISTRATION MS-026, VARIATION BBC.
12. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE.

SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			NOTE
	BBC			
	MIN.	NOM.	MAX.	
A			1.60	
A_1	0.05		0.15	12
A_2	1.35	1.40	1.45	
D		9.00 BSC.		4
D_1		7.00 BSC.		7, 8
E		9.00 BSC.		4
E_1		7.00 BSC.		7, 8
L	0.45	0.60	0.75	
N		48		
e		0.5 BSC.		
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc			0.08	
ddd			0.08	

ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8516DY	ICS8516DY	48 Lead LQFP	250 per tray	0°C to 70°C
ICS8516DYT	ICS8516DY	48 Lead LQFP on Tape and Reel	2000	0°C to 70°C

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