PRELIMINARY

Integrated Circuit Systems, Inc.

# ICS8431-11
## CLOCK SYNTHESIZER

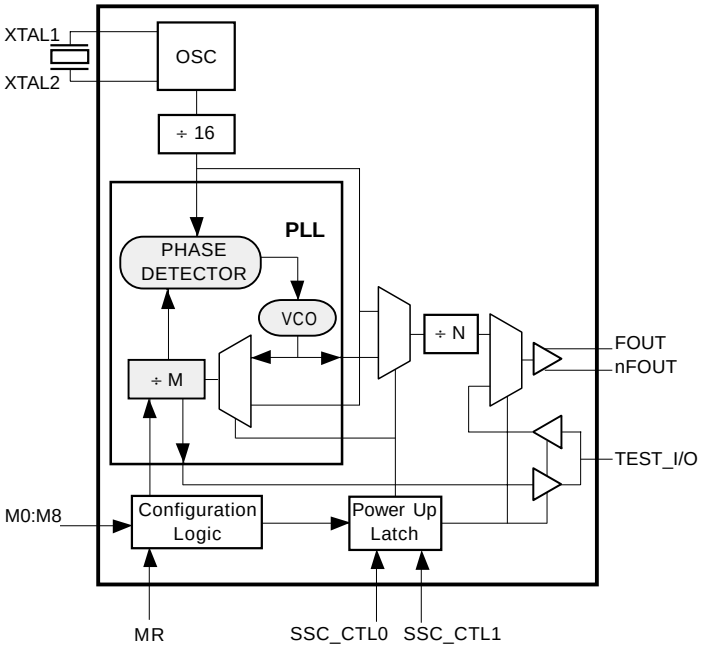
## GENERAL DESCRIPTION

The ICS8431-11 is a general purpose clock frequency synthesizer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The VCO operates at a frequency range of 280MHz to 400MHz. The output frequency can be programmed using the parallel interface, M0 thru M8, to the configuration logic. Spread spectrum clocking is programmed via the Power Up Latch inputs SSC_CTL0 and SSC_CTL1.

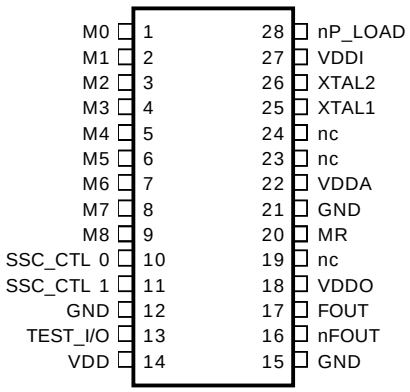
## FEATURES

- Fully integrated PLL
- Differential 3.3V LVPECL output
- Programmable PLL loop divider for generating a variety of output frequencies.
- Crystal oscillator interface
- Spread Spectrum Clocking (SSC) fixed at 1/2% modulation for environments requiring ultra low EMI
- Master reset for programming contents of the Power Up Latch
- LVTTL / LVCMOS control inputs
- PLL bypass modes supporting in-circuit testing and on-chip functional block characterization
- 3.3V supply voltage
- 28 lead SOIC
- 0°C to 70°C ambient operating temperature

## BLOCK DIAGRAM




## PIN ASSIGNMENT




**ICS8431-11**
**28-Lead SOIC**
**M Package**
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

## FUNCTIONAL DESCRIPTION

The ICS8431-11 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A 16MHz series-resonant , fundamental crystal is used as the input to the on-chip oscillator. The output of the oscillator is divided by 16 prior to the phase detector. With a 16MHz crystal this provides a 1MHz reference frequency. The VCO of the PLL operates over a range of 280 to 400MHz. The output of the loop divider is also applied to the phase detector.

The phase detector and the loop filter force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to the LVPECL output buffer. The divider provides a 50% output duty cycle.

The programmable features of the ICS8431-11 support four output operational modes and a programmable PLL loop divider. The four output operational modes are spread spectrum clocking (SSC), non-spread spectrum clock and two test modes and are controlled by the Power Up Latch. After power up the latch is disabled and the initial programmed values can only be overwritten by removing all power to the device or by asserting the master reset input, MR. A HIGH-to-LOW transition on MR latches new data into the Power Up Latch.

Programming the Spread Spectrum Clocking (SSC) feature is accomplished by configuring the internal Power Up Latch. The input to this latch is encoded by the SSC_CTL[1:0] pins which define all functional states after power is applied. Figure 1 shows the timing relationship of the latched SSC_CTL[1:0] in relationship to the PLL power-on condition.

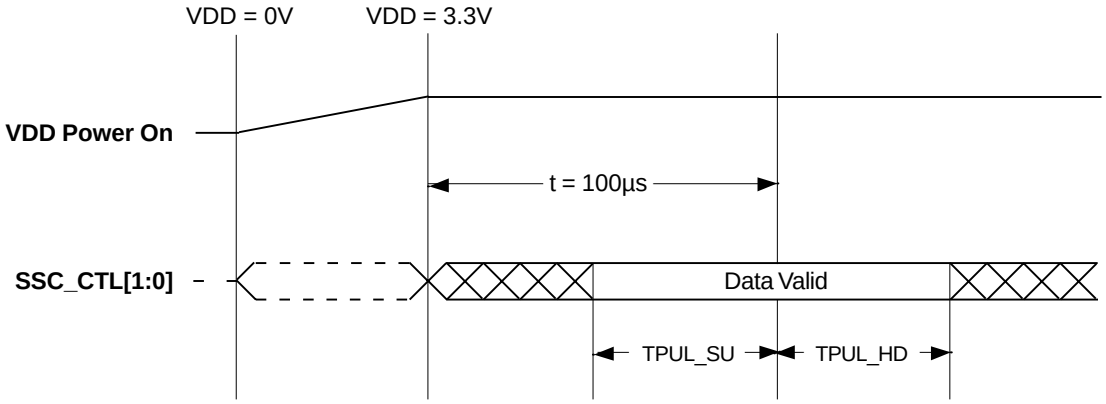



**FIGURE 1. POWER-UP CONFIGURATION TIMING**

Approximately 100µs after power is applied or a HIGH-to-LOW transistion on MR, the control bits SSC_CTL0 and SSC_CTL1 are latched. TPUL_SU is the time during which the data on the control bits is required to be valid before being latched. TPUL_HD is the time after the data is latched that the control bits are required to remain valid. The configuration latch can be overwritten by removing the power or by asserting MR and applying data to the inputs that meet the setup and hold time requirment during power-on or of the master rest input. The power-on setup and hold time requirements are defined in Figure 1. Table 3A, Control Input Function Table defined the valid commands for SSC_CTL[1:0] lines.

The PLL loop divider or M divider is programmed by using inputs M0 through M8. Normally upon system power-up the nP_LOAD input is held LOW until sometime after power becomes valid. On the LOW-to-HIGH transistion of nP_LOAD, the values present at M[8:0] are captured. The relationship between the VCO frequency, the crystal frequency and the loop counter/ divider is defined as follows:

$$fVCO = \frac{fxtal}{16} \times M$$

The M count and the required values of M0:M8 for programming the VCO are shown in Table 3B, Programmable VCO Frequency Function Table. The frequency out is defined as follows:

$$fout = \frac{fVCO}{N} = \frac{fxtal}{16} \times \frac{M}{N}$$

For the ICS8431-11 N equals 2. Valid M values for which the PLL will achieve lock are defined as $280 \leq M \leq 400$.

**TABLE 1. PIN DESCRIPTIONS**

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1 -9 | M0-M8 | Input | | M divider inputs. Data latched on LOW-to-HIGH transistion of nP_LOAD input. LVCMOS / LVTTL pins interface levels. |
| 10, 11 | SSC CTL 0, SSC CTL 1 | Input | Pullup | These LVCMOS / LVTTL pins are sampled during power-up to configure the SSC control. |
| 12 | GND | Power | | Ground pin for core and test output. |
| 13 | TEST I/O | Input / Output | | Programmed as input in PLL bypass mode. |
| 14 | VDD | Power | | Power supply pin for core and test output. |
| 15 | GND | Power | | Ground pin for output. |
| 16, 17 | nFOUT, FOUT | Output | | These differential outputs are main output drivers for the synthesizer. They are compatible with terminated positive referenced LVPECL logic. |
| 18 | VDDO | Power | | Power supply pin for output. |
| 19, 23, 24 | nc | Unused | | No connection. |
| 20 | MR | Input | Pulldown | Reset M counter. Loads and latches data on SSC_CTL0, SSC_CTL1 into Power-Up latch. |
| 21 | GND | Power | | PLL ground pin. |
| 22 | VDDA | Power | | PLL power supply pin. |
| 25, 26 | XTAL1, XTAL2 | Input | | Crystal oscillator input. |
| 27 | VDDI | Power | | Power supply pin for core. |
| 28 | nP_LOAD | Input | Pullup | M divider latch enable input. LVTTL / LVCMOS interface levels. |

**TABLE 2. PIN CHARACTERISTICS**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| CIN | Input Capacitance | | | | | pF |
| RPULLUP | Input Pullup Resistor | | | 51 | | KΩ |
| RPULLDOWN | Input Pulldown Resistor | | | 51 | | KΩ |

**TABLE 3A. SSC CONTROL INPUT FUNCTION TABLE**

| Inputs | | TEST_I/O Source | SSC | Outputs | | Operational Modes |
|---|---|---|---|---|---|---|
| SSC_CTL1 | SSC_CTL0 | | | FOUT, nFOUT | TEST_I/O | |
| 0 | 0 | Internal | Disabled | fXTAL ÷ 16 ÷ N | fXTAL ÷ 16 ÷ M | PLL bypass; Oscillator, oscillator, M and N dividers test mode. NOTE 1 |
| 0 | 1 | PLL | Enabled | 200MHz | Hi-Z | Default SSC; Modulation Factor = ½ Percent |
| 1 | 0 | External | Disabled | Test Clk | Input | PLL Bypass Mode, (1MHz ≤ Test Clk ≤ 200MHz) |
| 1 | 1 | PLL | Disabled | 200MHz | Hi-Z | No SSC Modulation |

NOTE 1: Used for in house debug and characterization.

**TABLE 3B. PROGRAMMABLE VCO FREQUENCY FUNCTION TABLE**

| VCO Frequency (MHz) | M Count | 256 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|
| | | M8 | M7 | M6 | M5 | M4 | M3 | M2 | M1 | M0 |
| 250 | 250 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 251 | 251 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 252 | 252 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 253 | 253 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| • | • | • | • | • | • | • | • | • | • | • |
| • | • | • | • | • | • | • | • | • | • | • |
| 498 | 498 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 499 | 499 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 500 | 500 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | 4.6V |
| Inputs | -0.5V to VDD + 0.5V |
| Outputs | -0.5V to VDDO + 0.5V |
| Ambient Operating Temperature | 0°C to 70°C |
| Storage Temperature | -65°C to 150°C |

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of product at these condition or any conditions beyond those listed in the *DC Electrical Characteristics* or *AC Electrical Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. LVTTL, LVCMOS DC ELECTRICAL CHARACTERISTICS,** VDD = VDDA = VDDO = 3.3V±5%, $T_A$ = 0°C TO 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| VDDA, VDDO, VDD | Power Supply Voltage | | | 3.135 | 3.3 | 3.465 | V |
| VIH | Input High Voltage | M0:M8, SSC_CTL0, SSC_CTL1, TEST_I/O | 3.135V ≤ VDD ≤ 3.465V | 2 | | 3.765 | V |
| VIL | Input Low Voltage | M0:M8, SSC_CTL0, SSC_CTL1, TEST_I/O | 3.135V ≤ VDD ≤ 3.465V | -0.3 | | 0.8 | V |
| IIH | Input High Current | M0:M8, SSC_CTL0, SSC_CTL1 | VDD = VIN = 3.465V | | | 50 | µA |
| | TEST_I/O | | VDD = VIN = 3.465V | | | 50 | µA |
| IIL | Input Low Current | M0:M8, SSC_CTL0, SSC_CTL1 | VDD = 3.465V, VIN = 0V | -600 | | | µA |
| | TEST_I/O | | VDD = 3.465V, VIN = 0V | -50 | | | µA |

**TABLE 4B. LVPECL DC ELECTRICAL CHARACTERISTICS,** VDD = VDDA = VDDO = 3.3V±5%, $T_A$ = 0°C TO 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| VOH | Output High Voltage; NOTE 1, 2 | VDDx = 3.3V | 2.1 | | 2.2 | V |
| VOL | Output Low Voltage; NOTE 1, 2 | VDDx = 3.3V | 1.4 | | 1.5 | V |
| VSWING | Peak-to-Peak Output Voltage Swing | | 600 | | 800 | V |
| IOH | Output High Current | | 16 | | 18 | mA |
| IOL | Output Low Current | | 2 | | 4 | mA |

NOTE 1: These values are for VDDO equal to 3.3V. Output levels will vary 1:1 with VDDO.
NOTE 2: Output terminated with 50Ω to VDDO - 2V.

**TABLE 5. CRYSTAL CHARACTERISTICS**

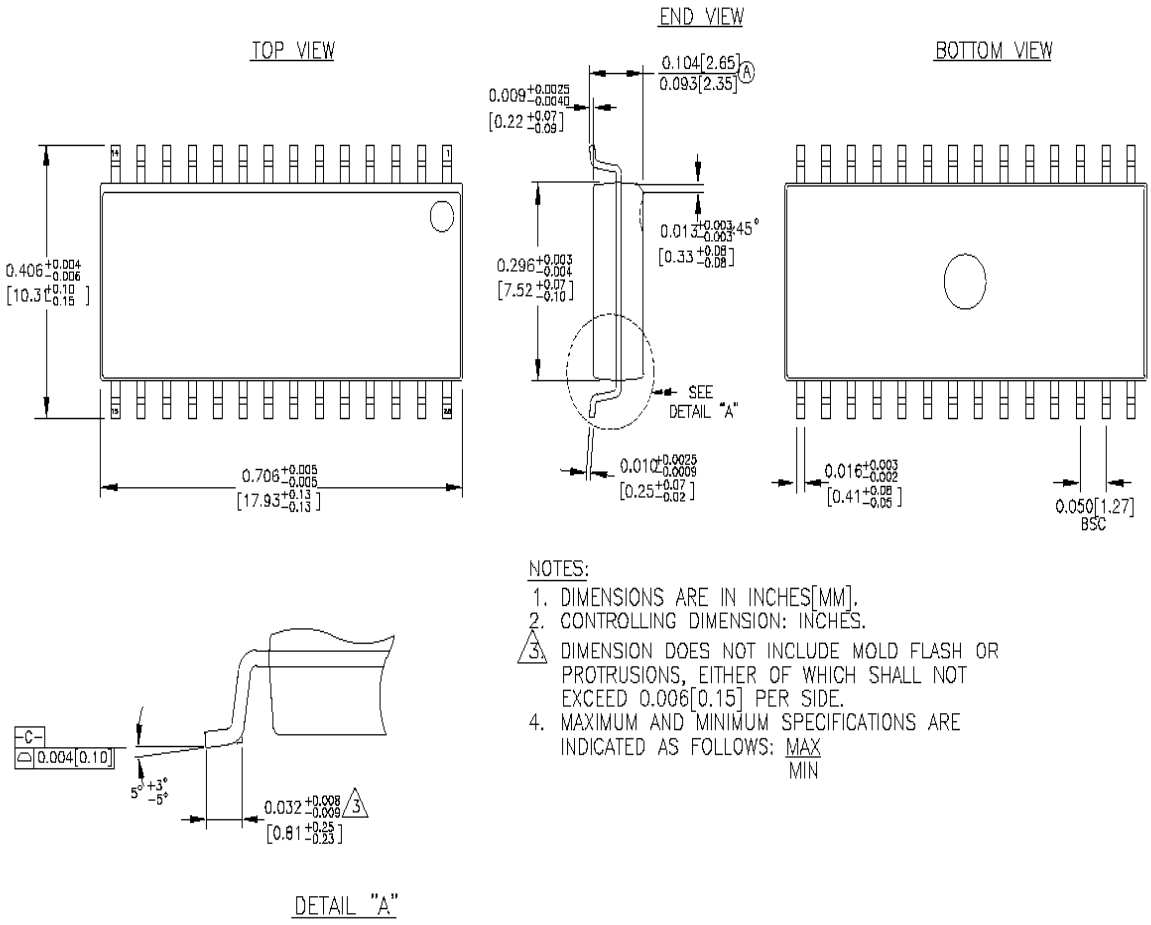
| Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Crystal Cut | Mode of Oscillation | | | | |
| Frequency Tolerance | | | | | ppm |
| Frequency Stability | | | | | ppm |
| Drive Level | | | | | µW |
| Equivalent Series Resistance (ESR) | | | | | Ω |
| Shunt Capacitiance | | | | | pF |
| Series Pin Inductance | | | | | nH |
| Aging | | | | | ppm |

**TABLE 6. AC ELECTRICAL CHARACTERISTICS,** VDD = VDDA = VDDO = 3.3V±5%, $T_A$ = 0°C TO 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| tjit | Peak Jitter (Short Cycle); NOTE 1 | | | | | 50 | ps |
| tDC | Output Duty Cycle; NOTE 1 | | | 47 | | 53 | % |
| tR | Output Rise Time | | 20% to 80% | 300 | | 800 | ps |
| tF | Output Fall Time | | 20% to 80% | 300 | | 800 | ps |
| Fm | SSC Modulation Frequency | | | 30 | | 33.33 | KHz |
| Fmf | SSC Modulation Factor | | | 0.5 | | | % |
| tLOCK | PLL Lock Time | | | | | TBD | µs |
| tPW | Input Pulse Width | nP_LOAD | | TBD | | | ns |
| tS | Setup Time | SSC_CTLx to MR | | 10 | | | ns |
| | | M to nP_LOAD | | TBD | | | |
| tH | Hold Time | SSC_CTLx to MR | | 0 | | | ns |
| | | M to nP_LOAD | | TBD | | | |
| tPUL_SU | Configuration Latch Setup Time | | | 10 | | | ns |
| tPUL_HD | Configuration Latch Hold Time | | | 0 | | | ns |

NOTE 1: Spread spectrum clocking enabled.

## PACKAGE OUTLINE AND DIMENSIONS - M SUFFIX




NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.15] PER SIDE.
4. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX / MIN

## ORDERING INFORMATION

| Part/Order Number | Marking | Package | Count | Temperature |
|---|---|---|---|---|
| ICS8431AM-11 | ICS8431AM-11 | 28 Lead SOIC | | 0°C to 70°C |
| ICS8431AM-11T | ICS8431AM-11 | 28 Lead SOIC on Tape and Reel | | 0°C to 70°C |