Clock Generation Interfacing for Mixed 3V and 5V Systems

In many system designs it may be advantageous or mandatory to use both five to three volt supply components. Most of the Frequency and Timing Generators (FTGs) that ICS produces will operate from both 5.0 (4.5 - 5.5V) and 3.3 (2.7 - 3.7V) volt power supplies. This application note suggests some recommended solutions, their implementation and important points to be considered when interfacing signals that must connect between clock generators, and logic circuits operating at different supply voltages. Examples of the interface circuits are also included.

The major considerations are logic voltage levels, power dissipation of the circuits, and signal duty cycle as defined by switching threshold voltages.

Logic Levels

TTL logic, in general, has its logic switching levels located at 0.8 and 2.0 volts. CMOS logic switches at the midpoint between VDD and VSS (usually ground) potential. The further that the input signals swing (and stay) beyond these levels, the more noise margin and thus stability a circuit exhibits. A 2.5V amplitude signal, biased to an appropriate DC voltage, is sufficient to trigger both CMOS gates operating at 3.0 volts VDD and TTL compatible inputs at 3 or 5V.

Power Dissipation

If an input signal that exceeds the supply voltage by more than .6 volts is applied to a CMOS or TTL circuit, then the internal protection circuits will begin to draw current. This will cause excessive internal heat to be dissipated, excessive drive to be required, and longer times for the gate to change state due to the stored charge needed to discharge the saturated diodes junction. In the extreme (current into input exceeds 100 mA) case, latch-up can be induced in CMOS circuits.

Duty Cycle

The threshold level that ICS uses for measuring the duty cycle for both TTL and CMOS compatible inputs powered at 3 and 5 volts is 1.4 volts. This attribute permits a uniform method for interfacing and specifying both types of circuits.

A common system configuration is to use a 5V supply for the CPU and peripherals, but run a graphics controller (such as Cirrus CL-GD6412) from 3V. An excellent solution to system clocking is a combination of the AV9154A motherboard clock generator (to provide the clocks required by the CPU and peripherals) and the ICS9161A graphics frequency generator (to produce the video and memory clocks for the graphics controller). The AV9154A is powered from the 5V supply and the ICS9161A is connected to the 3V supply. The principal technical consideration is the interface of the 5V REFCLK (14.318 MHz) output signal of the AV9154A to the ICS9161A ICLK input. Other variations of this situation occur when 3 volt CPUs must be used in predominately 5 volt designs.

Two approaches are recommended as a solution to this situation. A simple and inexpensive solution is to use a voltage divider (Figure 1) to scale the 5 volt VDD max signal to a 3.0 volt maximum signal. However, this approach will cause the driving gate to source about 9 mA (resistor DC current alone) from its 5V supply when the signal is at a logic high level. Due to the constant DC load on the driving device, this solution may not be desirable at higher clock frequencies because of the fact that the constant DC loading will steal current from the driving device at critical times (such as rise and fall edge periods) that, therefore, cannot be used to overcome the capacitive reactance of the gate being driven. During these transition periods the loss of the drivers ability to sink and source maximum currents results in increased waveform transition times and thus poorer circuit performance.

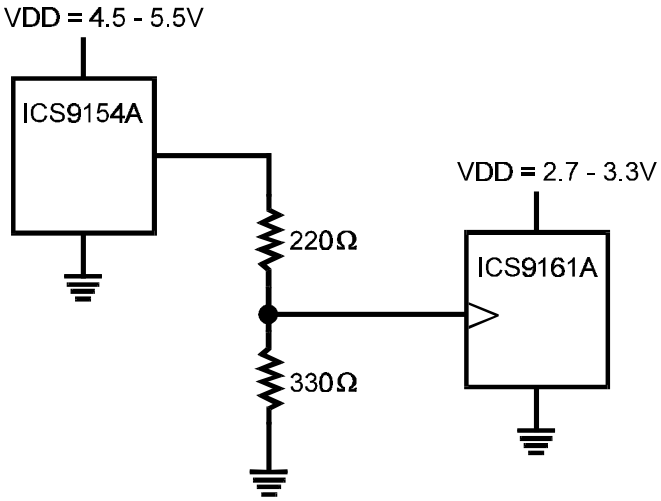

Figure 1

A second approach that improves performance at higher clock frequencies is shown in Figure 2. It has more components (3 rather than 2), but has the advantage of drawing no current (quiescently) from the 5 or 3 volt supply, and operates at greater coupling efficiency as the clock frequency increases. The resistors form a voltage divider (as in the first example) that set the maximum high signal level potential that is delivered to the load device input. This circuit will result in significantly less current draw from the supplies, but be aware that there are two caveats to this implementation.

First, the reactance (Xc) of the capacitor will effect the coupling as operating frequency decreases at an exponential rate. You must calculate its effect at the lowest possible signal frequency to offset any adverse effects that it has on the signal. If it has significant reactance in your implementation, this value must be included as part of the source (in this case the 220 ohm) resistors value to keep the voltage division correct.

Secondly, this is an AC coupled circuit. If the input signal ceases to exist or changes to a DC level (as in a stop clock or power down condition), the input, as seen by the ICS9161A device, will decay to 0 volts as the 330 ohm resistor discharges the stored charge on the input pin of the ICS9161A device.

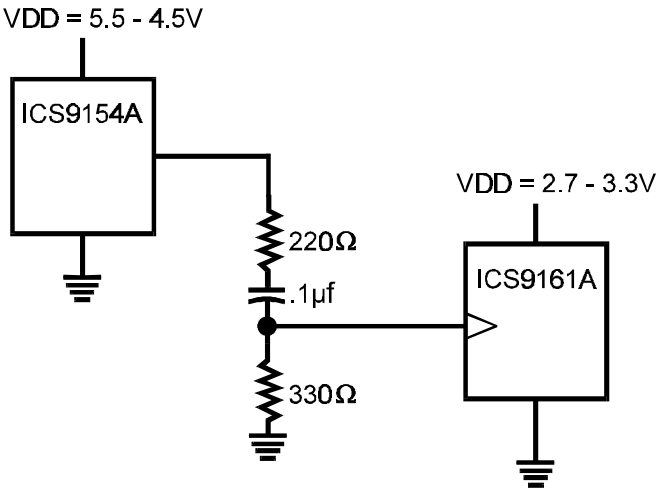

Figure 2

In the following scenario it is desired to drive a 5 volt logic device with a FTG that is operating from a 3 volt supply. In many instances the loading device will accept the 0 and 3 volt rail-to-rail swing that the CMOS device provides as adequate levels to operate with good reliability. In others you must produce a 0 to 5 volt level (or close to) to provide the circuit with required noise immunity or to meet load device mandated specifications.

Since the clock being generated must have a full 5 volt (or as close to as possible) swing, supplying the interface device(s) with 5 volt power is mandatory. For the best noise figure (minimum noise injection susceptibility), it is highly desirable to supply the interface circuitry from the same power source that is providing power to the device being driven by the resulting 5 volt logic clock(s). This will keep any power supply noise common (mode) to both device. Two approaches are recommended to achieve this. The one chosen will usually be determined by available unused gate inventory or the real estate on the PCB.

The first solution (Figure 3) involves the use of an NPN transistor and 2 resistors. An optional speed up capacitor (C1) may be needed if the clock being translated is of a very high frequency. The capacitor provides a very low impedance to the high frequency clock edge current components and allows them unrestricted access to the gates base (or FETs gate) to drain gate current or supply it as needed. The base resistor (R1) on the driver side limits the loading that the circuitry has on the driver and should be chosen based on overall circuit power dissipation, drivers maximum sink and source current specification, and the desired transistors base current. While the optional capacitor will aid in the initial edge current availability at the base of the transistor, a lower base resistor (R1) value will bolster initially bias, and assist in the transition time by providing a lower impedance path to the drivers internal sourcing and sinking devices. On the output side of the transistor is a single load resistor. Its value should be chosen with two points in mind. One is the current that the circuit (transistor) will draw when the device is saturated or fully turned on. The DC current (in a 50/50 duty cycle design) may be calculated by using half of the ohms law value using its resistance and VDD supply voltage. Don't forget to subtract the saturation drop of the transistor from the supply voltage. The smaller this current the slower the transistors output will rise and fall. This is due to its participation in the RC time constant that is in effect to charge the clock loads gate parasitic capacity and on the falling edge to remove this charge from that and the transistors junctions.

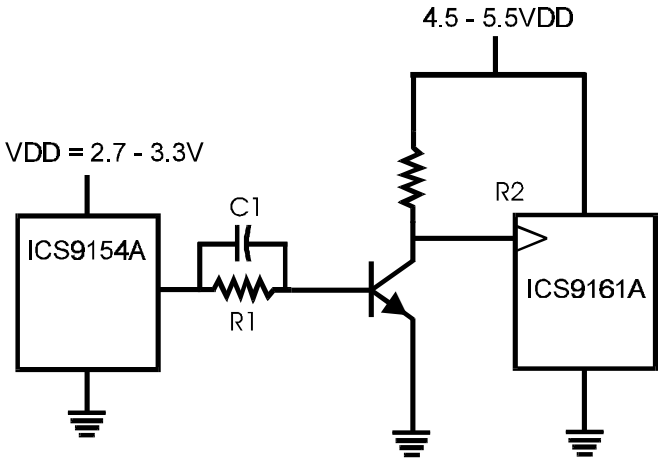

Figure 3

The second (Figure 4) involves a TTL or CMOS gate. This gate is also supplied with 5 volts so its output will swing, in the case of CMOS, from VCC to ground rail (minus the gates internal device saturation drop). In the case of a standard TTL gate, the outputs will be TTL in level. The choice of logic will depend, again, on excess gate inventory during design and/or the logic family levels that are mandated by the components that must be driven. If CMOS logic is used in the translator, both TTL and CMOS logic input levels will be met by this design. If the gate is TTL, its internal ability to sink current will exceed its ability to source current. If this adversely affects the output clocks duty cycle, a pull-down resistor may be required to restore precise duty cycles.

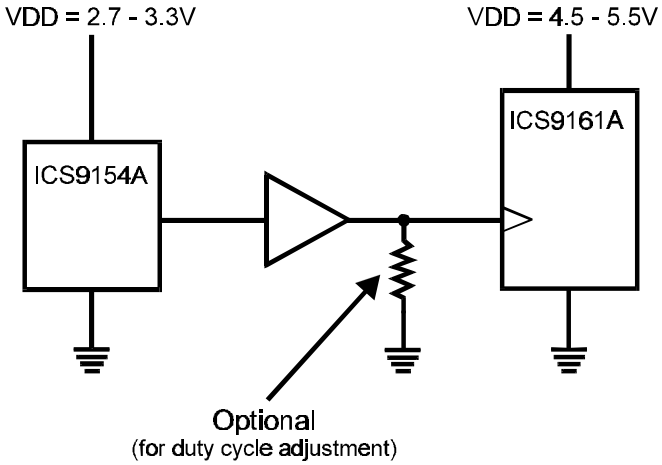

Figure 4

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