Integrated Circuit Systems, Inc.

# ICS9211-02

**Preliminary Product Preview**

# Direct Rambus™ Clock Generator

## General Description

The **ICS9211-02** is a High-speed clock generator providing 400 MHz differential clock source for direct Rambus™ memory system. It includes DDLL (Distributed Delay locked loop) and phase detection mechanism to synchronize the direct Rambus™ channel clock to an external system clock. ICS 9211-02 provides a solution for a broad range of Direct Rambus memory applications. The device works in conjunction with the ICS9250-09.

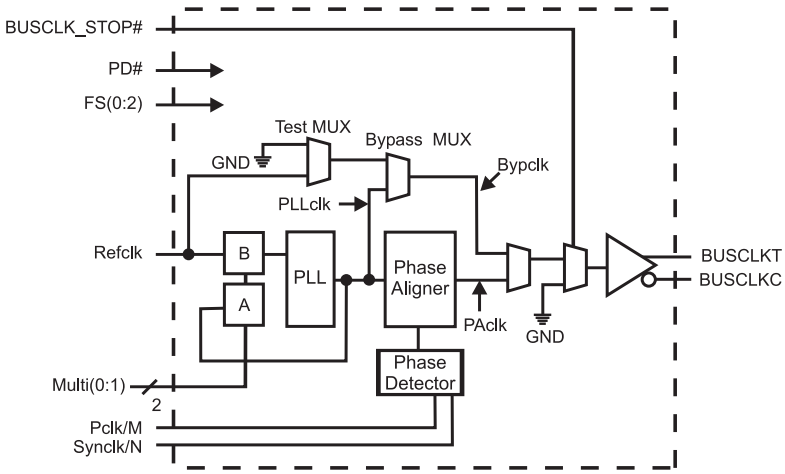
The **ICS9211-02** power management support system turns "off" the Rambus™ channel clock to minimize power consumption for mobile and other power –sensitive applications. In "clock off" mode the device remains "on" while the output is disabled, allowing fast transitions between clock-off and clock –on states. In "power down" mode it completely powers down for minimum power dissipation.

The ICS9211-02 meets the requirements for input frequency tracking when the input frequency clock is using Spread Spectrum clocking and also the optimum bandwidth is maintained while attenuating the jitter of the reference signal.

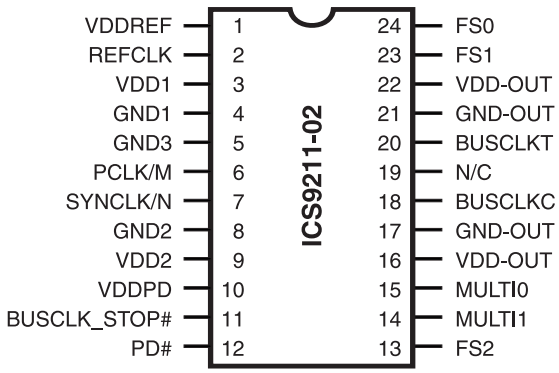
## Features

- Compatible with all Direct Rambus™ based IC s
- Up to 400 MHz differential clock source for direct Rambus™ memory system
- Cycle to cycle jitter is less than 60ps
- 3.3 ± 5% supply
- Synchronization flexibility: Supports Systems that need clock domains of Rambus channel to synchronize with system or processor clock, or systems that do not require synchronization of the Rambus clock to another system clock
- Excellent power management support
- REFCLK input is from the ICS9250-09.

## Block Diagram




## Pin Configuration




**24-Pin 150 Mil SSOP**

## Pin Descriptions

| Pin # | Name | Type | Description |
|---|---|---|---|
| 1 | VDDREF | REFV | Reference voltage for refclk, to be connected to CK133 |
| 2 | REFCLK | IN | Reference clock, to be connected to CK133 |
| 3 | VDD1 | PWR | 3.3 V power supply used for PLL |
| 4 | GND1 | PWR | Ground for PLL |
| 5 | GND3 | PWR | Ground for control inputs |
| 6,7 | PCLK/M, SYNCLK/N | IN | Phase controller input, used to drive a phase aligner that adjusts the phase of the busclk. |
| 8 | GND2 | PWR | Ground for phase aligner |
| 9 | VDD2 | PWR | 3.3 V power supply used for phase aligner |
| 10 | VDDPD | REFV | Reference voltage for phase detector inputs connected to the controller |
| 11 | BUSCLK_ STOP# | IN | Active low output enable/disable |
| 12 | PD# | IN | 3.3V CMOS active low power down, the device is powered down when the "(PD#) =0" |
| 14,15 | MULTI (0:1) | IN | 3.3V CMOS PLL Multiplier select, logic for selecting the multiply ratio for the PLL from the input REFCLK |
| 16 | VDD_OUT | PWR | 3.3V supply for clock out puts |
| 17 | GND_OUT | PWR | Ground for clock outputs |
| 18 | BUSCLKC | OUT | Out put clock connected to the Rambus channel. This output is the complement of BUSCLK |
| 19 | N/C | N/C | NOT USED |
| 20 | BUSCLKT | OUT | Out put clock connected to the Rambus channel. This output is the true component of BUSCLK |
| 21 | GND_OUT | PWR | Ground for clock outputs |
| 22 | VDD_OUT | PWR | 3.3V supply for clock out puts |
| 13,23,24 | FS(0:2) | IN | 3.3V CMOS Mode control, used in selecting bypass, test, normal, and output test (OE) |

## PLL DIVIDER SELECTION AND PLL VALUES ( PLLCLK = REFCLK*A/B)

| Multo | Mult1 | A | B | PLLCLK for REFCLK=50MHz | PLLCLK for REFCLK=66.6MHz |
|---|---|---|---|---|---|
| 0 | 0 | 9 | 2 | 225 | 300 |
| 0 | 1 | 6 | 1 | 300 | 400 |
| 1 | 0 | 16 | 3 | 267 | 356 |
| 1 | 1 | 8 | 1 | 400 | Reserved |

| BYPASS AND TEST MODE SELECTION | | | | | | |
|---|---|---|---|---|---|---|
| Mode | FS0 | FS1 | FS2 | Bypclk (int.) | BusClk | BusClkB |
| Normal | 0 | 0 | 0 | Gnd | PAclk | PAclkB |
| Bypass | 1 | 0 | 0 | PLLclk | PLLclk | PLLclkB |
| Test | 1 | 1 | 0 | Refclk | Refclk | RefclkB |
| Vendor Test A | 0 | 0 | 1 | - | - | - |
| Vendor Test B | 1 | 0 | 1 | - | - | - |
| Reserved | 1 | 1 | 1 | - | - | - |
| Output Test (OE) | 0 | 1 | X | - | Hi-Z | Hi-Z |

## POWER MANAGEMENT MODES

| State | PwrDnB | StopB |
|---|---|---|
| NORMAL | 1 | 1 |
| Clk Off | 1 | 0 |
| Powerdown | 0 | X |

## Absolute Maximum Ratings

Supply Voltage . . . . . 4.0 V
Logic Inputs . . . . . GND –0.5 V to $V_{DD}$ +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## Electrical Characteristics-input/supply/Outputs

| Parameters | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage | VDD | 3.15 | 3.45 | V |
| Refclk Input cycle time | $t_{CYCLE,IN}$ | 10 | 40 | ns |
| Input cycle-to-cycle Jitter | $t_{J,IN}$ | - | 250 | ps |
| Input Duty cycle over 10k cycles | $DC_{IN}$ | 40% | 60% | $t_{CYCLE}$ |
| Input frequency of modulation | $F_{m,in}$ | 30 | 33 | KHz |
| Modulation index | $P_{M,IN}$ | 0.25 | 0.5 | % |
| Phase detector input cycle time at PDclk/M & Synclk/N | $t_{CYCLE,PD}$ | 30 | 100 | ns |
| Initial phase error at phase detector inputs | $T_{err,init}$ | -0.5 | 0.5 | $t_{CYCLE,PD}$ |
| Phase detector input duty cycle over 10k cycles | $D_{CIN,PD}$ | 25% | 75% | $t_{CYCLE,PD}$ |
| Input rise & fall times ( measured at 20%-80% of input voltage) for PDCLK/M & SYNCLK/N,&REfCLK | $T_{IR}$,$T_{IF}$ | - | 1 | ns |
| Input capacitance at PDCLK/M,Synclk/N,&REFCLK | $C_{IN,PD}$ | - | 7 | pF |
| Input Capacitance matching at PCLK/M & SYNCLK/N | $\Delta C_{IN,PD}$ | - | 0.5 | pF |
| Input capacitance at CMOS pins | $C_{IN,CMOS}$ | - | 10 | pF |
| Input (CMOS) signal low voltage | $V_{IL}$ | - | 0.3 | Vdd |
| Input (CMOS) signal high voltage | $V_{IH}$ | 0.7 | - | Vdd |
| REFCLK input low voltage | $V_{IL,R}$ | - | 0.3 | Vddi,R |
| REFCLK input high voltage | $V_{IH,R}$ | 0.7 | - | Vddi,R |
| Input signal low voltage for PD inputs and STOP | $V_{IL,PD}$ | - | 0.3 | Vddi,PD |
| Input signal high voltage for PD inputs and STOP | $V_{IH,PD}$ | 0.7 | - | Vddi,PD |
| Input supply referance for REFCLK | $V_{DD,IR}$ | 1.3 | 3.3 | V |
| Input supply referance vfor PD inputs | $V_{DDI,PD}$ | 1.3 | 3.3 | V |
| Phase detector phase error for distributed loop measured at PDCLK/M & SYNCLK/N(rising | $t_{ERR,PD}$ | -100 | 100 | ps |
| Cycle cycle time | $t_{CYCLE}$ | 2.5 | 3.75 | ns |
| Cycle-to-cycle jitter at Busclk/BUSCLKB | $t_J$ | - | 60 | ps |
| Total jitter over 2,3, or 4clock cycles | tJ | - | 100 | ps |
| Phase aligner, phase step size (BSCLK/BUSCLKB) | $t_{STEP}$ | 1 | - | ps |
| PLL out put phase error when tracking SSC | $t_{ERR,SSC}$ | -100 | 100 | ps |
| Out put crossing-point voltage | $V_X$ | 1.3 | 1.8 | V |
| Output voltage swing | $V_{COS}$ | 0.4 | 0.6 | V |
| Output high voltage | $V_H$ | - | 2 | V |
| Out put duty cycle over 10k cycle | DC | 40% | 60% | $t_{CYCLE}$ |
| Output cycle -to-cycle duty cycle error | $t_{DC,ERR}$ | - | 50 | ps |
| Output rise & fall times ( measured at 20%-80% of output voltage) | $t_{CR}$,$t_{CF}$ | 300 | 500 | psd |
| Difference between rise and fall times on a single device(20%-80%) | $t_{CR,CF}$ | - | 100 | ps |

**General Layout Precautions:**

1) Use a ground plane on the top layer of the PCB in all areas not used by traces.

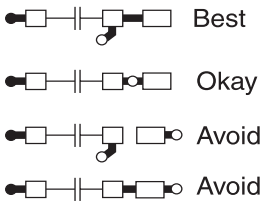
2) Make all power traces and vias as wide as possible to lower inductance.

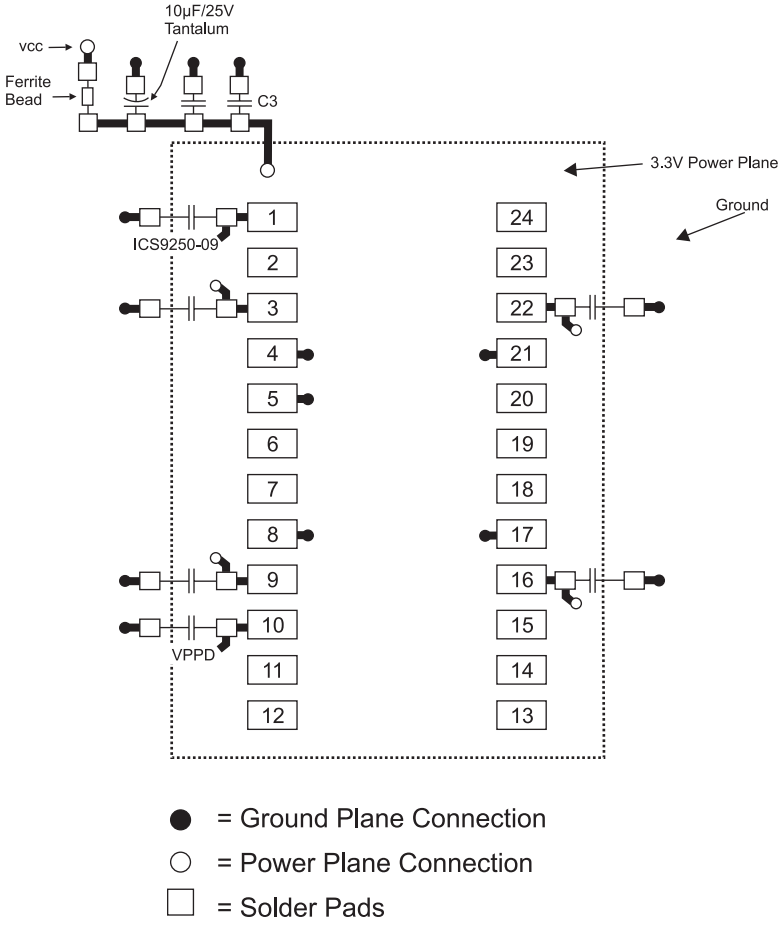
**Capacitor Values:**

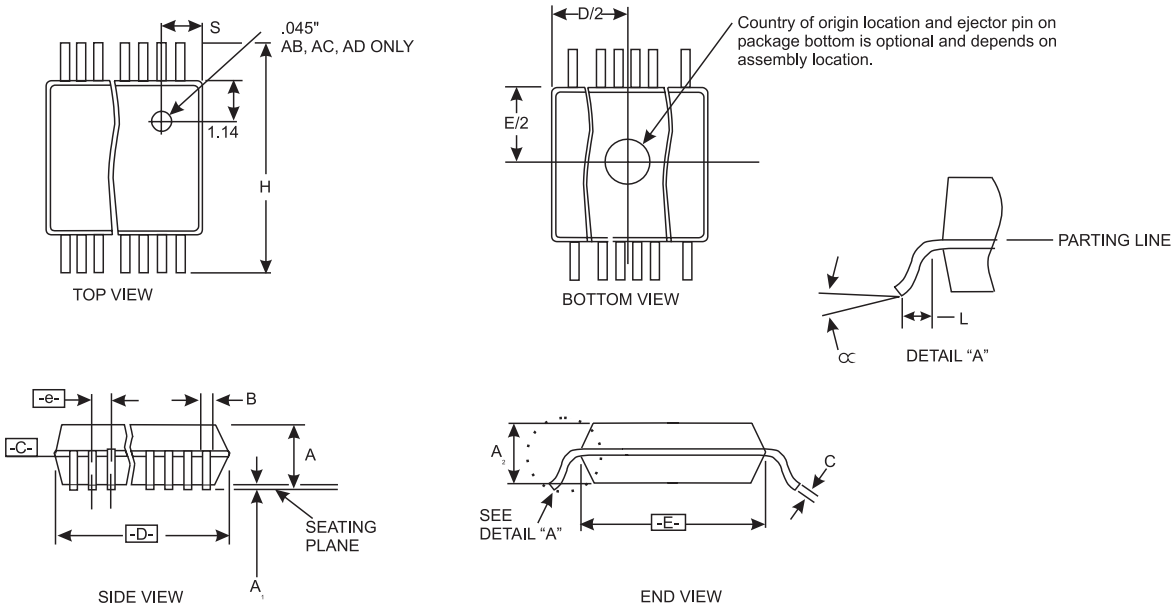
C3 : 100pF ceramic

All unmarked capacitors are 0.01µF ceramic

**Connections to VDD:**






| SYMBOL | COMMON DIMENSIONS | | | VARIATIONS | D | | | S | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | N |
| A | .061 | .064 | .068 | AA | .189 | .194 | .196 | .0020 | .0045 | .0076 | 16 |
| A1 | .004 | .006 | .0098 | AB | .337 | .342 | .344 | .0500 | .0525 | .0550 | 20 |
| A2 | .055 | .058 | .061 | AC | .337 | .342 | .344 | .0250 | .0275 | .0300 | 24 |
| B | .008 | .010 | .012 | AD | .386 | .391 | .393 | .0250 | .0280 | .0300 | 28 |
| C | .0075 | .008 | .0098 | | | | | | | | |
| D | SEE VARIATIONS | | | | | | | | | | |
| E | .150 | .155 | .157 | | | | | | | | |
| e | .025 BSC | | | | | | | | | | |
| H | .230 | .236 | .244 | | | | | | | | |
| L | .010 | .013 | .016 | | | | | | | | |
| N | SEE VARIATIONS | | | | | | | | | | |
| S | SEE VARIATIONS | | | | | | | | | | |
| ∝ | 0° | 5° | 8° | | | | | | | | |
| X | 0.85 | 0.93 | .100 | | | | | | | | |

**150 mil SSOP Package**

Diminisions are in inches

## Ordering Information

**ICS9211yF-02**

Example:

**ICS XXXX y F - PPP**

- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator**
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device