



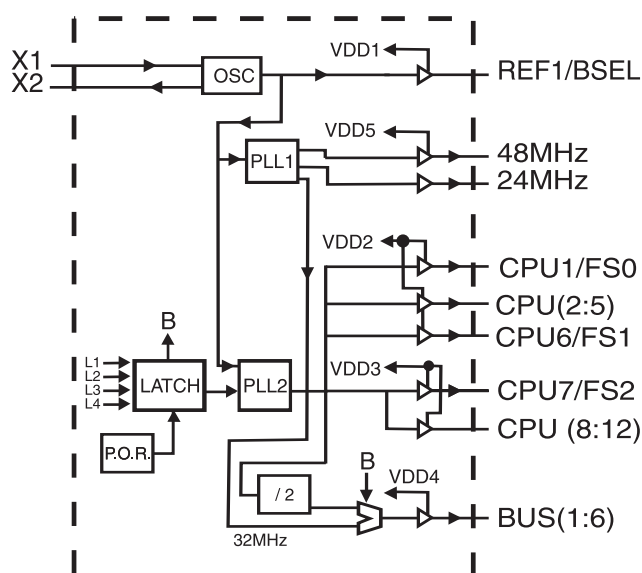
Frequency Generator for Pentium™ Based Systems

General Description

The **ICS9169C-273** is a low-cost frequency generator designed specifically for Pentium based chip set systems. The integrated buffer minimizes skew and provides all the clocks required. A 14.318 MHz XTAL crystal provides the reference clock to generate standard Pentium frequencies. The CPU clock makes gradual frequency transitions without violating the PLL timing of internal microprocessor clock multipliers.

Twelve CPU clock outputs provide sufficient clocks for the CPU, chip set, memory and up to two DIMM connectors (with four clocks to each DIMM). Either synchronous (CPU/2) or asynchronous (32 MHz) PCI bus operation can be selected by latching data on the BSEL input.

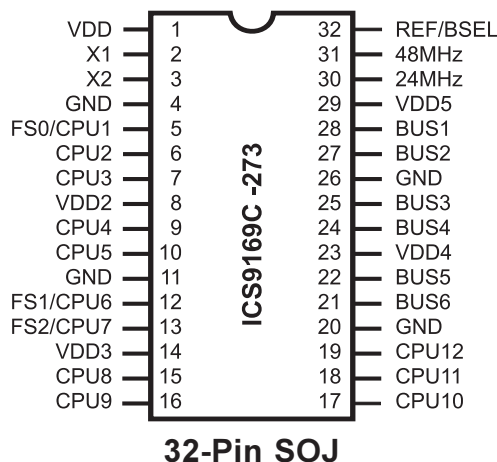
Block Diagram



Features

- Twelve selectable CPU clocks operate up to 83.3MHz
- Maximum CPU jitter of ± 200 ps
- Six BUS clocks support sync or async bus operation
- 250ps skew window for CPU outputs, 500ps skew window for BUS outputs
- CPU clocks BUS clocks skew 0-2ns (CPU early)
- Integrated buffer outputs drive up to 30pF loads
- 3.0V - 3.7V supply range, CPU(1:6) outputs 2.5V(2.375-2.62V) VDD option
- 32-pin SOJ package
- Logic inputs latched at Power-On for frequency selection saving pins as Input/Output
- 48 MHz clock for USB support and 24 MHz clock for FD

Pin Configuration



Functionality

3.3V \pm 10%, 0-70°C
Crystal (X1, X2) = 14.31818 MHz

VDD Groups:

VDD1 = X1, X2, REF/BSEL
VDD2 = CPU(1:6)
VDD3 = CPU(7:12) & PLL Core
VDD4 = BUS(1:6)
VDD5 = 48/24 MHz

Latched Inputs:

L1 = BSEL
L2 = FS0
L3 = FS1
L4 = FS2

| ADDRESS SELECT | | | CPU(1:12) (MHz) | BUS (1:6)MHz | | 48MHz | 24MHz | REF |
|----------------|-----|-----|-----------------|--------------|----------|----------|----------|----------|
| FS2 | FS1 | FS0 | | BSEL=1 | BSEL=0 | | | |
| 0 | 0 | 0 | 50 | 25 | 32 | 48 | 24 | REF |
| 0 | 0 | 1 | 60 | 30 | 32 | 48 | 24 | REF |
| 0 | 1 | 0 | 66.6 | 33.3 | 32 | 48 | 24 | REF |
| 0 | 1 | 1 | REF/2 | REF/4 | REF/3 | REF/2 | REF/4 | REF |
| 1 | 0 | 0 | 55 | 27.5 | 32 | 48 | 24 | REF |
| 1 | 0 | 1 | 75 | 37.5 | 32 | 48 | 24 | REF |
| 1 | 1 | 0 | 83.3 | 41.7 | 32 | 48 | 24 | REF |
| 1 | 1 | 1 | Tristate | Tristate | Tristate | Tristate | Tristate | Tristate |

Pentium is a trademark on Intel Corporation.



Pin Descriptions

| PIN NUMBER | PIN NAME | TYPE | DESCRIPTION |
|-------------------------|------------------|------|--|
| 1 | VDD1 | PWR | Power for device logic, and 24/48MHz output |
| 2 | X1 | IN | XTAL or external reference frequency input. This input includes XTAL load capacitance and feedback bias for a 12-16MHz crystal, nominally 14.31818MHz external crystal load of 30pF to GND recommended for VDD power on faster than 2.0ms. |
| 3 | X2 | OUT | XTAL output which includes XTAL load capacitance. External crystal load of 10pF to GND recommended for VDD power on faster than 2.0ms. |
| 4,11,20,26 | GND | PWR | Ground for device logic. |
| 5 | CPU(1) | OUT | Processor clock output which is a multiple of the input reference frequency. |
| | FS0 | IN | Frequency multiplier select pin. See shared pin description.* |
| 6,7,9,10,15,16,17,18,19 | CPU (2:5) (8:12) | OUT | Processor clock outputs which are a multiple of the input reference frequency. |
| 8 | VDD2 | PWR | Power for CPU(1:6) output buffers only. Can be reduced VDD for 2.5V (2.375-2.62V) next generation processor clocks. |
| 12 | CPU(6) | OUT | Processor clock output which is a multiple of the input reference frequency internal pull up devices. |
| | FS1 | IN | Frequency multiplier select pin. See shared pin description.* |
| 13 | CPU(7) | OUT | Processor clock output which is a multiple of the input reference frequency internal pull up devices. |
| | FS2 | IN | Frequency multiplier select pin. See shared pin description.* |
| 14 | VDD3 | PWR | Power for CPU(7:12) output buffers. Must be nominal 3.3V (3.0 to 3.7V) |
| 28, 27, 25, 24, 22, 21 | BUS (1:6) | OUT | BUS clock outputs which are a multiple of the input reference clock. |
| 23 | VDD4 | PWR | Power for BUS clock buffers BUS(1:6). |
| 29 | VDD5 | PWR | Power for fixed clock buffer (48 MHz, 24 Mhz). |
| 30 | 24MHz | OUT | Fixed 24MHz clock (assuming a 14.31818MHz REF frequency). |
| 31 | 48MHz | OUT | Fixed 48MHz clock (assuming a 14.31818MHz REF frequency). |
| 32 | REF | OUT | Fixed 14.31818MHz clock (assuming a 14.31818MHz REF frequency). |
| | BSEL | IN | Selection for synchronous or asynchronous bus clock operation. See shared pin programming description late in this data sheet for further explanation. |

* The internal pull-up will vary from 350K to 500K based on temperature.



Shared Pin Operation - Input/Output Pins

Shared Pin Operation - Input/Output Pins 5, 12, 13 and 32 on the ICS9169C-273 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 4-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operation for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kiloohm(10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figures 1 and 2 show the recommended PCB means of implementing this function. In Fig. 1 either one of the resistors is stuffed on the board (selective stuffing) to configure the device's internal logic. Figures 2a and b provide a single resistor stuffing option where either solder spot tabs or a physical jumper header may be used. These figures illustrate the optimal PCB physical layout options. These configuration resistors are of such a large ohmic value that they do not effect the low impedance clock signals. The layouts have been optimized to provide as little impedance transition to the clock signal as possible, as it passes through the programming resistor pad(s).

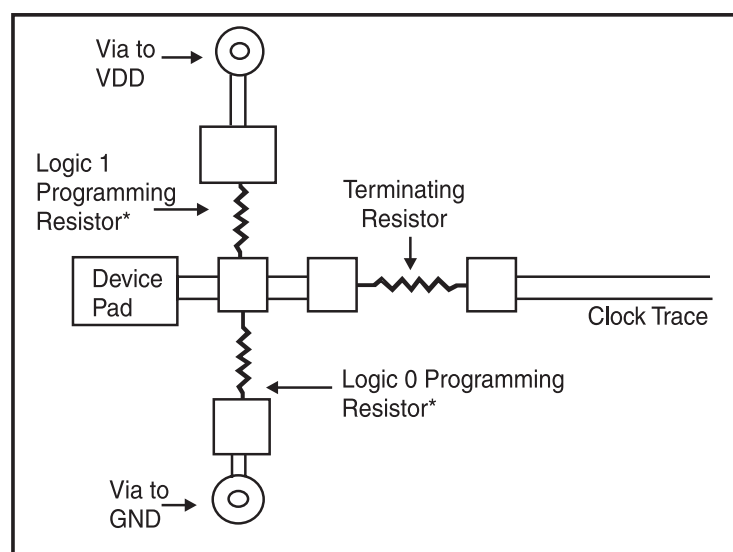


Fig. 1

Test Mode Operation

The ICS9169C-273 includes a production test verification mode of operation. This requires that the FSO and FS1 pins be programmed to a logic high and the FS2 pin be programmed to a logic low(see Shared Pin Operation section). In this mode the device will output the following frequencies.

| Pin | | Frequency |
|------------|----------|-----------|
| REF | | REF |
| 48MHz | | REF/2 |
| 24MHz | | REF/4 |
| CPU (1:12) | | REF2 |
| BUS (1:6) | BSEL=1 | REF/4 |
| | BSEL = 0 | REF/3 |

Note: REF is the frequency of either the crystal connected between the devices X1and X2 or, in the case of a device being driven by an external reference clock, the frequency of the reference (or test) clock on the device's X1 pin.

(Resistors are surface mount devices shown schematically between 5.m. pads)

*use only one programming resistor

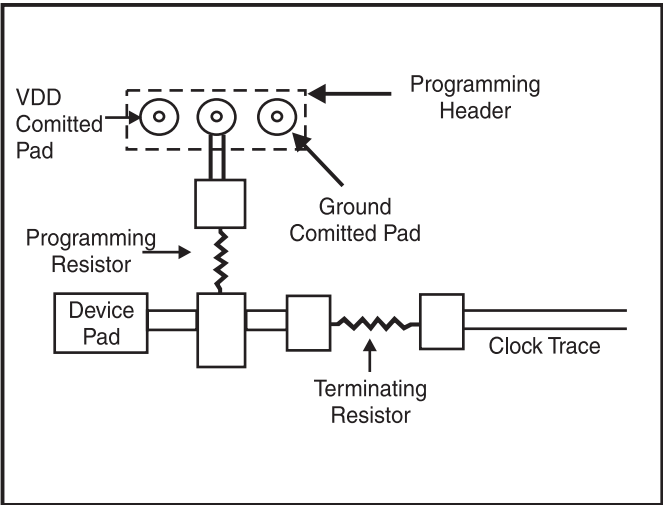


Fig. 2a

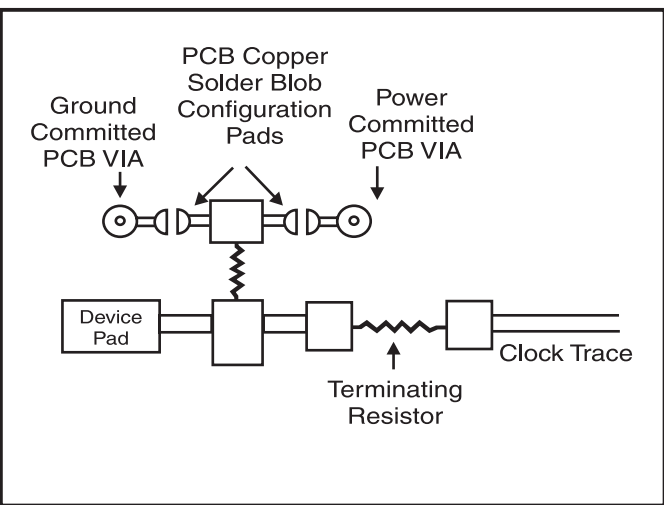


Fig. 2b

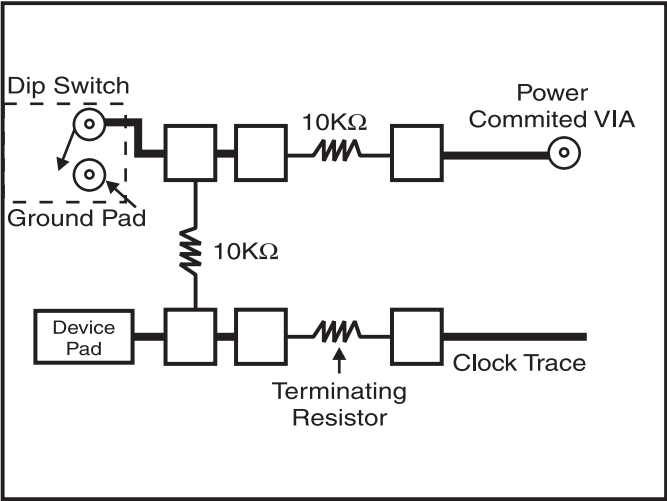


Fig. 3



Technical Pin Function Descriptions

VDD1

This is the power supply to the internal logic of the device as well as the following clock output buffers:

- A. REF clock output buffers
- B. BUS clock output buffers
- C. Fixed clock output buffers

This pin may be operated at any voltage between 3.0 and 5.5 volts. Clocks from the listed buffers that it supplies will have a voltage swing from ground to this level. For the actual guaranteed high and low voltage levels of these clocks, please consult the AC parameter table in this data sheet.

GND

This is the power supply ground return pin for the internal logic of the device as well as the following Clock Output buffers:

- A. REF clock output buffers
- B. BUS clock output buffers
- C. CPU clock output buffers
- D. Fixed clock output buffers
- E. 24/48MHz clock output buffers

X1

This pin serves one of two functions. When the device is used with a crystal, X1 acts as the input pin for the reference signal that comes from the discrete crystal. When the device is driven by an external clock signal, X1 is the device' input pin for that reference clock. This pin also implements an internal crystal loading capacitor that is connected to ground. See the data tables for the value of the capacitor.

X2

This pin is used only when the device uses a Crystal as the reference frequency source. In this mode of operation, X2 is an output signal that drives (or excites) the discrete crystal. This pin also implements an internal crystal loading capacitor that is connected to ground. See the data tables for the value of the capacitor.

CPU (1:12)

These pins are clock outputs that drive the processor and other CPU related circuitry that require clocks which are in tight skew tolerance with the CPU clock. The voltage swing of these clocks is controlled by that which is applied to the VDD pins of the device. See note on VDD3. See the Functionality Table at the beginning of this data sheet for a list of the specific frequencies that this clock operates at and the selection codes that are necessary to produce these frequencies.

BUS (1:6)

These pins are the Clock Outputs that are intended to drive the systems plug-in card bus. The voltage swing of these

clocks is controlled by the supply that is applied to the VDD pin of the group. See the Functionality Table at the beginning of this data sheet for a list of the specific frequencies that this clock operates at and the selection codes that are necessary to produce these frequencies.

FS0, FS1, FS2

These pins control the frequency of the clocks at the CPU, CPUL, BUS & SDRAM pins. See the Functionality table at the beginning of this data sheet for a list of the specific frequencies that this clock operates at and the selection codes that are necessary to produce these frequencies. The device reads these pins at power-up and stores the programmed selection code in an internal data latch. (See programming section of this data sheet for configuration circuitry recommendations.

BSEL

When this pin is a logic 1, it will place the CPU clocks in the synchronous mode (running at half the frequency of the Ref). If this pin is a logic 0, it will be in the asynchronous mode for the CPU clocks and will operate at the preprogrammed fixed frequency rate. It is a shared pin and is programed the same way as the frequency select pins.

VDD (2:3)

These are the power supply pins for the CPU (1:6) and CPU (7:12) clock buffers. By separating the clock power pins, each group can receive the appropriate power decoupling and bypassing necessary to minimize EMI and crosstalk between the individual signals. VDD2 can be reduced to 2.5V VDD for advanced processor clocks, which will bring CPU (1:6) outputs at 0 to 2.5V output swings.

VDD4

This is the power supply pin for BUS clock buffers BUS (1:6).

VDD5

This is the power supply pin for fixed clock buffer (48MHz and 24MHz).

48 MHz

This is a fixed frequency clock that is typically used to drive Super I/O peripheral device needs.

24 MHz

This is a fixed frequency clock that is typically used to drive Keyboard controller clock needs.

REF

This is a fixed frequency clock that runs at the same frequency as the input reference clock (typically 14.31818 MHz) is and typically used to drive Video and ISA BUS requirements.



Absolute Maximum Ratings

| | |
|-------------------------------------|--------------------------------|
| Supply Voltage | 7.0 V |
| Logic Inputs | GND –0.5 V to $V_{DD} + 0.5$ V |
| Ambient Operating Temperature | 0°C to +70°C |
| Storage Temperature | –65°C to +150°C |

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

$V_{DD} = 3.0 - 3.7$ V, $T_A = 0 - 70^\circ\text{C}$ unless otherwise stated

| DC Characteristics | | | | | | |
|----------------------------------|----------|--|-------------|-------|-------------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
| Input Low Voltage | V_{IL} | | - | - | $0.2V_{DD}$ | V |
| Input High Voltage | V_{IH} | | $0.7V_{DD}$ | - | - | V |
| Input Low Current | I_{IL} | $V_{IN} = 0$ V | -28.0 | -10.5 | - | μA |
| Input High Current | I_{IH} | $V_{IN} = V_{DD}$ | -5.0 | - | 5.0 | μA |
| Output Low Current ¹ | I_{OL} | $V_{OL} = 0.8$ V; for CPU, BUS, Fixed CLKs | 16.0 | 25.0 | - | mA |
| Output High Current ¹ | I_{OH} | $V_{OL} = 2.0$ V; for CPU, BUS, Fixed CLKs | - | -30.0 | -14 | mA |
| Output Low Current ¹ | I_{OL} | $V_{OL} = 0.8$ V; for REF CLK | 19.0 | 30.0 | - | mA |
| Output High Current ¹ | I_{OH} | $V_{OL} = 2.0$ V; for REF CLK | - | -38.0 | -16.0 | mA |
| Output Low Voltage ¹ | V_{OL} | $I_{OL} = 8$ mA; for CPU, BUS, Fixed CLKs | - | 0.3 | 0.4 | V |
| Output High Voltage ¹ | V_{OH} | $I_{OH} = -8$ mA; for CPU, BUS, Fixed CLKs | 2.4 | 2.8 | - | V |
| Output Low Voltage ¹ | V_{OL} | $I_{OL} = 10$ mA; for REF CLK | - | 0.3 | 0.4 | V |
| Output High Voltage ¹ | V_{OH} | $I_{OH} = -15$ mA; for REF CLK | 2.4 | 2.8 | - | V |
| Supply Current | I_{DD} | @66.6 MHz; all outputs unloaded | - | 90 | 180 | mA |

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

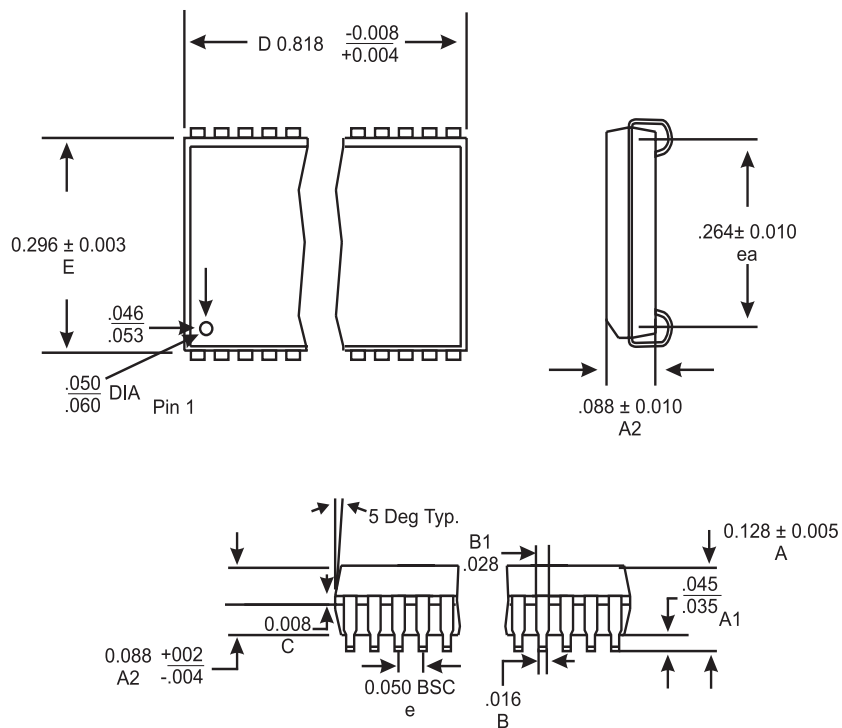


Electrical Characteristics at 3.3V

$V_{DD} = 3.0 - 3.7V$, $T_A = 0 - 70^\circ C$ unless otherwise stated

| AC Characteristics | | | | | | |
|---|------------|---|------|--------|------|-------|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
| Rise Time ¹ | T_{r1} | 20pF load, 0.8 to 2.0V CPU & BUS | - | 0.9 | 1.5 | ns |
| Fall Time ¹ | T_{f1} | 20pF load, 2.0 to 0.8V CPU & BUS | - | 0.8 | 1.4 | ns |
| Rise Time ¹ | T_{r2} | 20pF load, 20% to 80% CPU & BUS | - | 1.5 | 2.5 | ns |
| Fall Time ¹ | T_{f2} | 20pF load, 80% to 20% CPU & BUS | - | 1.4 | 2.4 | ns |
| Duty Cycle ¹ | D_t | 20pF load @ $V_{OUT}=1.4V$ | 45 | 50 | 60 | % |
| Jitter, One Sigma ¹ | T_{j1s1} | CPU & BUS Clocks; Load=20pF, BSEL=1 | - | 50 | 150 | ps |
| Jitter, Absolute ¹ | T_{jab1} | CPU & BUS Clocks; Load=20pF, BSEL=1 | -250 | - | 250 | ps |
| Jitter, One Sigma ¹ | T_{j1s2} | REF & Fixed CLK; Load=20pF | - | 1 | 3 | % |
| Jitter, Absolute ¹ | T_{jab2} | REF & Fixed CLK; Load=20pF | -5 | 2 | 5 | % |
| Input Frequency ¹ | F_i | | 12.0 | 14.318 | 16.0 | MHz |
| Logic Input Capacitance ¹ | C_{IN} | Logic input pins | - | 5 | - | pF |
| Crystal Oscillator Capacitance ¹ | C_{INX} | X1, X2 pins | - | 18 | - | pF |
| Power-on Time ¹ | t_{on} | From $V_{DD}=1.6V$ to 1st crossing of 66.6 MHz V_{DD} supply ramp < 40ms | - | 2.5 | 4.5 | ms |
| Clock Skew ¹ | T_{sk1} | CPU to CPU; Load=20pF; @1.4V | - | 150 | 250 | ps |
| Clock Skew ¹ | T_{sk2} | BUS to BUS; Load=20pF; @1.4V | - | 150 | 250 | ps |
| Clock Skew ¹ | T_{sk3} | CPU to BUS; Load=20pF; @1.4V (CPU is early) | 0 | 1.0 | 2 | ns |
| Clock Skew ¹ | T_{SR4} | CPU (@3.3V) to CPU (@2.5V) (2.5V CPU is late) | | 0.5 | 1 | ns |

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.



SOJ Package

Ordering Information

ICS9169CJ-273

Example:

ICS XXXX M-PPP

