



Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 7, 13, 27, 33	VDD	PWR	Power for control logic, PLL and output buffers.
2	X1	IN	XTAL or external reference frequency input. This input includes XTAL load capacitance and feedback bias for a 12 - 16 MHz crystal, nominally 14.31818 Mhz.
3	X2	OUT	XTAL output which includes XTAL load capacitance.
4, 10, 16, 23, 30	GND	PWR	Ground for logic, PLL and output buffers.
5, 6, 8, 9, 11, 12, 14, 15	CPU(1:8)	OUT	Processor clock outputs which are a multiple of the input reference frequency as shown in the table above.
17, 18, 19	FS(1:2)	IN	Frequency multiplier select pins. See table above. These inputs have internal pull-up devices.
20	BSEL	IN	Selector for synchronous or asynchronous bus operation.
21, 22, 24, 25, 26, 28, 29	BUS(1:7)	OUT	Bus clock outputs.
31	48MHz	OUT	Fixed 48 MHz clock (with 14.318 MHz input).
32	24MHz	OUT	Fixed 24 MHz clock (with 14.318 MHz input).
34, 35, 36	REF(1:3)	OUT	REF is a buffered copy of the crystal oscillator or reference input clock, nominally 14.31818 Mhz.



Absolute Maximum Ratings

Supply Voltage	7.0 V
Logic Inputs	GND –0.5 V to $V_{DD} + 0.5$ V
Ambient Operating Temperature	0°C to +70°C
Storage Temperature	–65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

$V_{DD} = 3.0 - 3.7$ V, $T_A = 0 - 70^\circ\text{C}$ unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	$0.2V_{DD}$	V
Input High Voltage	V_{IH}		$0.7V_{DD}$	-	-	V
Input Low Current	I_{IL}	$V_{IN}=0$ V	-28.0	-10.5	-	μA
Input High Current	I_{IH}	$V_{IN}=V_{DD}$	-5.0	-	5.0	μA
Output Low Current1	I_{OL}	$V_{OL}=0.8$ V; for CPUs & BUSes	30.0	47.0	-	mA
Output High Current1	I_{OH}	$V_{OL}=2.0$ V; for CPUs & BUSes	-	-66.0	-42.0	mA
Output Low Current1	I_{OL}	$V_{OL}=0.8$ V; for fixed CLKs	25.0	38.0	-	mA
Output High Current1	I_{OH}	$V_{OL}=2.0$ V; for fixed CLKs	-	-47.0	-30.0	mA
Output Low Voltage1	V_{OL}	$I_{OL}=15$ mA; for CPUs & BUSes	-	0.3	0.4	V
Output High Voltage1	V_{OH}	$I_{OH}=-30$ mA; for CPUs & BUSes	2.4	2.8	-	V
Output Low Voltage1	V_{OL}	$I_{OL}=12.5$ mA; for fixed CLKs	-	0.3	0.4	V
Output High Voltage1	V_{OH}	$I_{OH}=-20$ mA; for fixed CLKs	2.4	2.8	-	V
Supply Current	I_{DD}	@66.6 MHz; all outputs unloaded	-	55	110	mA

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.



Preliminary Product Preview

Electrical Characteristics at 3.3V

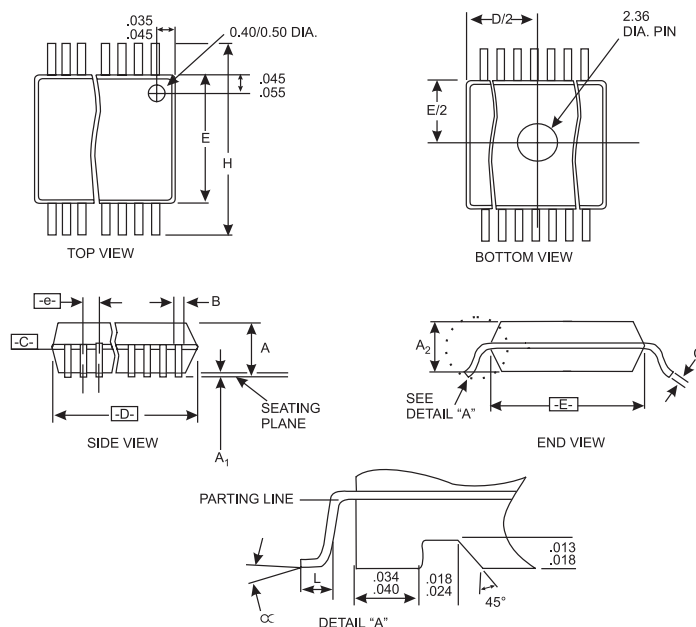
 $V_{DD} = 3.0 - 3.7\text{ V}$, $T_A = 0 - 70^\circ\text{C}$ unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time ¹	T_{r1}	20pF load, 0.8 to 2.0V CPU & BUS	-	0.9	1.5	ns
Fall Time ¹	T_{f1}	20pF load, 2.0 to 0.8V CPU & BUS	-	0.8	1.4	ns
Rise Time ¹	T_{r2}	20pF load, 20% to 80% CPU & BUS	-	1.5	2.5	ns
Fall Time ¹	T_{f2}	20pF load, 80% to 20% CPU & BUS	-	1.4	2.4	ns
Duty Cycle ¹	D_t	20pF load @ $V_{OUT}=1.4\text{V}$	45	50	55	%
Jitter, One Sigma ¹	T_{j1s1}	CPU & BUS Clocks; Load=20pF, >25 MHz	-	50	150	ps
Jitter, Absolute ¹	T_{jab1}	PCLK & BCLK Clocks; Load=20pF, FOUT>25 MHz	-200	-	200	ps
Jitter, One Sigma ¹	T_{j1s2}	Fixed CLK; Load=20pF	-	1	3	%
Jitter, Absolute ¹	T_{jab2}	Fixed CLK; Load=20pF	-5	2	5	%
Input Frequency ¹	F_i		12.0	14.318	16.0	MHz
Logic Input Capacitance ¹	C_{IN}	Logic input pins	-	5	-	pF
Crystal Oscillator Capacitance ¹	C_{INX}	X1, X2 pins	-	18	-	pF
Power-on Time ¹	t_{on}	From $V_{DD}=1.6\text{V}$ to 1st crossing of 66.6 MHz V_{DD} supply ramp < 40ms	-	2.5	4.5	ms
Frequency Settling Time ¹	t_s	From 1st crossing of acquisition to < 1% settling	-	2.0	4.0	ms
Clock Skew ¹	T_{sk1}	CPU to CPU; Load=20pF; @1.4V	-	150	250	ps
Clock Skew ¹	T_{sk2}	BUS to BUS; Load=20pF; @1.4V	-	300	500	ps
Clock Skew ¹	T_{sk3}	CPU & BUS; Load=20pF; @1.4V	1	2.6	4	ns

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.



Preliminary Product Preview



SSOP Package

SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.097	.101	.110	AA	.602	.607	.612	36
A1	.008	.010	.0116	AB	.701	.706	.711	44
A2	.090	.092	.094	AC	.620	.625	.630	48
B	.0091	.014	.017	AD	.720	.725	.730	56
C	.0091	.010	.0125					
D	See Variations							
E	.292	.296	.299					
e	.0315 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	See Variations							
∞	0°	5°	8°					
X	.085	.093	.100					

This table in inches

Ordering Information

ICS9169CF-26

Example:

ICS XXXX F - PPP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
F=SSOP

Device Type (consists of 3 or 4 digit numbers)

Prefix

ICS, AV = Standard Device