Integrated Circuit Systems, Inc.

ICS9169C-22

Preliminary Product Preview

Frequency Generator for Pentium™ Based Systems

General Description

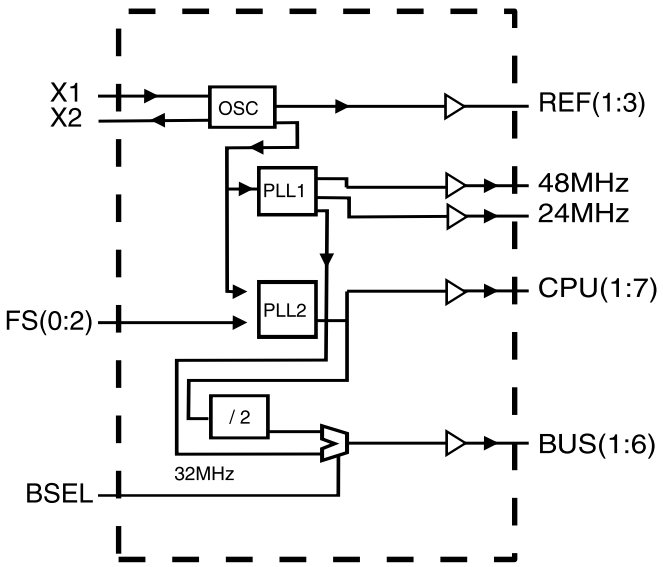
The **ICS9169C-22** is a low-cost frequency generator designed specifically for Pentium-based chip set systems. The integrated buffer minimizes skew and provides all the clocks required. A 14.318 MHz XTAL oscillator provides the reference clock to generate standard Pentium frequencies. The CPU clock makes gradual frequency transitions without violating the PLL timing of internal microprocessor clock multipliers.

Either synchronous (CPU/2) or asynchronous (32 MHz) PCI bus operation can be selected.

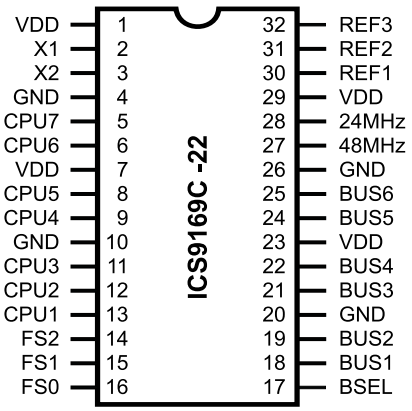
Features

- Seven selectable CPU clocks operate up to 83.3MHz
- Maximum CPU jitter of ±200ps
- Six BUS clocks support sync or async bus operation
- 500ps skew window for all synchronous clock edges
- CPU clocks to BUS clocks in sync mode skew 1-4 ns (CPU early)
- Integrated buffer outputs drive up to 30pF loads
- 3.0V - 3.7Vsupply range
- 32-pin SOIC package
- 48 MHz clock for USB support and 24 MHz clock for FD

Block Diagram



Pin Configuration



32-Pin SOIC

Functionality

3.3V±10%, 0-70°C
Crystal (X1, X2) = 14.31818 MHz

BSEL	FS2	FS1	FS0	CPU (1:7) MHz	BUS (1:6) MHz	48 MHz	24 MHz	REF (1:3)
0	0	0	0	55	27.5	48	24	14.318
0	0	0	1	80	40	48	24	14.318
0	0	1	0	100	50	48	24	14.318
0	0	1	1	75	37.5	48	24	14.318
0	1	0	0	50	25	48	24	14.318
0	1	0	1	66.6	33.3	48	24	14.318
0	1	1	0	60	30.0	48	24	14.318
0	1	1	1	Tristate	Tristate	Tristate	Tristate	Tristate
1	select	select	select	as above	32.0	48	24	14.318

Pentium is a trademark on Intel Corporation.

FS3	FS2	FS1	FS0	2XCPUCLK	CPUCLK	
0	0	0	0	4X Input	40MHz	FIN < 20 MHz
0	0	0	1	2X Input	33.33 MHz	
0	0	1	0	3X Input	25 MHz	
0	0	1	1	8X Input	20 MHz	
0	1	0	0	.5X Input	50 MHz*	
0	1	0	1	.75X Input	16.7 MHz	
0	1	1	0	5X Input		
0	1	1	1	7X Input		
1	0	0	0	64MHz	32 MHz	FIN ≥ 2.0 MHz
1	0	0	1	2X Input	Input	
1	0	1	0	3X Input	1.5X Input	
1	0	1	1	8X Input*	4X Input*	
1	1	0	0	.5X Input	.25X Input	
1	1	0	1	.25X Input	.125X Input	
1	1	1	0	5X Input		
1	1	1	1	7X Input		

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1,7,23,29	VDD	PWR	Power for logic, PLL and output buffers.
2	X1	IN	XTAL or external reference frequency input. This input includes XTAL load capacitance and feedback bias for a 12-16 MHz crystal, nominally 14.31818 Mhz.
3	X2	OUT	XTAL output which includes XTAL load capacitance.
4,10,20,26	GND	PWR	Ground for logic, PLL and output buffers.
5,6,8,9,11,12,13	CPU(1:7)	OUT	Processor clock outputs which are a multiple of the input reference frequency as shown in the table above.
14,15,16	FS(0:2)	IN	Frequency multiplier select pins. See table above. These inputs have internal pull up devices.
17	BSEL	IN	Selector for synchronous or asynchronous bus operation.
18,19,21,22,24,25	BUS(0:5) (1:6)	OUT	Bus clock outputs.
27	48MHz	OUT	Fixed 48 MHz clock (with 14.318 MHz input).
28	24MHz	OUT	Fixed 24 MHz clock (with 14.318 MHz input).
30,31,32	REF(0:2) (1:3)	OUT	REF is a buffered copy of the crystal oscillator or reference input clock, nominally 14.31818 MHz.

Absolute Maximum Ratings

Supply Voltage ..... 7.0 V

Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature ..... 0°C to +70°C

Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.7 V, T_A = 0 – 70° C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	0.2VDD	V
Input High Voltage	V_{IH}		0.7VDD	-	-	V
Input Low Current	I_{IL}	VIN=0V	-28.0	-10.5	-	µA
Input High Current	I_{IH}	VIN=VDD	-5.0	-	5.0	µA
Output Low Current[1]	I_{OL}	VOL=0.8V; for CPU & BUS	30.0	47.0	-	mA
Output High Current[1]	I_{OH}	VOL=2.0V; for CPU & BUS	-	-66.0	-42.0	mA
Output Low Current[1]	I_{OL}	VOL=0.8V; for fixed CLKs	25.0	38.0	-	mA
Output High Current[1]	I_{OH}	VOL=2.0V; for fixed CLKs	-	-47.0	-30.0	mA
Output Low Voltage[1]	V_{OL}	IOL=15mA; for CPU & BUS	-	0.3	0.4	V
Output High Voltage[1]	V_{OH}	IOH=-30mA; for CPU & BUS	2.4	2.8	-	V
Output Low Voltage[1]	V_{OL}	IOL=12.5mA; for fixed CLKs	-	0.3	0.4	V
Output High Voltage[1]	V_{OH}	IOH=-20mA; for fixed CLKs	2.4	2.8	-	V
Supply Current	I_{DD}	@66.6 MHz; all outputs unloaded	-	55	110	mA

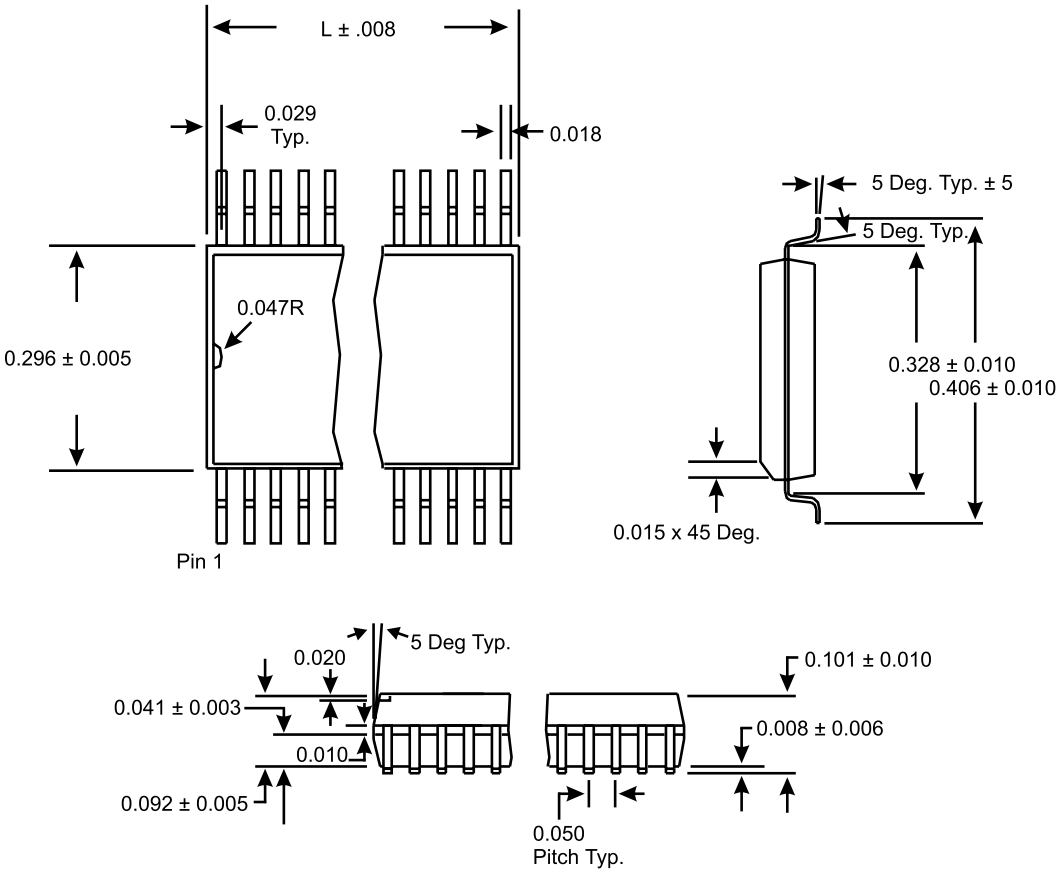
Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.7 V, T_A = 0 – 70° C unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time[1]	T_{r1}	20pF load, 0.8 to 2.0V CPU & BUS	-	0.9	1.5	ns
Fall Time[1]	T_{f1}	20pF load, 2.0 to 0.8V CPU & BUS	-	0.8	1.4	ns
Rise Time[1]	T_{r2}	20pF load, 20% to 80% CPU & BUS	-	1.5	2.5	ns
Fall Time[1]	T_{f2}	20pF load, 80% to 20% CPU & BUS	-	1.4	2.4	ns
Duty Cycle[1]	D_t	20pF load @ VOUT=1.4V	45	50	55	%
Jitter, One Sigma[1]	T_{j1s1}	CPU & BUS Clocks; Load=20pF, FOUT>25 Mhz	-	50	150	ps
Jitter, Absolute[1]	T_{jab1}	CPU & BUS Clocks; Load=20pF, FOUT>25 Mhz	-200	-	200	ps
Jitter, One Sigma[1]	T_{j1s2}	Fixed CLK; Load=20pF	-	1	3	%
Jitter, Absolute[1]	T_{jab2}	Fixed CLK; Load=20pF	-5	2	5	%
Input Frequency[1]	F_i		12.0	14.318	16.0	MHz
Logic Input Capacitance[1]	C_{IN}	Logic input pins	-	5	-	pF
Crystal Oscillator Capacitance[1]	C_{INX}	X1, X2 pins	-	18	-	pF
Power-on Time[1]	t_{on}	From VDD=1.6V to 1st crossing of 66.6 Mhz VDD supply ramp < 40ms	-	2.5	4.5	ms
Frequency Settling Time$_1$	t_s	From 1st crossing of acquisition to < 1% settling	-	2.0	4.0	ms
Clock Skew[1]	T_{sk1}	CPU & BUS; Load=20pF; @1.4V	-	150	250	ps
Clock Skew[1]	T_{sk}	BUS to BUS; Load=20pF; @1.4V	-	300	500	ps
Clock Skew[1]	T_{sk3}	CPU & BUS; Load=20pF; @1.4V	1	2.6	4	ns

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.



SOIC Package

LEAD COUNT	32L
DIMENSONL	.804

Ordering Information

ICS9169CM-22

Example:

ICS XXXX M - PPP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
M=SOIC

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV = Standard Device