Integrated Circuit Systems, Inc.

ICS9150-04

Pentium Pro™ and SDRAM Frequency Generator

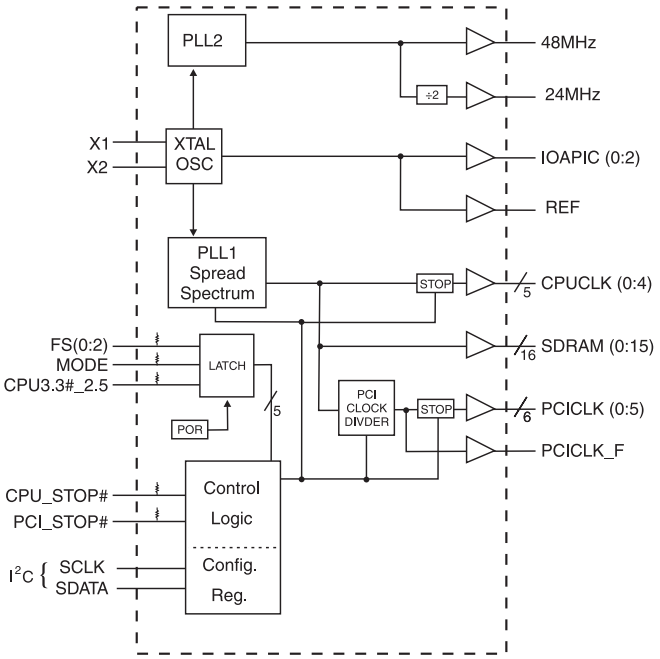
General Description

The **ICS9150-04** generates all clocks required for high speed RISC or CISC microprocessor systems such as Intel PentiumPro or Cyrix. Eight different reference frequency multiplying factors are selectable from 50 to 83.3MHz.

Features include five CPU, seven PCI and Sixteen SDRAM clocks. One reference output is available equal to the crystal frequency, plus three IOAPIC outputs powered by VDDL1. One 48 MHz for USB is provided plus a 24 MHz. Spread Spectrum built in up to ±1.5% modulation to reduce EMI. Serial programming I^2C interface allows changing functions, stop clock programing and Frequency selection. Rise time adjustment for VDD at 3.3V or 2.5V CPU. Additionally, the device meets the Pentium power-up stabilization, which requires that CPU and PCI clocks be stable within 2ms after power-up.

High drive PCICLK and SDRAM outputs typically provide greater than 1 V/ns slew rate into 30pF loads. CPUCLK outputs typically provide better than 1V/ns slew rate into 20pF loads while maintaining 50±5% duty cycle. The REF 24 and 48 MHz and SDRAM 12, 13 clock outputs typically provide better than 0.5V/ns slew rates.

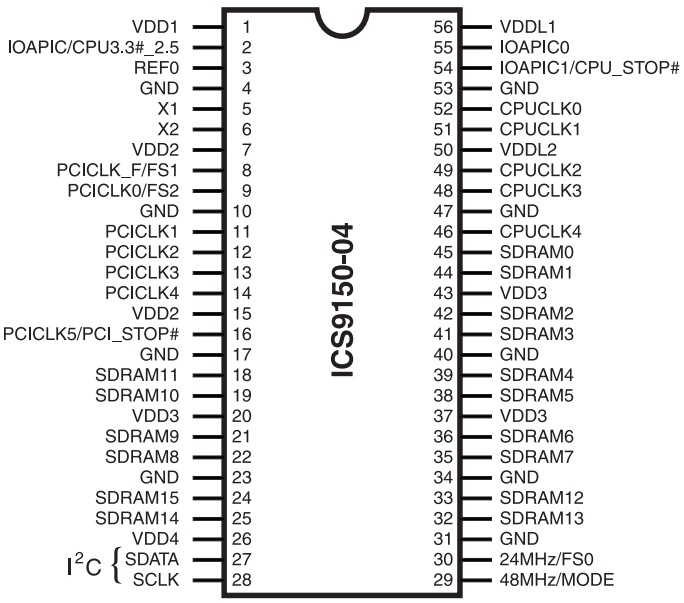
Block Diagram



Features

- Generates five processor, six bus, one 14.31818MHz (3.3V) three IOAPIC, 16 SDRAM clocks, 48MHz USB clock and 24MHz Super I/O clock.
- Synchronous clocks skew matched to 250 ps window on CPUCLKs and 500ps window on PCICLKs
- Skew from CPU (earlier) to PCI clock - 1 to 4ns, 2.6ns nom.
- Power Management Control Input pins when MODE Low
- VDD(1:4) - 3.3V ±10% (inputs 5V tolerant w/series R)
- VDDL(1:2) - 2.5V or 3.3V ±5%
- I^2C interface for programming stopclocks plus spread spectrum options (±0.5% or ±1.5%, center spread or down spread)
- 56-pin SSOP package

Pin Configuration



56-Pin SSOP

Power Groups

VDD1 = REF, X1, X2
VDD2 = PCICLK_F, PCICLK(0:5)
VDD3 = SDRAM (0:15), supply for PLL core,
VDD4 = 48MHz, 24MHz
VDDL1 = IOAPIC (0:2)
VDDL2 = CPUCLK (0:4)

Pentium is a trademark of Intel Corporation
I^2C is a trademark of Philips Corporation.

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
2	IOAPIC2	OUT	IOAPIC clock output (14.318MHz) powered by VDDL1
	CPU3.3#_2.5	IN	Indicates whether VDDL1 & VDDL2 are 3.3 or 2.5V. Output buffer strength compensates for VDDL selection to maintain CPU to SDRAM skew. High = 2.5V, Low = 3.3V. Has pull-up to VDDL1, must use series resistor for 3.3 or 5V logic levels.
3	REF0	OUT	14.318 MHz reference clock outputs.
4, 10, 17, 23, 31, 34, 40, 47, 53	GND	PWR	Ground.
5	X1	IN	14.318MHz input. Has internal load cap, (nominal 33pF).
6	X2	OUT	Crystal output. Has internal load cap (33pF) and feedback resistor to X1
8	PCICLK_F	OUT	Free running BUS clock during PCI_STOP#=0.
	FS1[1]	IN	Latched frequency select input. Has pull-up to VDD2.
9	PCICLK0	OUT	BUS clock output
	FS2[1]	IN	Latched frequency select input. Has pull-up to VDD2.
11, 12, 13, 14	PCICLK (1:4)	OUT	BUS clock outputs.
27	SDATA	IN	Serial data in for serial config port. (I^2C)
28	SCLK	IN	Clock input for serial config port. (I^2C)
30	24MHz	OUT	24MHz clock output for Super I/O or FD.
	FS0[1]	IN	Latched frequency select input. Has pull-up to VDD4.
29	48MHz	OUT	48MHz clock output for USB.
	MODE[1]	IN	Latched input for MODE select. Converts 2 outputs to power management CPU_STOP# and PCI_STOP# when low. Has pull-up to VDD4.
1, 7, 15, 20, 26, 37, 43	VDD2, VDD1, VDD3, VDD4	PWR	Nominal 3.3V power supply, see power groups for function.
50, 56	VDDL2, VDDL1	PWR	CPU and IOAPIC clock buffer power supply, either 2.5 or 3.3V nominal.
18, 19, 21, 22, 24, 25, 32, 33, 35, 36, 38, 39, 41, 42, 44, 45	SDRAM (0:15)	OUT	SDRAM clocks
55	IOAPIC0	OUT	IOAPIC clock output. (14.318 MHz) Poweredby VDDL1
46, 48, 49, 51, 52	CPUCLK (0:4)	OUT	CPU Output clocks. Powered by VDDL2 (60 or 66.6MHz)
54	IOAPIC1	OUT	IOAPIC clock output. (14.31818 MHz) Powered by VDDL1
	CPU_STOP#	IN	Halts CPUCLK clocks at logic "0" level when low. (in mobile, MODE=0)
16	PCICLK5	OUT	PCI BUS clock 5
	PCI_STOP#	IN	Halts PCICLK (0:4) at logic "0" level when low. (in mobile, MODE=0)

Notes:

1: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.

Definitions

5 Latched Inputs at Internal Power-On Reset:

	Pin shared as
MODE	48MHz/MODE
CPU3.3_2.5#V	IOAPIC2/CPU3.3#_2.5
FS0	24MHz/FS0
FS1	PCICLK_F/FS1
FS2	PCICLK0/FS2

2 Realtime Inputs

Pins 27, 28 - I^2C Serial input SDATA & SCLK

Pull-ups

2 pins with input latch or I/O have IOAPIC output function with VDDL1 which can be at 2.5V or 3.3V. These inputs will have to use series resistor (above 100Ω) to external VIN to be 3.3 & 5V logic input tolerant.

PMOS output stage provides input clamp diode to VDDL.

- Nwell resistor Pull-ups 100 to 150KΩ to local VDD
  (ie on IOAPIC pins use VDDL1, on FS1, 2 use VDD2, FS0=VDD4 and PCI_STOP#)

Functionality

V_{DD}1,2,3 = 3.3V±5%, V_{DDL}1,2 = 2.5V±5% or 3.3±5%, TA=0 to 70°C
Crystal (X1, X2) = 14.31818MHz

FS2	FS1	FS0	CPU, SDRAM(MHz)	PCICLK (MHz)	REF, IOAPIC (MHz)
1	1	1	66.8	33.4 (1/2 CPU)	14.318
1	1	0	60.0	30.0 (1/2 CPU)	14.318
1	0	1	75.0	37.5 (1/2 CPU)	14.318
1	0	0	83.3	33.3	14.318
0	1	1	68.5	34.25 (1/2 CPU)	14.318
0	1	0	83.3	41.65 (1/2 CPU)	14.318
0	0	1	75.0	32	14.318
0	0	0	50.0	25.0 (1/2 CPU)	14.318

Mode Pin - Power Management Input Control

MODE, Pin 55	Pin 54	Pin 16
0	CPU_STOP# Input	PCI_STOP# Input
1	IOAPIC1 Output	PCICLK5 Output

Power Management Functionality

CPU_STOP#	PCI_STOP#	CPUCLK Outputs	PCICLK(0:5) Outputs	PCICLK_F, REF, IOAPIC 48MHz and SDRAM	Crystal OSC	VCO
0	0	Stopped Low	Stopped Low	Running	Running	Running
0	1	Stopped Low	Running	Running	Running	Running
1	0	Running	Stopped Low	Running	Running	Running
1	1	Running	Running	Running	Running	Running

Spread Spectrum Functionality

BYTE0, Bit1 SS_EN	BYTE0, Bit2 SS_TYPE	BYTE0, Bit7	CPU, SDRAM and PCI CLOCKS	REF, IOAPIC	24,48MHz
1	0	0	Frequency modulated in center spread spectrum mode +1.5%, -1.5%	14.318MHz	24,48MHz
		1	Frequency modulated in center spread spectrum mode +0.5%, -0.5%	14.318MHz	24,48MHz
	1	0	Frequency modulated in down spread spectrum mode +0%, -3.0%	14.318MHz	24,48MHz
		1	Frequency modulated in down spread spectrum mode +0%, -1.0%	14.318MHz	24,48MHz
0	X	X	Normal, Steady frequency mode	14.318MHz	24,48MHz

CPU 3.3#_2.5V Buffer selector for CPUCLK driver.

CPU3.3#_2.5 Latched Input Level	Buffer Selected for Operation at:
1	2.5V VDD
0	3.3V VDD

Technical Pin Function Descriptions

VDD(1,2,3,4)
This is the power supply to the internal core logic of the device as well as the clock output buffers for REF, PCICLK, and SDRAM.

This pin operates at 3.3V volts. Clocks from the listed buffers that it supplies will have a voltage swing from Ground to this level. For the actual guaranteed high and low voltage levels for the Clocks, please consult the DC parameter table in this data sheet.

VDDL1,2
This is the power supply for the CPUCLK and IOAPIC output buffers. The voltage level for these outputs may be 2.5 or 3.3volts. Clocks from the buffers that each supplies will have a voltage swing from Ground to this level. For the actual Guaranteed high and low voltage levels of these Clocks, please consult the DC parameter table in this Data Sheet.

GND
This is the power supply ground (common or negative) return pin for the internal core logic and all the output buffers.

X1
This input pin serves one of two functions. When the device is used with a Crystal, X1 acts as the input pin for the reference signal that comes from the discrete crystal. When the device is driven by an external clock signal, X1 is the device input pin for that reference clock. This pin also implements an internal Crystal loading capacitor that is connected to ground. With nominal value of 33pF no external load cap is needed for a CL=17 to 18pF crystal.

X2
This Output pin is used only when the device uses a Crystal as the reference frequency source. In this mode of operation, X2 is an output signal that drives (or excites) the discrete Crystal. The X2 pin will also implement an internal Crystal loading capacitor that is nominally 33pF.

CPUCLK (0:4)
These Output pins are the Clock Outputs that drive processor and other CPU related circuitry that requires clocks which are in tight skew tolerance with the CPU clock. The voltage swing of these Clocks is controlled by the Voltage level applied to the VDDL2 pin of the device. See the Functionality Table for a list of the specific frequencies that are available for these Clocks and the selection codes to produce them.

SDRAM(0:15)
These Output Clocks are used to drive Dynamic RAM's and are low skew copies of the CPU Clocks. The voltage swing of the SDRAM's output is controlled by the supply voltage that is applied to VDD3 of the device. Operates at 3.3 volts.

IOAPIC (0:2)
These Outputs are fixed frequency Output Clocks that run at the Reference Input frequency (typically 14.31818MHz) . Its voltage level swing is controlled by VDDL1 and may operate at 2.5 or 3.3volts.

REF0
The REF Output is a fixed frequency Clock that runs at the same frequency as the Input Reference Clock X1 or the Crystal (typically 14.31818MHz) attached across X1 and X2.

PCICLK_F
This Output is equal to PCICLK(0:5). It is FREE RUNNING, and will not be stopped by PCI_STOP#.

PCICLK (0:5)
These Output Clocks generate all the PCI timing requirements for a Pentium/Pro based system. They conform to the current PCI specification. They run at 1/2 CPU frequency, for most choices of FS (0:2).

FS(0:2)
These Input pins control the frequency of the Clocks at the CPU, PCICLK and SDRAM output pins. These inputs are Bidirectional Input/Output pins, latched at internal power-on-reset.

MODE
This Input pin is used to select the Input function of the I/O pins. An active Low will place the I/O pins in the Input mode and enable the stop clock functions. (This is the Power Management Mode)

CPU_STOP#
This is a synchronous active Low Input pin used to stop the CPUCLK clocks in an active low state. All other Clocks including SDRAM clocks will continue to run while this function is enabled. The CPUCLK's will have a turn ON latency of at least 3 CPU clocks. This input pin valid only when MODE=0 (Power Management Mode)

PCI_STOP#
This is a synchronous active Low Input pin used to stop the PCICLK clocks in an active low state. It will not effect PCICLK_F nor any other outputs. This input pin valid only when MODE=0 (Power Management Mode)

I^2C (SDATA, SCLK)
The SDATA and SCLOCK Inputs are use to program the device. The clock generator is a slave-receiver device in the I^2C protocol. It will allow read-back of the registers. See configuration map for register functions. The I^2C specification in Philips I^2C Peripherals Data Handbook (1996) should be followed.

48MHz
This is a fixed frequency Clock output at 48MHz that is typically used to drive USB devices.

24MHz
This pin is a fixed frequency clock output typically used to drive Super I/O devices.

CPU_3.3#_2.5
This Input pin controls the CPU output buffer strength for skew matching CPU and SDRAM outputs to compensate for the external VDDL supply condition. It is important to use this function when selecting power supply requirements for VDDL1,2. A logic "1" (ground) will indicate 2.5V operation and a logic "0" will indicate 3.3V operation. This pin has an internal pullup resistor to VDD.

General I²C serial interface information

A. For the clock generator to be addressed by an I²C controller, the following address must be sent as a start sequence, with an acknowledge bit between each byte.

Clock Generator Address (7 bits)		+ 8 bits dummy command code		+ 8 bits dummy Byte count		Then Byte 0, 1, 2, etc in sequence until STOP.
A(6:0) & R/W#	ACK		ACK		ACK	
D2(H)						

B. The clock generator is a slave/receiver I²C component. It can "read back "(in Philips I²C protocol) the data stored in the latches for verification. (set R/W# to 1 above). There is no BYTE count supported, so it does not meet the Intel SMB PIIX4 protocol.

Clock Generator Address (7 bits)		Byte 0		Byte 1		Byte 0, 1, 2, etc in sequence until STOP.
A(6:0) & R/W#	ACK		ACK		ACK	
D3(H)						

C. The data transfer rate supported by this clock generator is 100K bits/sec (standard mode)

D. The input is operating at 3.3V logic levels.

E. The data byte format is 8 bit bytes.

F. To simplify the clock generator I²C interface, the protocol is set to use only block writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.

G The Fixed clocks 24, 48MHz are not addressable in the registers for Stopping. These outputs are always running, except in Tristate Mode.

H. At power-on, all registers are set to a default condition. See Byte 0 detail for default condition, Bytes 1 through 5 default to a 1 (Enabled output state)

Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default bits 0-3 to logic 0)

Bit	Description			PWD
Bit 7	0 - ±1.5% Spread Spectrum Modulation 1 - ±0.5% Spread Spectrum Modulation			0
Bit 6:4	Bit6 Bit5 Bit4	CPU clock	PCI	Note 1
	111	66.8	33.4(1/2 CPU)	
	110	60.0	30.0 (1/2 CPU)	
	101	75.0	37.5 (1/2 CPU)	
	100	83.3	33.3	
	011	68.5	34.5 (1/2 CPU)	
	010	83.3	41.65 (1/2 CPU)	
	001	75.0	32.0	
	000	50.0	25.0 (1/2 CPU)	
Bit 3	0 - Frequency is selected by hardware select, Latched Inputs 1 - Frequency is selected by Bit 6:4 (above)			0
Bit 2	0 - Spread Spectrum center spread type. (default) 1 - Spread Spectrum down spread type.			0
Bit 1 Bit 0	Bit1 Bit0 1 1 - Tri-State 1 0 - Spread Spectrum Enable 0 1 - Testmode 0 0 - Normal Operation			0 0

Note 1. Default at Power-up will be for latched logic inputs to define the frequency. Bits 4, 5, 6 are default to 000. If bit 3 is written to a 1 to use Bits 6:4, then these should be defined to the desired frequency at same write cycle.

Note: PWD = Power-Up Default

I²C is a trademark of Philips Corporation

Select Functions

FUNCTION DESCRIPTION	OUTPUTS				
	CPU	PCI, PCI_F	SDRAM	REF	IOAPIC
Tri - State	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Test Mode	TCLK/2[1]	TCLK/4[1]	TCLK/2[1]	TCLK[1]	TCLK[1]

Notes:
1. REF is a test clock on the X1 inputs during test mode.

Byte 1: CPU Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	46	1	CPUCLK4 (Act/Inact)
Bit 3	48	1	CPUCLK3 (Act/Inact)
Bit 2	49	1	CPUCLK2 (Act/Inact)
Bit 1	51	1	CPUCLK1 (Act/Inact)
Bit 0	52	1	CPUCLK0 (Act/Inact)

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 2: PCICLK Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	8	1	PCICLK_F (Act/Inact)
Bit 5	16	1	PCICLK5 (Act/Inact) Desktop Mode Only
Bit 4	14	1	PCICLK4 (Act/Inact)
Bit 3	13	1	PCICLK3 (Act/Inact)
Bit 2	12	1	PCICLK2 (Act/Inact)
Bit 1	11	1	PCICLK1 (Act/Inact)
Bit 0	9	1	PCICLK0 (Act/Inact)

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 3: SDRAM Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	35	1	SDRAM7 (Act/Inact)
Bit 6	36	1	SDRAM6 (Act/Inact)
Bit 5	38	1	SDRAM5 (Act/Inact)
Bit 4	39	1	SDRAM4 (Act/Inact)
Bit 3	41	1	SDRAM3 (Act/Inact)
Bit 2	42	1	SDRAM2 (Act/Inact)
Bit 1	44	1	SDRAM1 (Act/Inact)
Bit 0	45	1	SDRAM0 (Act/Inact)

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 4: SDRAM Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	24	1	SDRAM15 (Act/Inact)
Bit 6	25	1	SDRAM14 (Act/Inact)
Bit 5	32	1	SDRAM13 (Act/Inact)
Bit 4	33	1	SDRAM12 (Act/Inact)
Bit 3	18	1	SDRAM11 (Act/Inact)
Bit 2	19	1	SDRAM10 (Act/Inact)
Bit 1	21	1	SDRAM9 (Act/Inact)
Bit 0	22	1	SDRAM8 (Act/Inact)

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 5: Peripheral Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	2	1	IOAPIC2 (Act/Inact)
Bit 5	54	1	IOAPIC1 (Act/Inact) Desktop Mode Only
Bit 4	55	1	IOAPIC0 (Act/Inact)
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	3	1	REF0 (Act/Inact)

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 6: Peripheral Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserve

Notes:
1. Byte 6 is reserved by Integrated Circuit Systems for future applications.

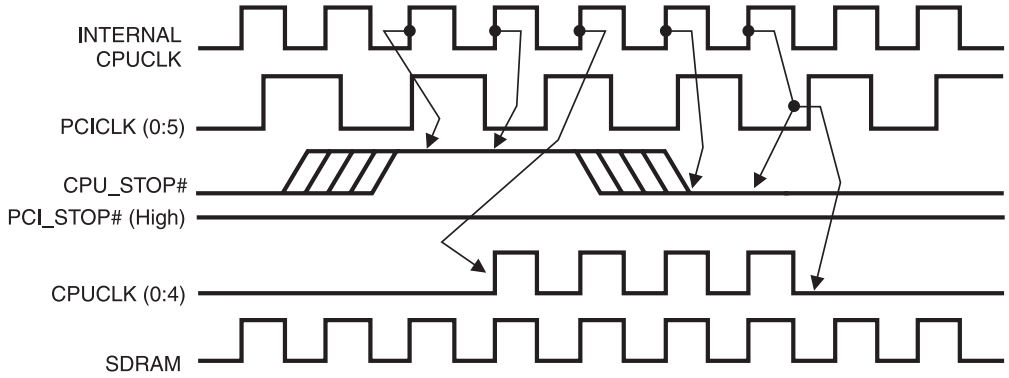
ICS9150-04 Power Management Requirements

SIGNAL	SIGNAL STATE	Latency No. of rising edges of free running PCICLK
CPU_ STOP#	0 (Disabled)[2]	1
	1 (Enabled)[1]	1
PCI_STOP#	0 (Disabled)[2]	1
	1 (Enabled)[1]	1

Notes.
1. Clock on latency is defined from when the clock enable goes active to when the first valid clock comes out of the device.
2. Clock off latency is defined from when the clock enable goes inactive to when the last clock is driven low out of the device.

CPU_STOP# Timing Diagram

CPUSTOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. CPU_STOP# is synchronized by the **ICS9150-04**. The minimum that the CPUCLK is enabled (CPU_STOP# high pulse) is 100 CPUCLKs. All other clocks will continue to run while the CPUCLKs are disabled. The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.

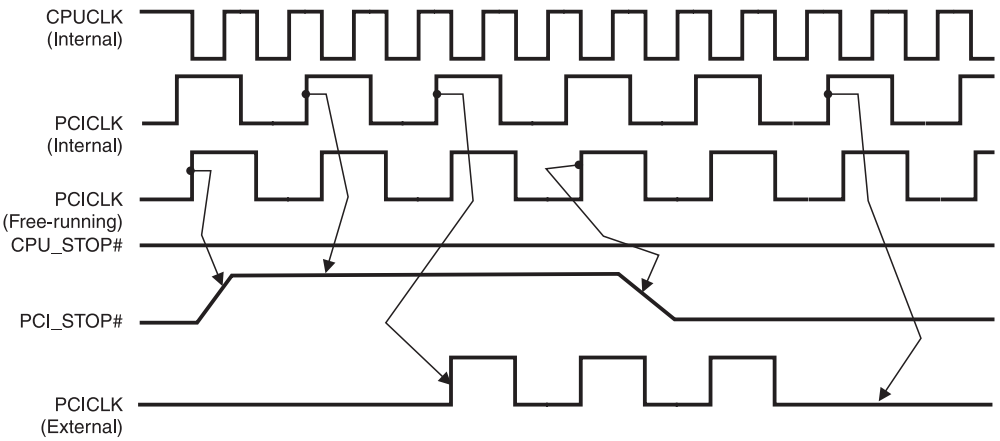


Notes:

1. All timing is referenced to the internal CPUCLK.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the **ICS9150-04.**
3. All other clocks continue to run undisturbed.
4. PCI_STOP# is shown in a high (true) state.

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9150-04**. It is used to turn off the PCICLK (0:5) clocks for low power operation. PCI_STOP# is synchronized by the **ICS9150-04** internally. The minimum that the PCICLK (0:5) clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK (0:5) clocks. PCICLK (0:5) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:5) clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9150 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9150.
3. All other clocks continue to run undisturbed.
4. CPU_STOP# is shown in a high (true) state.

Shared Pin Operation - Input/Output Pins

Pins 2, 8, 9, 29 and 30 on the **ICS9150-04** serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 4-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm(10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figs. 1 and 2 show the recommended means of implementing this function. In Fig. 1 either one of the resistors is loaded onto the board (selective stuffing) to configure the device's internal logic. Figs. 2a and b provide a single resistor loading option where either solder spot tabs or a physical jumper header may be used.

These figures illustrate the optimal PCB physical layout options. These configuration resistors are of such a large ohmic value that they do not effect the low impedance clock signals. The layouts have been optimized to provide as little impedance transition to the clock signal as possible, as it passes through the programming resistor pad(s).

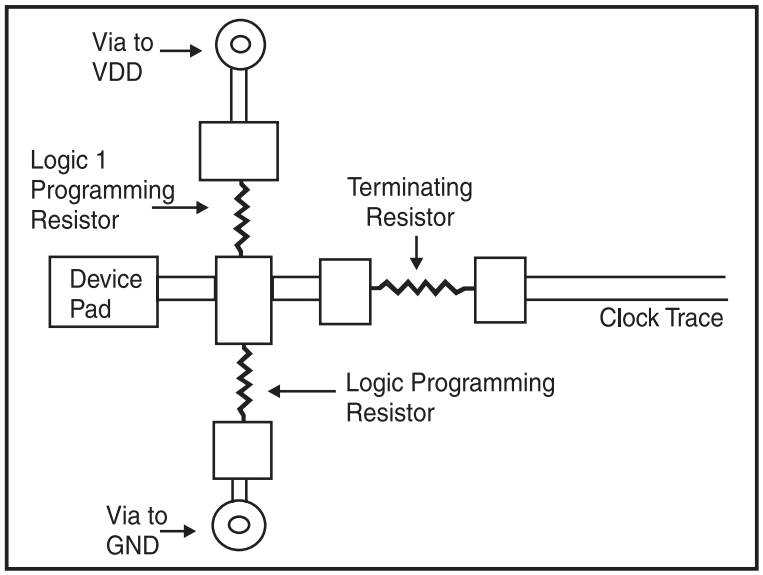


Fig. 1

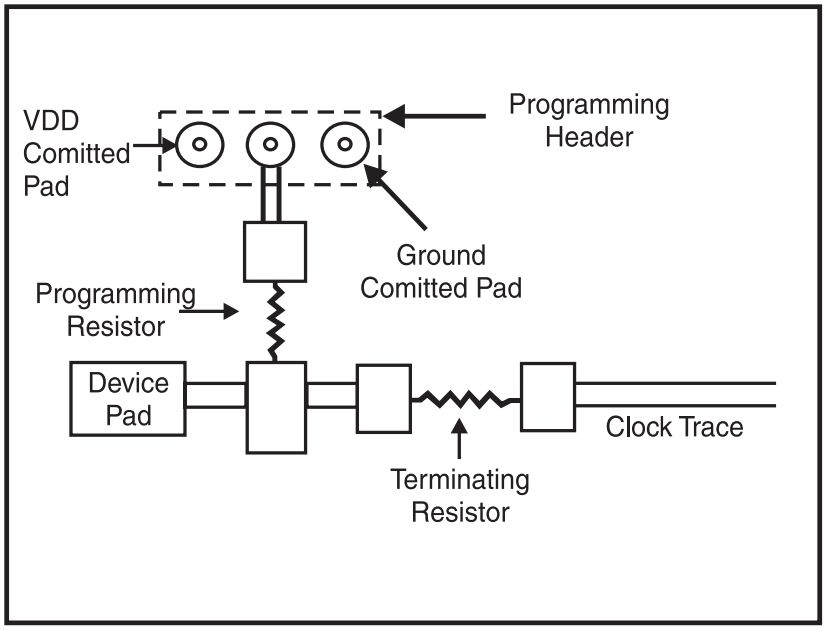

VDD
Comitted
Pad
Programming
Header
Ground
Comitted Pad
Programming
Resistor
Device
Pad
Clock Trace
Terminating
Resistor

Fig. 2a

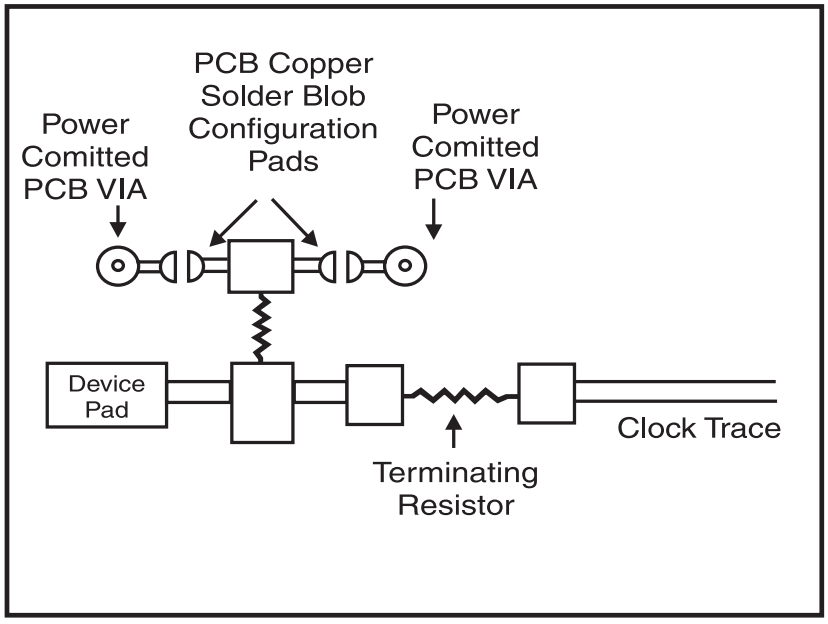

PCB Copper
Solder Blob
Configuration
Pads
Power
Comitted
PCB VIA
Power
Comitted
PCB VIA
Device
Pad
Clock Trace
Terminating
Resistor

Fig. 2b

Absolute Maximum Ratings

Supply Voltage ..... 7.0 V
Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = V_{DDL} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}		0.1	5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5	2.0		µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200	-100		µA
Operating Supply Current	$I_{DD3.3OP}$	C_L = 0 pF; Select @ 66MHz		135	160	mA
Input frequency	F_i	V_{DD} = 3.3 V;		14.318		MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			2	ms
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.				ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			2	ms
Skew[1]	$T_{CPU-SDRAM1}$	V_T = 1.5 V; V_{DD} = 3.3; 66.8 MHz; SDRAM Leads		200	350	ps
	$T_{CPU-PCI1}$	V_T = 1.5 V;	1	2.2	4	ns

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = V_{DDL} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current Skew[1]	$I_{DD2.5OP}$	C_L = 0 pF; Select @ 66M		5	30	mA
	$T_{CPU-SDRAM2}$	V_T = 1.5V; V_{TL} = 1.25V; V_{DDL} = 2.5; 66.8MHz; SDRAM Leads		500	800	ps
	$T_{CPU-PCI2}$	V_T = 1.5V; V_{TL} = 1.25V; CPU Leads	1	2.5	4	ns

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	RDSP2B[1]	$V_O = V_{DD}*(0.5)$	10		25	Ω
Output Impedance	RDSN2B[1]	$V_O = V_{DD}*(0.5)$	10		25	Ω
Output High Voltage	VOH2B	I_{OH} = -8 mA	2	2.2		V
Output Low Voltage	VOL2B	I_{OL} = 12 mA		0.3	0.4	V
Output High Current	IOH2B	V_{OH} = 2.0 V		-20	-16	mA
Output Low Current	IOL2B	V_{OL} = 0.7 V	19	26		mA
Rise Time	tr2B[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V		2.5	3	ns
Fall Time	tf2B[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1.6	2	ns
Duty Cycle	dt2B[1]	V_T = 1.25 V	43	46	55	%
Skew	tsk2B[1]	V_T = 1.25 V		60	250	ps
Jitter, Single Edge Displacement[2]	tjsed2B[1]	V_T = 1.25 V		200	300	ps
Jitter, One Sigma	tj1s2B[1]	V_T = 1.25 V		80	150	ps
Jitter, Absolute	tjabs2B[1]	V_T = 1.25 V	-300	80	300	ps

[1] Guaranteed by design, not 100% tested in production.

2 Edge displacement of a period relative to a 10-clock-cycle rolling average period.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-10%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2A}[1]	$V_O = V_{DD}*(0.5)$	10		20	Ω
Output Impedance	R_{DSN2A}[1]	$V_O = V_{DD}*(0.5)$	10		20	Ω
Output High Voltage	V_{OH2A}	I_{OH} = -28 mA	2.5	2.6		V
Output Low Voltage	V_{OL2A}	I_{OL} = 27 mA		0.35	0.4	V
Output High Current	I_{OH2A}	V_{OH} = 2.0 V		-29	-23	mA
Output Low Current	I_{OL2A}	V_{OL} = 0.8 V	33	37		mA
Rise Time	t_{r2A}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.9	2.5	ns
Fall Time	t_{f2A}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.4	2	ns
Duty Cycle	d_{t2A}[1]	V_T = 1.5 V	45	48	55	%
Skew	t_{sk2A}[1]	V_T = 1.5 V		80	250	ps
Jitter, Single Edge Displacement[2]	tjsed2A[1]	V_T = 1.25 V		200	250	ps
Jitter, One Sigma	t_{j1s2A}[1]	V_T = 1.5 V		60	150	ps
Jitter, Absolute	t_{jabs2A}[1]	V_T = 1.5 V	-300	200	300	ps

Electrical Characteristics - PCI

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-10%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -28 mA	2.4	3		V
Output Low Voltage	V_{OL1}	I_{OL} = 23 mA		0.2	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-60	-40	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	41	50		mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.4	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.3	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	49	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		80	500	ps
Jitter, One Sigma[1]	t_{j1s1}	V_T = 1.5 V, synchronous, excluding select 4		30	150	ps
	t_{j1s1a}	V_T = 1.5 V, synchronous, select 4		385	550	ps
	t_{j1s1b}	V_T = 1.5 V, asynchronous, select 1		175	250	ps
Jitter, Absolute[1]	t_{jabs1}	V_T = 1.5 V, synchronous, excluding select 4	-250	100	250	ps
	t_{j1s1a}	V_T = 1.5 V, synchronous, select 4	-700	510	700	ps
	t_{jabs1b}	V_T = 1.5 V, asynchronous, select 1	-500	390	500	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-10%; C_L = 20 - 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP3}[1]	$V_O = V_{DD}*(0.5)$	10		24	Ω
Output Impedance	R_{DSN3}[1]	$V_O = V_{DD}*(0.5)$	10		24	Ω
Output High Voltage	V_{OH3}	I_{OH} = -28 mA (except SDRAM12,13)	2.4	3		V
	V_{OH3a}	I_{OH} = -16 mA (SDRAM12,13)	2.4	2.6		V
Output Low Voltage	V_{OL3}	I_{OL} = 23 mA (except SDRAM12,13)		0.2	0.4	V
	V_{OL3a}	I_{OL} = 9 mA (SDRAM12,13)		0.3	0.4	V
Output High Current	I_{OH3}	V_{OH} = 2.0 V (except SDRAM12,13)		-60	-40	mA
	I_{OH3a}	V_{OH} = 2.0 V (SDRAM12,13)		-32	-22	mA
Output Low Current	I_{OL3}	V_{OL} = 0.8 V (except SDRAM12,13)	41	50		mA
	I_{OL3a}	V_{OL} = 0.8 V (SDRAM12,13)	16	25		mA
Rise Time	T_{r3}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 (except SDRAM12,13)		1.2	2	ns
	T_{r3a}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V (SDRAM12,13)		2.5	4	ns
Fall Time	T_{f3}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 (except SDRAM12,13)		1.1	2	ns
	T_{f3a}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V (SDRAM12,13)		2.7	4	ns
Duty Cycle	D_{t3}[1]	V_T = 1.5 V	45	51	57	%
Skew	T_{sk3}[1]	V_T = 1.5 V (except SDRAM12,13)		285	500	ps
Jitter, One Sigma	T_{j1s3}[1]	V_T = 1.5 V		50	150	ps
Jitter, Absolute	T_{jabs3}[1]	V_T = 1.5 V	-250	-	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP4B}[1]	$V_O = V_{DD}*(0.5)$	10		30	Ω
Output Impedance	R_{DSN4B}[1]	$V_O = V_{DD}*(0.5)$	10		30	Ω
Output High Voltage	$V_{OH4\B}$	I_{OH} = -8 mA	2	2.1		V
Output Low Voltage	V_{OL4B}	I_{OL} = 12 mA		0.3	0.4	V
Output High Current	I_{OH4B}	V_{OH} = 1.7 V		-20	-16	mA
Output Low Current	I_{OL4B}	V_{OL} = 0.7 V	19	26		mA
Rise Time	t_{r4B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1.9	4	ns
Fall Time	t_{f4B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1.5	3.2	ns
Duty Cycle	d_{t4B}[1]	V_T = 1.25 V	45	53	55	%
Skew	t_{sk4B}[1]	V_T = 1.25 V		60	250	ps
Jitter, One Sigma	t_{j1s4B}[1]	V_T = 1.25 V		1	3	%
Jitter, Absolute	t_{jabs4B}[1]	V_T = 1.25 V	-5		5	%

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-10%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O4}			14.318		MHz
Output Impedance	R_{DSP4A}[1]	$V_O = V_{DD}*(0.5)$	10		30	Ω
Output Impedance	R_{DSN4A}[1]	$V_O = V_{DD}*(0.5)$	10		30	Ω
Output High Voltage	V_{OH4A}	I_{OH} = -16 mA	2.4	2.6		V
Output Low Voltage	V_{OL4A}	I_{OL} = 9 mA		0.3	0.4	V
Output High Current	I_{OH4A}	V_{OH} = 2.0 V		-32	-22	mA
Output Low Current	I_{OL4A}	V_{OL} = 0.8 V	16	25		mA
Rise Time	t_{r4A}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.8	4	ns
Fall Time	t_{f4A}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		2.2	4	ns
Duty Cycle	d_{t4A}[1]	V_T = 1.5 V	45	53	57	%
Skew	t_{sk4A}[1]	V_T = 1.25 V		60	250	ps
Jitter, One Sigma	t_{j1s4A}[1]	V_T = 1.5 V		1	3	%
Jitter, Absolute	t_{jabs4A}[1]	V_T = 1.5 V	-5	-	5	%

[1]Guaranteed by design, not 100% tested in production.

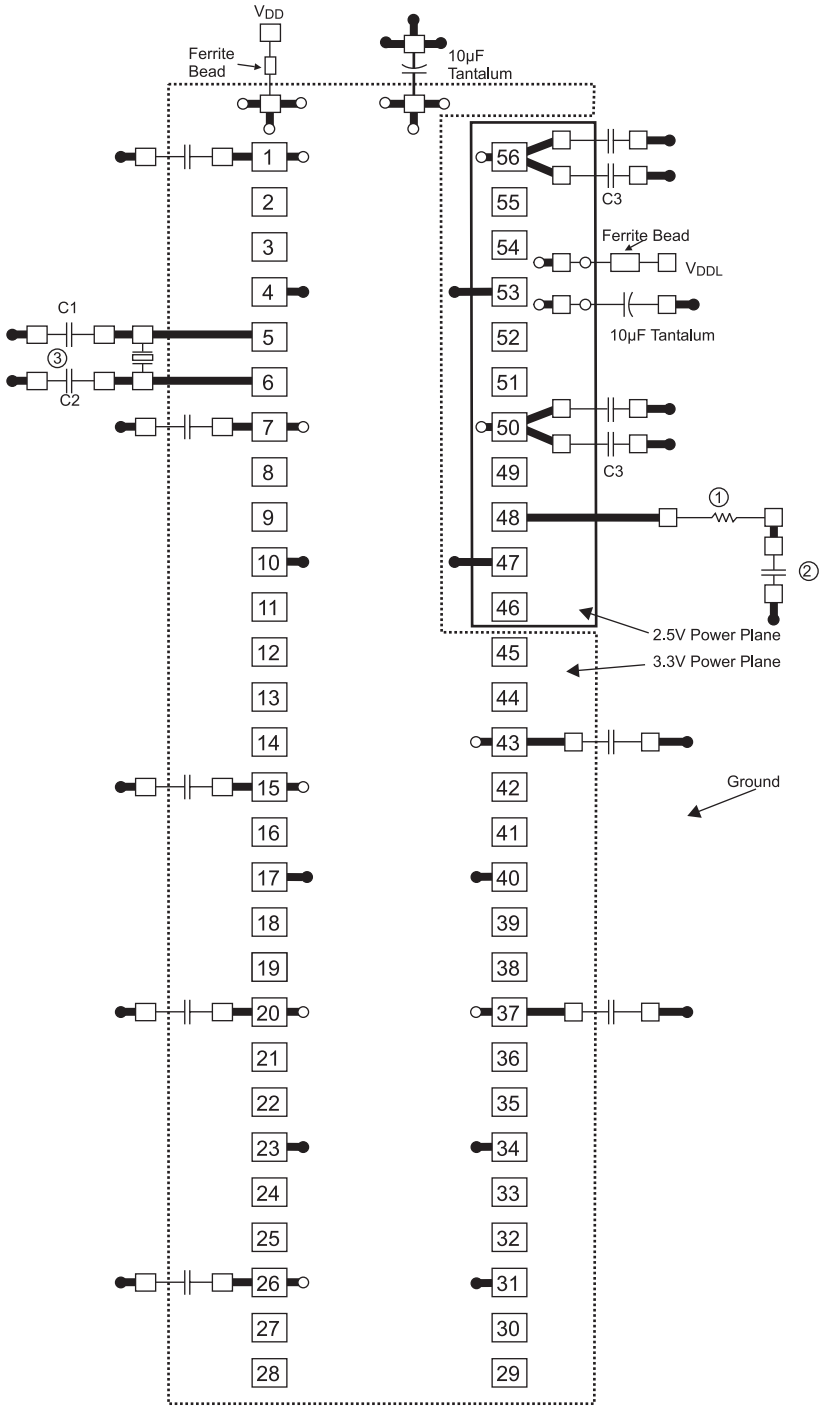
Electrical Characteristics - 24MHz, 48MHz, REF0

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-10%; C_L = 10 -20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O24M}			24		MHz
Output Frequency	F_{O48M}			48		MHz
Output Frequency	F_{OREF}			14.318		MHz
Output Impedance	R_{DSP5}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output Impedance	R_{DSN5}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH5}	I_{OH} = -16 mA	2.4	2.6		V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA		0.3	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-32	-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16	25		mA
Rise Time	t_{r5}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.7	4	ns
Fall Time	t_{f5}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		2.1	4	ns
Duty Cycle	d_{t5}[1]	V_T = 1.5 V	45	54	57	%
Jitter, One Sigma	t_{j1s5}[1]	V_T = 1.5 V		1	3	%
Jitter, Absolute	t_{jabs5}[1]	V_T = 1.5 V	-5	-	5	%

[1]Guaranteed by design, not 100% tested in production.

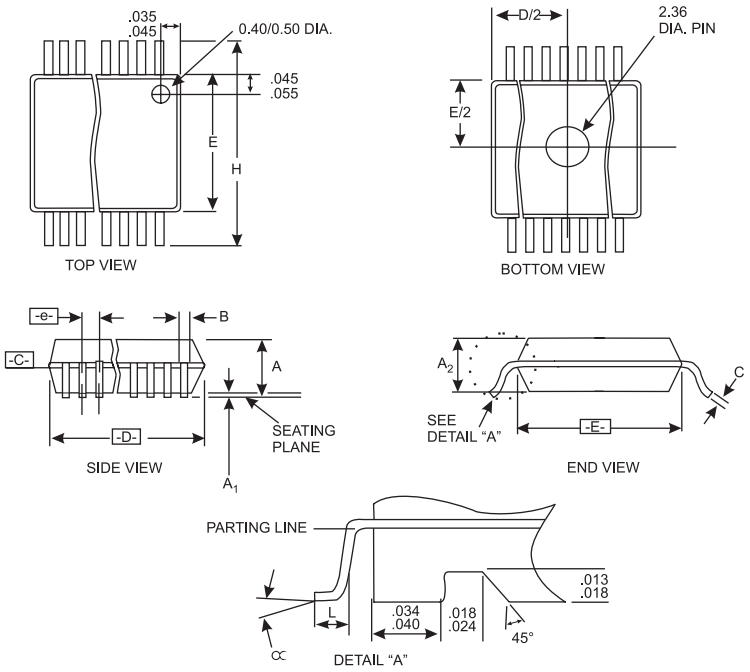
General Layout Precautions:
1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
2) Make all power traces and vias as wide as possible to lower inductance.



Notes:
1 All clock outputs should have series terminating resistor. Not shown in all places to improve readibility of diagram
2 Optional EMI capacitor should be used on all CPU, SDRAM, and PCI outputs.
3 Optional crystal load capacitors are recommended.

Capacitor Values:
C1, C2 : Crystal load values determined by user
C3 : 100pF ceramic
All unmarked capacitors are 0.01µF ceramic

● = Ground Plane Connection
○ = Power Plane Conncetion
□ = Solder Pads



SSOP Package

SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.101	.110	AC	.620	.625	.630	48
A1	.008	.012	.016	AD	.720	.725	.730	56
A2	.088	.090	.092					
B	.008	.010	.0135					
C	.005	-	.010					
D	See Variations							
E	.292	.296	.299					
e	0.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	See Variations							
∝	0°	5°	8°					
X	.085	.093	.100					

Ordering Information

ICS9150F-04

Example:

ICS XXXX F - PPP

- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device