Dual Voltage Video/Memory Clock Generator

Introduction

The Integrated Circuit Systems **ICS90C65** is a dual clock generator for VGA applications. It simultaneously generates two clocks. One clock is for the video memory, and the other is the video dot clock.

The **ICS90C65** has been specifically designed to serve the portable PC market with operation at either 3.3V or 5V with a comprehensive power-saving shut-down mode.

This data sheet supplies sales order information, a functional overview, signal pin details, a block diagram, AC/DC characteristics, timing diagrams, and package mechanical information.

Description

The Integrated Circuit Systems Video Graphics Array Clock Generator (**ICS90C65)** is capable of producing different output frequencies under firmware control. The video output frequency is derived from a 14.318 MHz system clock available in IBM PC/XT/AT and Personal System/2 computers. It is designed to work with Western Digital Imaging Video Graphics Array and 8514/A devices to optimize video subsystem performance.

The video dot clock output may be one of 15 internally-generated frequencies or one external input. The selection of the video dot clock frequency is done through four inputs.

- VSEL0
- VSEL1
- VSEL2
- VSEL3

VSEL0 and VSEL1 are latched by the SELEN signal. VSEL2 and VSEL3 are used as direct inputs to the VCLK selection. Table 1-1 is the truth table for VCLK selection.

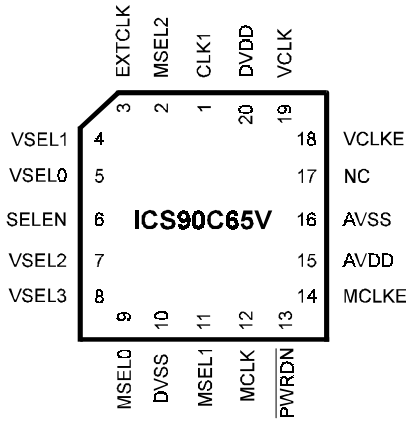
The input and truth table have been designed to allow a direct connection to one of the many Western Digital Imaging VGA controllers or 8514/A chip sets.

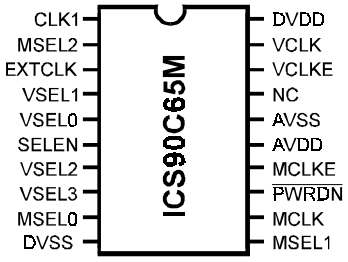
The MCLK output is one of eight internally-generated frequencies as shown in Table 1-2. The various VCLK and MCLK frequencies are derived from the 14.318 MHz input frequency.

The VCLKE and MCLKE input can tristate the VCLK and MCLK outputs to facilitate board level testing.

Features

- Specified for dual voltage operation (V_{DD}=3.3V or 5V), but operates continuously from 3.0V to 5.25V
- Designed to be powered-down for extended battery life
- Backward compatibility to the ICS90C64 and ICS90C63
- Dual Clock generator for the IBM-compatible Western Digital Imaging Video Graphics Array (VGA) LSI devices, and 8514/A chip sets
- Integral loop filter components, reduce cost and phase jitter
- Generates fifteen video clock frequencies (including 25.175 and 28.322 MHz) derived from a 14.318 MHz system clock reference frequency
- On-chip generation of eight memory clock frequencies
- Video clock is selectable among the 15 internally generated clocks and one external clock
- CMOS technology
- Available in 20-pin PLCC, SOIC and DIP packages





Note:ICS90C65N (DIP) pin-out is identical to ICS90C65M (SOIC) pin-out.

ICS90C65 VGA Interface

The **ICS90C65** has two system interfaces: System Bus and VGA Controller, as well as other programmable inputs. Figure 1 shows how the Integrated Circuit Systems's VGA Clock **ICS90C65** is connected to a VGA controller. Western Digital Imaging VGA controllers normally have a status bit that indicates to the VGA controller that it is working with a clock chip. When working with a clock chip the VGA controller changes two of its clock inputs to outputs. They are theVCLK1/VCSLD/VCSEL and VCLK2/VCSEL/VCSELH outputs and they are used to select the required video frequency.

When the power-down capabilities are used, the control signal for $\overline{\text{PWRDN}}$ is normally held in one of a group of latches. If the power-down function is not to be used, ***PWRDN must be tied to V_{DD},*** otherwise the internal pull-down will place the chip in the power-down mode.

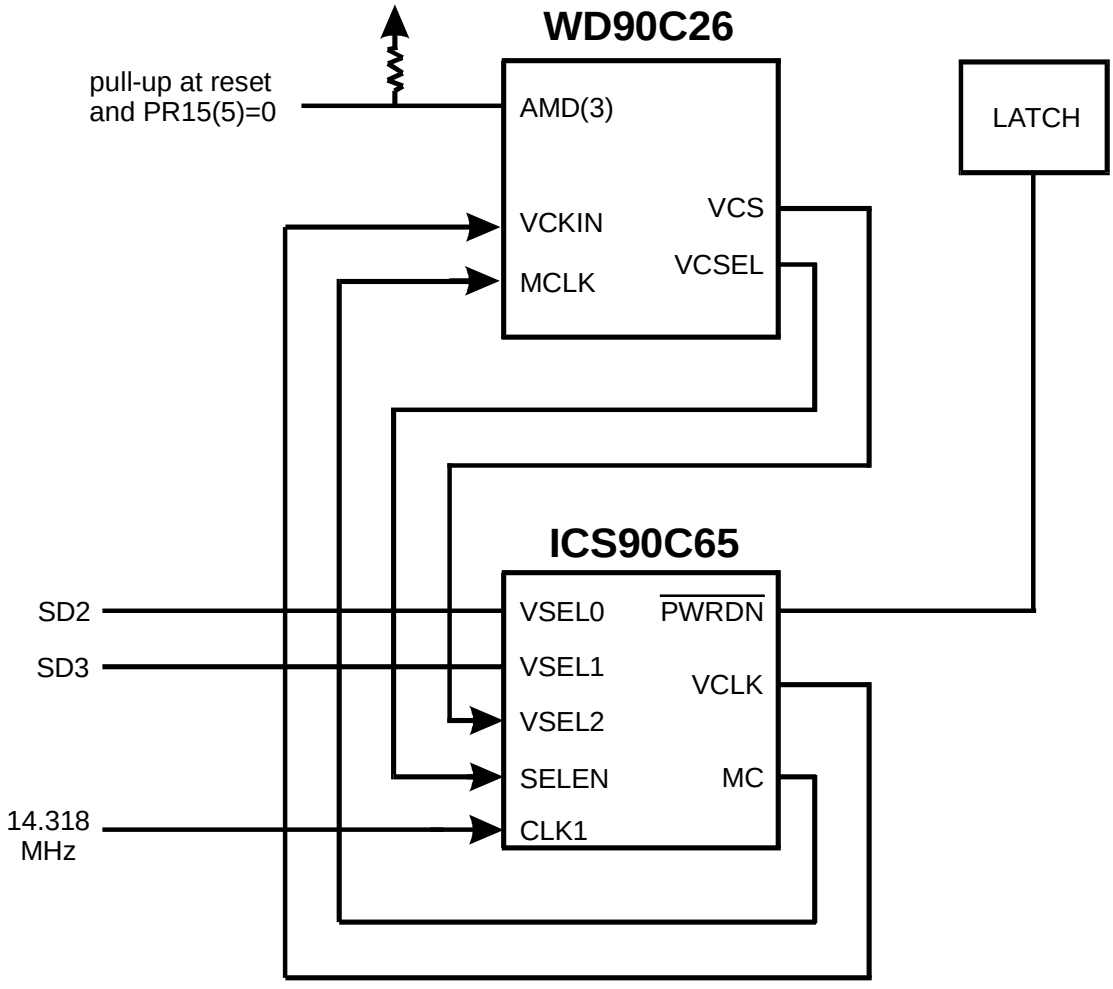


Figure 1

System Bus Inputs

The system bus inputs are:

- CLKI
- VSEL0
- VSEL1

The **ICS90C65** uses the system bus 14.318 MHz clock as a reference to generate all its frequencies for both video and memory clocks. Data lines D2 and D3 are commonly used as inputs to VSEL0 and VSEL1 for video frequency selection.

Inputs from VGA Controller

The VGA controller input to the **ICS90C65** is:

- SELEN

The **ICS90C65** is programmed to generate different video clock frequencies using the inputs of VSEL0, VSEL1, VSEL2, and VSEL3. The signals VSEL2 and VSEL3 may be supplied by the VGA controller as is the case in Western Digital Imaging VGA controllers. The inputs VSEL0-1 are latched with the signal SELEN. The SELEN input should be an active low pulse. This active low pulse is generated in Western Digital Imaging VGA controllers during I/O writes to internal register 3C2h.

Note: Only VSEL0 and VSEL1 are latched with signal SELEN.

Outputs to VGA Controller

The outputs from the **ICS90C65** to the VGA controller are:

- MCLK
- VCLK

MCLK and VCLK are the two clock outputs to the VGA controller.

Analog Filters

The analog filters are integral to the **ICS90C65** device. No external components are required. This feature reduces PC board space requirements and component costs. Phase-jitter is reduced as externally-generated noise cannot easily influence the phase-locked loop filter.

User-Definable Inputs

The user definable inputs are:

- EXTCLK
- VLCKE, MCLKE
- MSELO-2
- VSEL2, VSEL3
- $\overline{\text{PWRDN}}$

EXTCLK is an additional input that may be internally routed to the VCLK output. This additional input is useful for supporting modes that require frequencies not provided by the **ICS90C65** or for use during board test.

VCLKE and MCLKE are the output enable signals for VCLK and MCLK. When low the respective output is tristated.

MSEL0-2 are the memory clock (MCLK) select lines. Table 1-2 shows how MCLK frequencies are selected. All signals in this group have internal pull-up resistors.

VSEL2 and VSEL3 are video clock (VCLK) select lines that can select additional VCLK frequencies. See Table 1-1.

VSEL2 and VSEL3 have internal pull-ups.

$\overline{\text{PWRDN}}$ can place the **ICS90C65** in a power-down mode which drops its supply current requirement below 1 microamp. When placed in this mode, the digital inputs may be either high or low or floating without causing an increase in the **ICS90C65** supply current.

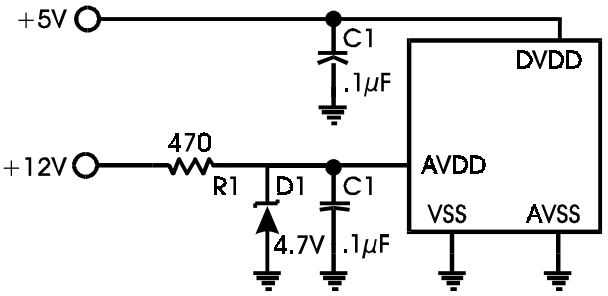
The $\overline{\text{PWRDN}}$ pin must be low (It has an internal pull-down.) in order to place the device in its low power state. The output pins (VCLK and MCLK) are driven high by the **ICS90C65** when it is in its low power state.

If CLKI is being driven by an external source, it may be driven low or high without a power penalty. If CLKI is at an intermediate voltage ($V_{SS}+0.5 < V_{IN} < V_{DD}-0.5$), there will be a small increase in supply current. If CLKI is driven at 14.318 MHz while the chip is in power-down, the **ICS90C65** supply current will increase to approximately 1.2 mA.

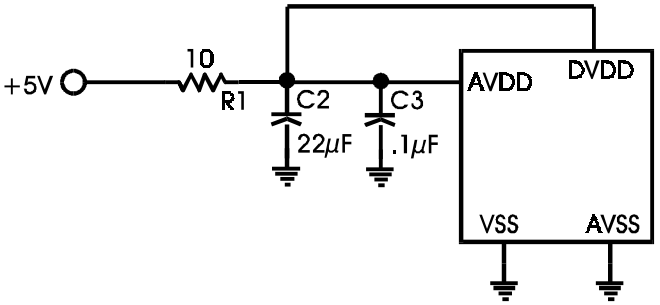
The SELEN (pin 6) may be used to guard against inadvertent frequency changes during power-down/powerup sequences. By holding the SELEN low during power-down and power-up sequences, the **ICS90C65** will retain the most recent video frequency selection.

Power Considerations

The **ICS90C65** product requires an AV_{DD} supply free of fast rise time transients. This requirement may be met in several ways and is highly dependent on the characteristics of the host system. A VGA adapter card is unique in that it must function in an unknown environment. +5 volt power quality is dependent not only on the quality of the power supply resident in the host system, but also on the other cards plugged into the host's backplane. Power supply noise ranges from fair to terrible. As the VGA adapter manufacturer has no control over this, he must assume the worst. The best solution is to create a clean +5 volts by deriving it from the +12 volt supply by using a zener diode and dropping resistor. A 470 Ohm resistor and 5.1 volt Zener diode are the least costly way to accomplish this. A .047 to .1 microfarad bypass capacitor tied from AV_{DD} to Av_{SS} insures good high- frequency decoupling of this point.



Laptop and notebook computers have entirely different problems with power. Typically they have no +12 volt supply; however, they are much quieter electrically. Because the designer has complete control of the system architecture, he can place sensitive components and systems such as the RAMDAC and Dual Video/Memory Clock away from DRAM and other noise-generating components. Most systems provide power that is clean enough to allow for jitter-free Dual Video/Memory Clock performance if the +5 volt supply is decoupled with a resistor and 22 microfarad Tantalum capacitor. Digital inputs that are desired to be held at a static logical high level should not be tied to +5 volts as this may result in excessive current drain through the ESD protection diode. The internal pull-up resistors will adequately keep these inputs high.



Pin Descriptions

The following table provides the pin descriptions for the 20-pin **ICS90C65** packages.

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
1	CLKI	IN	Reference input clock from system.
2	MSEL2	IN	Select input for MCLK selection.
3	EXTCLK	IN	External clock input for an additional frequency.
4	VSEL1	IN	Control input for VCLK selection.
5	VSEL0	IN	Control input for VCLK selection.
6	SELEN	IN	Strobe for latching VSEL(0,1) *(low enable)*.
7	VSEL2	IN	Control input for VCLK selection.
8	VSEL3	IN	Control input for VCLK selection.
9	MSEL0	IN	Select input for MCLK selection.
10	DVSS	-	Ground for Digital Circuit.
11	MSEL1	IN	Select input for MCLK selection.
12	MCLK	OUT	Memory Clock Output.
13	$\overline{\text{PWRDN}}$	IN	Power Down Control.
14	MCLKE	IN	Enable input for MCLK output *(high enables output)*.
15	AVDD	-	Power supply for analog circuit.
16	AVSS	-	Ground for analog circuit.
17	NC	-	No connection.
18	VCLKE	IN	Enable input for VCLK output *(high enables output)*.
19	VCLK	OUT	Video Clock Output.
20	DVDD	-	Power supply for Digital Circuit.

Note:
CLKI, EXTCLK,VSEL0, VSEL1,VSEL2, VSEL3, SELEN, MSEL0, MSEL1, MSEL2, VCLKE, and MCLKE - input pins have internal pull-up resistors. $\overline{\text{PWRDN}}$ has an internal pull-down resistor.

Absolute Maximum Ratings

Ambient Temperature under bias	0°C to 70°C
Storage temperature	-40°C to 125°C
Voltage on all inputs and outputs with respect to V_{SS}	0.3 to 7 volts

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (OV Ground). Positive current flows into the referenced pin.

Operating Temperature range	0°C to 70°C
Power supply voltage	3.0 to 5.25 volts

AC Timing Characteristics

The following notes apply to all of the parameters presented in this section:

1. REFCLK = 14.318 MHz
2. $T_C = 1/F_C$
3. All units are in nanoseconds (ns).
4. Maximum jitter is within a range of 30 µs after triggering on a 400 MHz scope.
5. Rise and fall time is between 0.8 and 2.0 VDC unless otherwise stated.
6. Output pin loading = 15pF
7. Duty cycle is measured at $V_{DD}/2$ unless otherwise stated.

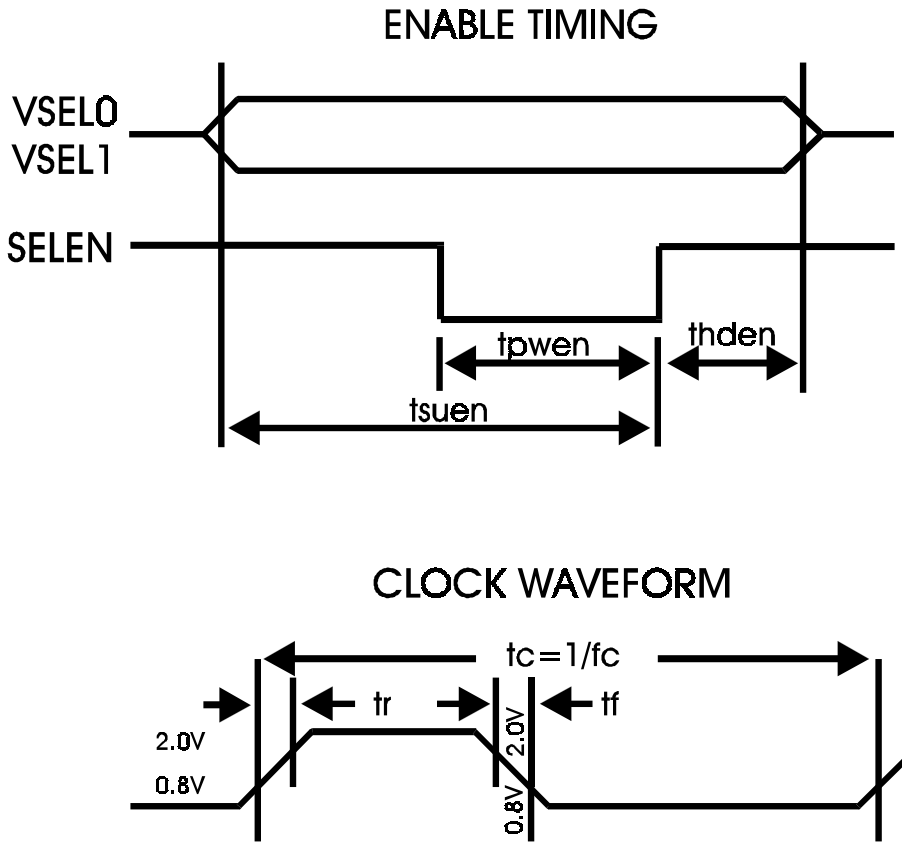
SYMBOL	PARAMETER	MIN	MAX	NOTES
	STROBE TIMING			
Tpw	Strobe Pulse Width	20	-	
Tsu	Setup Time Data to Strobe	20	-	
Thd	Hold Time Data to Strobe	10	-	
	MCLK and VCLK TIMINGS @ **5.0V**			
Tr	Rise Time	-	2	Duty Cycle 40% min. to
Tf	Fall Time	-	2	60% max.
-	Frequency Error		0.5	%
-	Maximum Frequency		135	MHz
-	Propagation Delay for Pass Through Frequency	-	20	ns
-	Output Enable to Tristate (into and out of) time		15	ns
	MCLK and VCLK TIMINGS @ **3.3V**			
Tr	Rise Time	-	3	Duty Cycle 40% min. to
Tf	Fall Time	-	3	60% max.
-	Frequency Error		.5	%
-	Maximum Frequency		110	MHz
-	Propagation Delay for Pass Through Frequency	-	30	ns
-	Output Enable to Tristate (into and out of) time		20	ns

DC Characteristics at 5 Volts VDD

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{DD}	Operating Voltage Range	4.75	5.25	V	
V_{IL}	Input Low Voltage	V_{SS}	0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0	V_{DD}	V	V_{DD} = 5V
I_{IH}	Input Leakage Current	-	10	µA	$V_{IN} = V_{CC}$
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = 8.0 mA
I_{DD}	Supply Current	-	30	mA	VDD = 5V
R_{UP}	Internal Pull-up Resistors	50	-	K ohms	V_{IN} = 0.0V
C_{in}	Input Pin Capacitance	-	8	pF	F_C = 1 MHz
C_{out}	Output Pin Capacitance	-	12	pF	F_C = 1 MHz
I_{PN}	Power-down Supply Current	-	1.0	µA	V_{DD}=3.3V
R_{DN}	Internal Pull-down Equivalent	20	-	K ohms	$V_{IN}=V_{DD}$=5V

DC Characteristics at 3.3 Volts V_{DD}

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{DD}	Operating Voltage Range	3.0	3.6	V	
V_{IL}	Input Low Voltage	V_{SS}	0.8	V	V_{DD} = 3.3V
V_{IH}	Input High Voltage	2.0	V_{DD}	V	V_{DD} = 3.3V
I_{IH}	Input Leakage Current	-	10	µA	$V_{in} = V_{DD}$
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 3.0 mA
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = 3.0 mA
I_{DD}	Supply Current	-	20	mA	V_{DD} = 3.3V
R_{UP}	Internal Pull-up Resistors	100	-	K ohms	V_{IN} = 0.0V
C_{in}	Input Pin Capacitance	-	8	pF	F_C = 1 MHz
C_{out}	Output Pin Capacitance	-	12	pF	F_C = 1 MHz
I_{PN}	Power-down Supply Current	-	1.0	µA	V_{DD} =3.3V
R_{DN}	Internal Pull-down Equivalent	50	-	K ohms	$V_{IN} = V_{DD}$ =3.3V



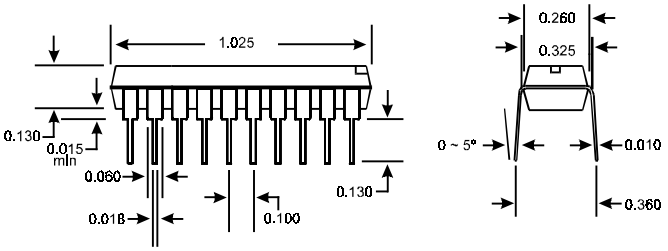
ICS90C65 Timing

Table 1-1 VCLK SELECTION

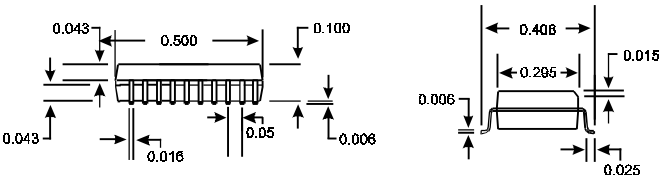
VSEL				
				VCLK FREQUENCY (MHz)
3	2	1	0	Pattern 951
0	0	0	0	30.0
0	0	0	1	77.25
0	0	1	0	EXTCLK
0	0	1	1	80.0
0	1	0	0	31.5
0	1	0	1	36.0
0	1	1	0	75.0
0	1	1	1	50.0
1	0	0	0	40.0
1	0	0	1	50.0
1	0	1	0	32.0
1	0	1	1	44.9
1	1	0	0	25.175
1	1	0	1	28.322
1	1	1	0	65.0
1	1	1	1	36.0

Table 1-2 MCLK SELECTION

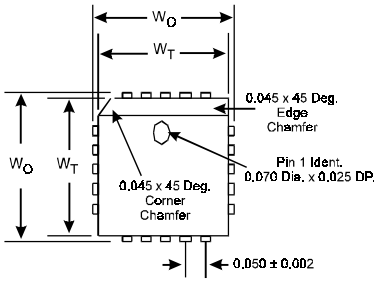
MSEL			
			MCLK FREQUENCIES (MHz)
2	1	0	Pattern 951
0	0	0	33.0
0	0	1	49.218
0	1	0	60.0
0	1	1	30.5
1	0	0	41.612
1	0	1	37.5
1	1	0	36.0
1	1	1	44.296

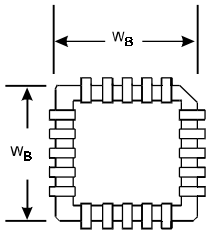


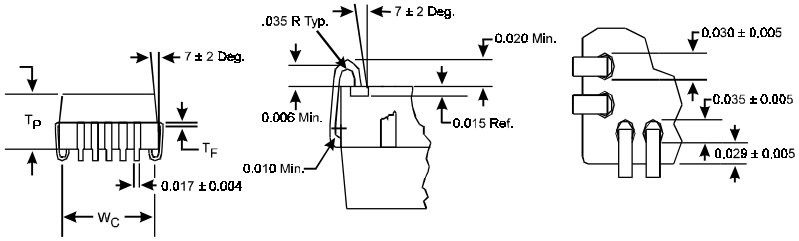
20-Pin DIP Package



20-Pin SOIC Package







PLCC Package

Ordering Information

ICS90C65N or ICS90C65M or ICS90C65V

Example:

ICS XXXX- XXX N

Package Type
N=DIP (Plastic) V=PLCC
M=SOIC

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3-6 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device