Integrated Circuit Systems, Inc.

ICS90C64A

Dual Video/Memory Clock Generator

Introduction

The Integrated Circuit Systems **ICS90C64A** is a dual clock generator for VGA applications. It simultaneously generates two clocks. One clock is for the video memory, and the other is the video dot clock.

This data sheet supplies sales order information, a functional overview, signal pin details, a block diagram, AC/DC characteristics, timing diagrams, and package mechanical information.

Description

The Integrated Circuit Systems Video Graphics Array Clock Generator (**ICS90C64A**) is capable of producing different output frequencies under firmware control. The video output frequency is derived from a 14.318 MHz system clock available in IBM PC/XT/AT and Personal System/2 computers. It is designed to work with Western Digital Imaging Video Graphics Array and 8514/A devices to optimize video subsystem performance.

The video dot clock output may be one of fifteen internally-generated frequencies or one external input. The selection of the video dot clock frequency is done through four inputs.

- VSEL0
- VSEL1
- VSEL2
- VSEL3

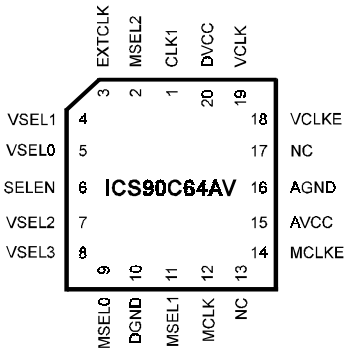
VSEL0 and VSEL1 are latched by the SELEN signal. VSEL2 and VSEL3 are used as direct inputs to the VCLK selection. Table 1-1 is the truth table for VCLK selection.

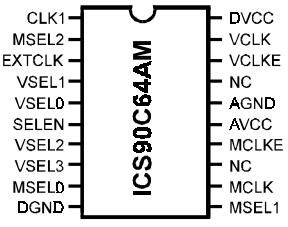
The input and truth table have been designed to allow a direct connection to one of the many Western Digital Imaging VGA controllers or 8514/A chip sets.

The MCLK output is one of eight internally-generated frequencies as shown in Table 1-2. The various VCLK and MCLK frequencies are derived from the 14.318 MHz Input frequency.

Features

- Improved compatibility with Western Digital Controllers
- 100% backward compatible with ICS90C63 and ICS90C64
- Dual Clock generator for the IBM compatible Western Digital Imaging Video Graphics Array (VGA) LSI devices, and 8514/A chip sets
- Integral loop filter components. Reduce cost and phase-jitter
- Generates 15 video clock frequencies (including 25.175 and 28.322 MHz) derived from a 14.318 MHz system clock reference frequency
- On-chip generation of eight memory clock frequencies.
- Video clock is selectable among the fifteen internally generated clocks and one external clock
- CMOS technology
- Available in 20-pin PLCC, SOIC, and DIP packages





Note: ICS90C64AN (DIP) pin-out is identical to ICS90C64AM (SOIC) pin-out.

ICS90C64A VGA Interface

The **ICS90C64A** has two system interfaces: System Bus and VGA Controller, as well as analog filters and seven user programmable inputs. Figure 2-1 shows how the Integrated Circuit Systems VGA Clock **ICS90C64A** is connected to a VGA controller. Western Digital Imaging VGA controllers normally have a status bit that indicates to the VGA controller that it is working with a clock chip. When working with a clock chip the VGA controller changes two of its clock inputs, VCLK1 and VCLK2, to outputs. These outputs are used to select the required video frequency.

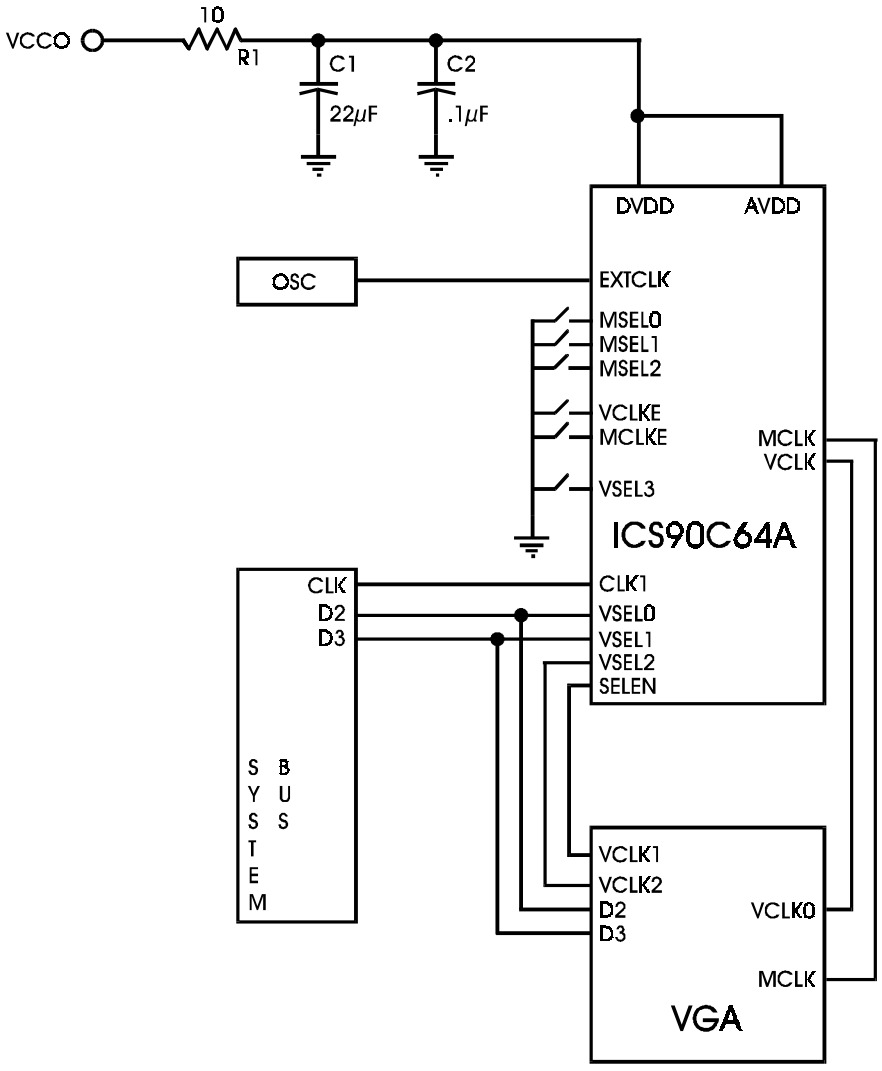


Figure 2-1 ICS90C64A Interface

Note:

C_2 should be placed as close as possible to the **ICS90C64A** AVDD pin.

System Bus Inputs

The system bus inputs are:

- CLK1
- VSEL0
- VSEL1

The **ICS90C64A** uses the system bus 14.318 MHz clock as a reference to generate all its frequencies for both video and memory clocks. Data lines D2 and D3 are commonly used as inputs to VSEL0 and VSEL1 for video frequency selection.

Inputs from VGA Controller

The VGA controller input to the **ICS90C64A** is:

- SELEN

The **ICS90C64A** is programmed to generate different video clock frequencies using the inputs of VSEL0, VSEL1, VSEL2, and VSEL3. The signals VSEL2 and VSEL3 may be supplied by the VGA controller as is the case in Western Digital Imaging VGA controllers. The inputs VSEL0-1 are latched with the signal SELEN. The SELEN input should be an active low pulse. This active low pulse is generated in Western Digital Imaging VGA controllers during I/O writes to internal register 3C2h.

Note: Only VSEL0 and VSEL1 are latched with signal SELEN.

Outputs to VGA Controller

The outputs from the **ICS90C64A** to the VGA controller are:

- MCLK
- VCLK

MCLK and VCLK are the two clock outputs to the VGA controller.

Analog Filters

The analog filters are integral to the **ICS90C64A** device. No external components are required. This feature reduces PC board space requirements and component costs. Phase-jitter is reduced as externally-generated noise cannot easily influence the phase-locked loop filter.

User-Definable Inputs

The user-definable inputs are:

- EXTCLK
- VLCKE, MCLKE
- MSELO-2
- VSEL2, VSEL3

EXTCLK is an additional input that may be internally routed to the VCLK output. This additional input is useful for supporting modes that require frequencies not provided by the **ICS90C64A**.

VCLKE and MCLKE are the output enable signals for VCLK and MCLK. When low, the respective output is tristated.

MSEL0-2 are the memory clock (MCLK) select lines. Table 1-2 shows how MCLK frequencies are selected. All signals in this group have internal pull-up resistors.

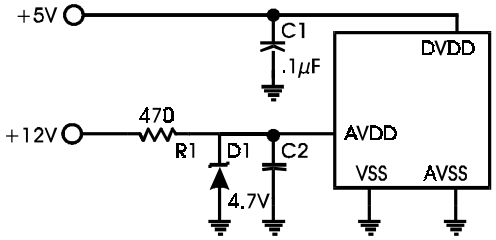
VSEL2 and VSEL3 are video clock (VCLK) select lines that can select additional VCLK frequencies. See Table 1-1.

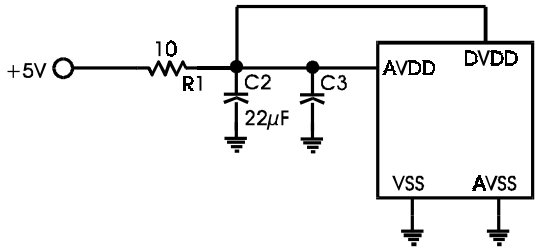
VSEL2 and VSEL3 have internal pull-ups.

Power Considerations

The **ICS90C64A** product requires an AV_{DD} supply free of fast rise time transients. This requirement may be met in several ways and is highly dependent on the characteristics of the host system. A VGA adapter card is unique in that it must function in an unknown environment. +5 volt power quality is dependent not only on the quality of the power supply resident in the host system, but also on the other cards plugged into the host's backplane. Power supply noise ranges from fair to terrible. As the VGA adapter manufacturer has no control over this, he must assume the worst. The best solution is to create a clean +5 volts by deriving it from the +12 volt supply by using a zener diode and dropping resistor. A 470 Ohm resistor and 5.1 volt Zener diode are the least costly way to accomplish this. A .047 to .1 microfarad bypass capacitor tied from AV_{DD} to AVss insures good high-frequency decoupling of this point.

Laptop and notebook computers have entirely different problems with power. Typically they have no +12 volt supply; however, they are much quieter electrically. Because the designer has complete control of the system architecture, he can place sensitive components and systems such as the RAMDAC and Dual Video/Memory Clock away from DRAM and other noise-generating components. Most systems provide power that is clean enough to allow for jitter- free Dual Video/Memory Clock performance if the +5 volt supply is decoupled with a resistor and 22 microfarad Tantalum capacitor. Digital inputs that are desired to be held at a static logical high level should not be tied to +5 volts as this will result in excessive current drain through the ESD protection diode. The internal pull-up resistors will adequately keep these inputs high.





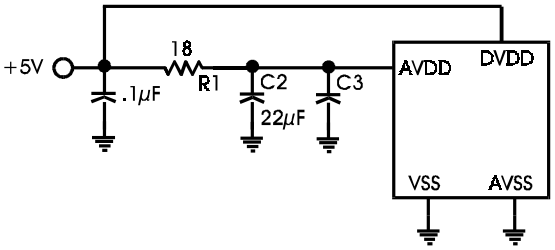


Table 1-1 VCLK Selection

3	2	1	0	VCLK Frequency (MHz)			
				ICS90C64A	ICS90C64A-903	ICS90C64A-907	ICS90C64A-909
0	0	0	0	30.0	30.0	30.250	30.0
0	0	0	1	77.25	77.25	77.25	77.25
0	0	1	0	EXTCLK	EXTCLK	EXTCLK	EXTCLK
0	0	1	1	80.0	80.0	80.0	80.0
0	1	0	0	31.5	31.5	31.5	31.5
0	1	0	1	36.0	36.0	35.5	36.0
0	1	1	0	75.0	75.0	75.0	75.0
0	1	1	1	50.0	50.0	72.0	50.0
1	0	0	0	40.0	40.0	40.0	40.0
1	0	0	1	50.0	50.0	50.0	50.0
1	0	1	0	32.0	32.0	32.0	32.0
1	0	1	1	44.9	44.9	44.9	44.9
1	1	0	0	25.175	25.175	25.175	25.175
1	1	0	1	28.322	28.322	28.322	28.322
1	1	1	0	65.0	65.0	65.0	65.0
1	1	1	1	36.0	36.0	36.0	36.0

Table 1-2 MCLK Selection

2	1	0	MCLK Frequencies (MHz)			
			ICS90C64A	ICS90C64A-903	ICS90C64A-907	ICS90C64A-909
0	0	0	33.0	33.0	65.0	75.0
0	0	1	49.218	49.218	49.218	40.0
0	1	0	60.0	60.0	60.0	45.0
0	1	1	30.5	30.5	62.5	50.0
1	0	0	41.612	41.612	41.612	55.0
1	0	1	37.5	37.5	37.5	60.0
1	1	0	36.0	36.0	55.0	65.0
1	1	1	44.296	44.296	44.296	70.0

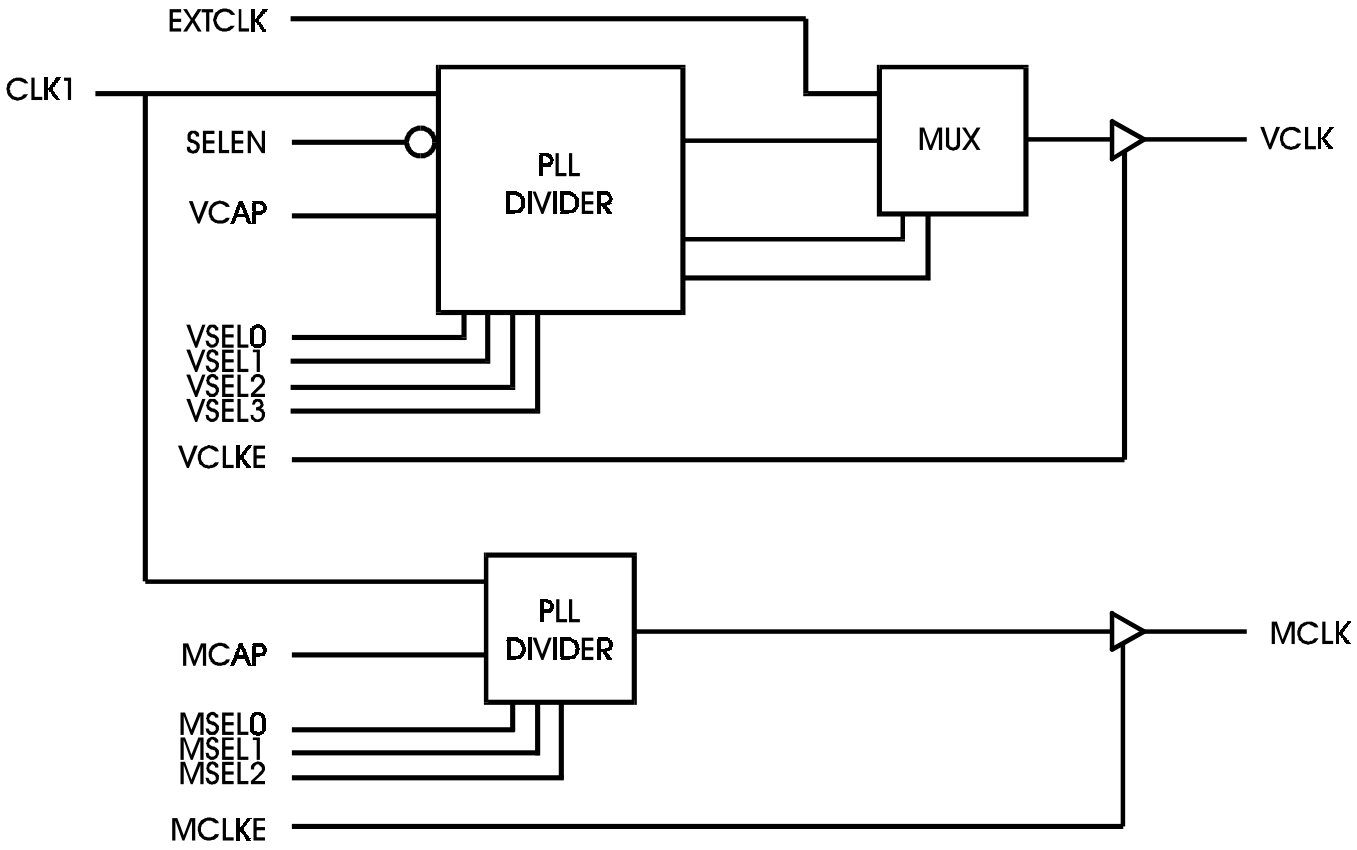


Figure 2-2 ICS90C64A Functional Block Diagram

Pin Descriptions

The following table provides the pin descriptions for the 20-pin **ICS90C64A** packages.

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
1	CLK1	IN	Reference input clock from system.
2	MSEL2	IN	Select input for MCLK selection.
3	EXTCLK	IN	External clock input for an additional frequency.
4	VSEL1	IN	Control input for VCLK selection.
5	VSEL0	IN	Control input for VCLK selection.
6	SELEN	IN	Strobe for latching VSEL(0,1) *(low enable)*.
7	VSEL2	IN	Control input for VCLK selection.
8	VSEL3	IN	Control input for VCLK selection.
9	MSEL0	IN	Select input for MCLK selection.
10	DGND	-	Ground for Digital Circuit.
11	MSEL1	IN	Select input for MCLK selection.
12	MCLK	OUT	Memory Clock Output.
13	NC	-	No connection.
14	MCLKE	IN	Enable input for MCLK output *(high enables output)*.
15	AVDD	-	Power supply for analog circuit.
16	AGND	-	Ground for analog circuit.
17	NC	-	No connection.
18	VCLKE	IN	Enable input for VCLK output *(high enables output)*.
19	VCLK	OUT	Video Clock Output.
20	DVDD	-	Power supply for Digital Circuit.

Note:
CLK1, EXTCLK,VSEL0, VSEL1,VSEL2, VSEL3, SELEN, MSEL0, MSEL1, MSEL2, VCLKE, and MCLKE - input pins have internal pull-up resistors.

Absolute Maximum Ratings

Ambient Temperature under bias	0°C to 70°C
Storage temperature	-40°C to 125 °C
Voltage on all inputs and outputs with respect to V_{SS}	0.5 to 7 volts

Note: Stresses above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (OV Ground). Positive current flows into the referenced pin.

Operating Temperature range	0°C to 70°C
Power supply voltage	4.75 to 5.25 volts

DC Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IL}	Input Low Voltage	V_{SS}		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{DD}	V	
I_{IH}	Input Leakage Current	-		10	µ A	$V_{in} = V_{DD}$
V_{OL}	Output Low Voltage	-		0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output High Voltage	V_{DD}-.4		-		I_{OH} = 4.0mA
V_{OH}	Output High Voltage	2.4		-	V	I_{OH} = 8.0 mA
I_{CC}	Supply Current	-	20	28	mA	No load VCLK = 28 MHz MCLK = 40 MHz
I_{CC}	Supply Current	-	27	35	mA	No load VCLK = 80 MHz MCLK = 40 MHz
R_{UP}	Internal Pull-up Resistors	50		-	K ohms	$V_{DD = 5V}$
C_{in}	Input Pin Capacitance	-		8	pF	F_C = 1 MHz
C_{out}	Output Pin Capacitance	-		12	pF	F_C = 1 MHz

AC Timing Characteristics

The following notes apply to all of the parameters presented in this section:

1. REFCLK = 14.318 MHz
2. $T_C = 1/F_C$
3. All units are in nanoseconds (ns), unless labeled otherwise.
4. Output pin loading = 15pF

SYMBOL	PARAMETER	MIN	TYP	MAX	NOTES
	SELEN TIMING				
T_{pwen}	Enable Pulse Width	20			
T_{suen}	Setup Time Data to Enable	20			
T_{hden}	Hold Time Data to Enable	10			
	Reference Input Clock				
Tr	Rise Time			10	Phase-Jitter 1 ns max.
Tf	Fall Time			10	Duty Cycle 42.5% min. to 57.5% max.
	MCLK and VCLK TIMINGS				
Tr	Rise Time		.9	1.5	.8V-2.0V*
Tf	Fall Time		.9	1.5	2.0V-.8V
Tr	Rise Time		1.2	2.0	.3 V_{DD}-.7 V_{DD}
Tf	Fall Time		1.2	2.0	.7 V_{DD}-.3 V_{DD}
T_{high}	Duty Cycle	50%		60%	1.4V Switch Point
T_{high}	Duty Cycle	45%		55%	V_{DD}/2 Switch Point
	Frequency Error			0.5	%
	Maximum Frequency			135	MHz
	Propagation Delay for Pass Through Frequency			20	ns
	Output Enable to Tri-State (into and out of) time			15	ns

*WD90C11 Video Controller is designed with TTL level input thresholds on the inputs driven by the ICS90C64A VCLK and MCLK outputs.
The later controllers (WD90C20, WD90C22, WD90C26, WD90C30, and WD90C31) are designed with input switch points of VCC/2 (CMOS).

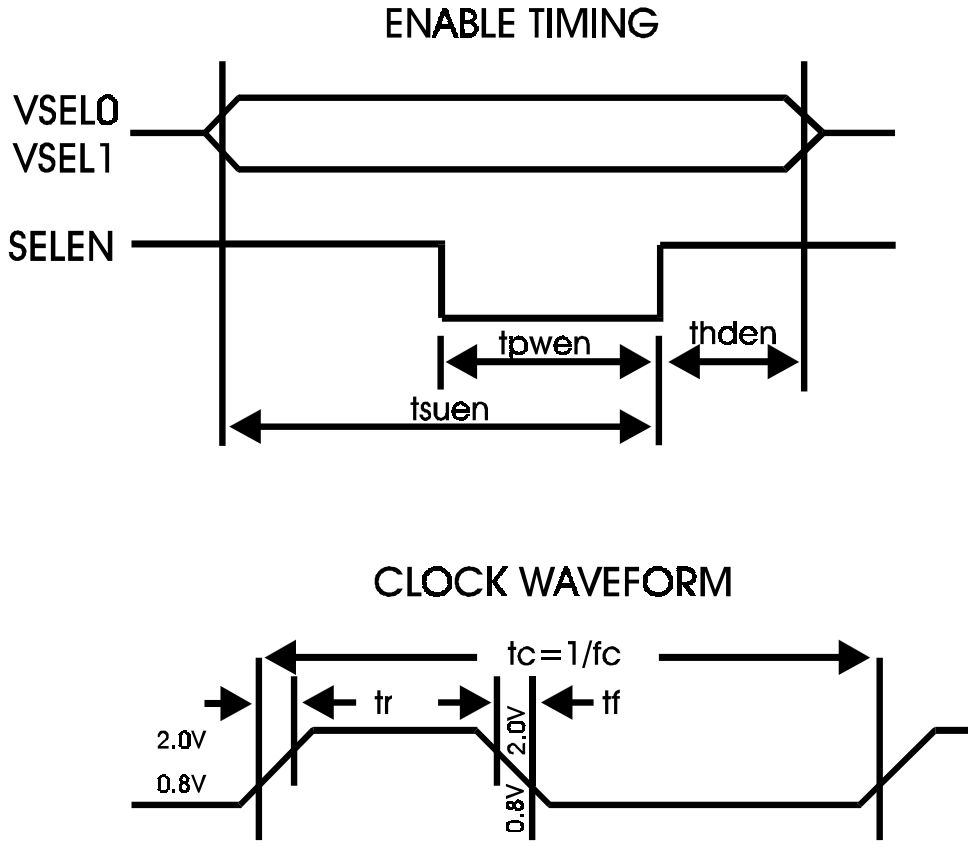
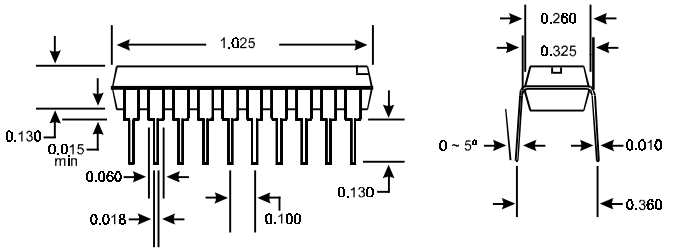
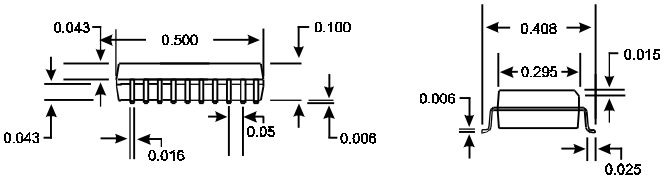


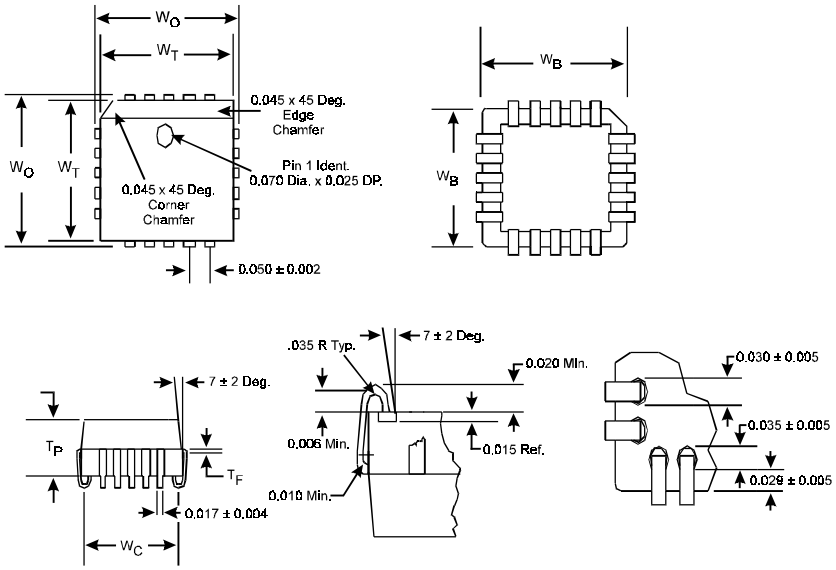
Figure 5-1 ICS90C64A Timing



20-Pin DIP Package



20-Pin SOIC Package



PLCC Package

Note:
All Package Dimensions in inches.

Ordering Information

ICS90C64AN or ICS90C64AM or ICS90C64AV

Example:

ICS XXXX- XXX N

- Package Type
  - N=DIP (Plastic) V=PLCC
  - M=SOIC
- Pattern Number (2 or 3 digit number for parts with ROM code patterns)
- Device Type (consists of 3-6 digit numbers)
- Prefix
  - ICS, AV=Standard Device; GSP=Genlock Device