Auto-Negotiation Advertisement Register (register 4 [0x04])

Bit	Definition	When bit=0	When bit=1	Access	Default	Hex
15	Next Page	always 0 - not capable of sending next pages		RO	0	0
14	Reserved by IEEE	always 0		RO	0	
13	Fault Indication to link partner	no fault	a fault has occurred locally	RW	0	
12	Technology Ability Field bit A7	reserved by IEEE		CW	0	
11	Technology Ability Field bit A6	reserved by IEEE		CW	0	1
10	Technology Ability Field bit A5	reserved by IEEE		CW	0	
9	TAF bit A4: 100Base-T4 Capability	always 0 - 100Base-T4 not supported		RO	0	
8	TAF A3: 100Base-TX Full Duplex Capability	100Base-TX FD not desired	100Base-TX FD supported	RW	1	
7	TAF A2: 100Base-TX Half Duplex Capability	100Base-TX HD not desired	100Base-TX HD supported	RW	1	E
6	TAF A1: 10Base-T Full Duplex Capability	10Base-T FD not desired	10Base-T FD supported	RW	1	
5	TAF A0: 10Base-T Half Duplex Capability	10Base-T HD not supported	10Base-T HD supported	RW	1	
4	Selector Field bit S4	IEEE 802.3 default		CW	0	
3	Selector Field bit S3	IEEE 802.3 default		CW	0	1
2	Selector Field bit S2	IEEE 802.3 default		CW	0	
1	Selector Field bit S1	IEEE 802.3 default		CW	0	
0	Selector Field bit S0	IEEE 802.3 default		CW	1	

Auto-Negotiation Advertisement Register (register 4)

The Auto-Negotiation advertisement register is a 16-bit read/write register used to indicate the basic capabilities of the local device. The values written into this register are exchanged with the remote link partner to determine the best link technology to enable. Normally it is desirable to advertise all of the capabilities supported by a node. In some cases a certain technology is not desired and in this case the corresponding bit can be set to logic zero. If a connection cannot be made in this case, management should enable all of the capabilities possessed and restart Auto-Negotiation.

Next Page (bit 15)

The **ICS1890** does not support the next page function. This bit is permanently set to a logic zero.

Reserved by IEEE (bit 14)

This reserved bit has no effect on the **ICS1890**. When read, a logic zero is always returned.

Remote Fault (bit 13) Management may set this bit to a logic one, which sets the remote fault bit in the transmitted base link code word to a logic one. This indicates to the link partner that an error has been detected at this end.
The Auto-Negotiation Power-up Remote Fault option (19:4) can also cause the remote fault bit in the transmitted base link code word to be set to a logic one.

Technology Ability Field (bits 12:5) This 8-bit field specifies the data transmission technologies supported by the **ICS1890**. On power-up when the HW/SW pin is set to SW, these bits are set to the values specified in the MII Status register. When the HW/SW pin is set to HW and ANSEL is enabled, the single bit corresponding to the values of the DPXSEL and 10/100SEL pins is enabled. All bits, except the 100Base-T4 (unsupported technology bit) may be set or cleared allowing management to select the advertised technologies.
Note that bits 12-10 are currently reserved by the IEEE Auto-Negotiation standard and should always be set to logic zero.

Selector Field (bits 4:0) This 5-bit field is used to select the technology supported by the **ICS1890**. It defaults to select IEEE 802.3 (00001). These bits can only be written using the command override mode and should only be set to a different value as allowed by the IEEE standard

Auto-Negotiation Link Partner Ability Register (register 5 [0x05])

Bit	Definition	When bit=0	When bit=1	Access	Default	Hex
15	Next Page	partner does not support next page exchange	partner supports next page exchange	RO	0	0
14	Reserved by IEEE	always 0		RO	0	
13	Remote Fault	no fault	a fault has occurred at the remote link partner	RO	0	
12	Technology Ability Field bit A7	reserved by IEEE		RO	0	
11	Technology Ability Field bit A6	reserved by IEEE		RO	0	0
10	Technology Ability Field bit A5	reserved by IEEE		RO	0	
9	TAF bit A4: 100Base-T4 Capability	partner does not support 100Base-T4	partner supports 100Base-T4	RO	0	
8	TAF A3: 100Base-TX Full Duplex Capability	partner does not support 100Base- TX Full Duplex	partner supports 100Base- TX Full Duplex	RO	0	
7	TAF A2: 100Base-TX Half Duplex Capability	partner does not support 100Base- TX Half Duplex	partner supports 100Base- TX Half Duplex	RO	0	0
6	TAF A1: 10Base-T Full Duplex Capability	partner does not support 10Base-T Full Duplex	partner supports 10Base-T Full Duplex	RO	0	
5	TAF A0: 10Base-T Half Duplex Capability	partner does not support 10Base-T Half Duplex	partner supports 10Base-T Half Duplex	RO	0	
4	Selector Field bit S4	see decode table		RO	0	
3	Selector Field bit S3	see decode table	802.3 = 00001	RO	0	0
2	Selector Field bit S2	see decode table	802.9 = 00010	RO	0	
1	Selector Field bit S1	see decode table		RO	0	
0	Selector Field bit S0	see decode table		RO	0	

Auto-Negotiation Link Partner Ability Register (register 5)

The Auto-Negotiation link partner ability register is a 16-bit read-only register used to indicate the abilities of the link partner. When compared to local abilities in register 4 and sorted by the standard IEEE priority table the highest possible performance link can be determined. Note that the values in this register are only valid when Auto-Negotiation is complete as indicated by (1:5) or the equivalent bit in the QuickPoll register.

Next Page (bit 15)

If set to a logic one, this bit indicates that the link partner can operate in the next page mode. Since the **ICS1890** does not support the next page function, no action or response results from this indication.

Reserved (bit 14)

This reserved bit will always be returned as a logic zero.

Remote Fault (bit 13)

When the remote fault bit of the Link Code Word is set to a logic one, the **ICS1890** sets the remote fault bit in the Link Partner Ability Register to a logic one. This indicates that the link partner has detected an error.

Technology Field (bits 12:5)

This 8-bit field specifies the data transmission technologies supported by the remote partner. The contents are valid on successful completion of Auto-Negotiation as indicated by a logic one in bit 5 of the **ICS1890** status register.

Selector Field (bits 4:0)

This 5-bit field indicates the technology supported by the link partner. A valid IEEE 802.3 link partner will always signal (00001). A code of (00010) indicates an IEEE 802.9a partner. All other codes are currently undefined.

Auto-Negotiation Expansion Register (register 6 [0x06])

Bit	Definition	When bit=0	When bit=1	Access	Default	Hex
15	Reserved by IEEE	always 0		CW	0	0
14	Reserved by IEEE	always 0		CW	0	
13	Reserved by IEEE	always 0		CW	0	
12	Reserved by IEEE	always 0		CW	0	
11	Reserved by IEEE	always 0		CW	0	0
10	Reserved by IEEE	always 0		CW	0	
9	Reserved by IEEE	always 0		CW	0	
8	Reserved by IEEE	always 0		CW	0	
7	Reserved by IEEE	always 0		CW	0	0
6	Reserved by IEEE	always 0		CW	0	
5	Reserved by IEEE	always 0		CW	0	
4	Parallel Detection Fault	no fault	more than one technology appeared valid	RO /LH	0	
3	Link Partner Next Page Able	link partner is not Next Page Able	link partner is Next Page Able	RO	0	0
2	Next Page Able	always 0 - next page not supported		RO	0	
1	Page Received	new link code word not received	new link code word received	RO /LH	0	
0	Link Partner is Auto-Negotiation Able	link partner not able	link partner support Auto-Negotiation	RO	0	

Auto-Negotiation Expansion Register (register 6)

The Auto-Negotiation expansion register is a 16-bit read-only register used to indicate the status of the auto-negotiation process. It is accessed via the management interface of the MII.

Reserved (bits 15:5)

These bits are reserved. The contents are permanently set to logic zeros.

Parallel Detection Fault (bit 4)

If set to a logic one, this bit indicates that a parallel detection fault has been detected. This means that more than one of the allowed technologies has detected a valid link.

Link Partner Next Page Able (bit 3)

If set to a logic one, this bit indicates that the link partner is capable of operating in the next page mode.

Next Page Able (bit 2)

This bit is permanently set to a logic zero indicating that the **ICS1890** is not able to operate in the next page mode.

Page Received (bit 1)

If set to a logic one, this bit indicates that three identical and consecutive link code words have been received from the link partner.

Link Partner Auto-Negotiation Able (bit 0)

If set to a logic one, this bit indicates that the link partner is able to participate in the auto-negotiation process. If set to a logic zero, it is not able to participate in the auto-negotiation process.

Extended Control Register (register 16 [0x10])

Bit	Definition	When bit=0	When bit=1	Access	Default	Hex
15	Command Register Override	don't allow writes to CW bits	allow next write to effect both RW & CW bits	RW /SC	0	
14	Reserved for ICS	Read unspecified		RW /0	-	
13	Reserved for ICS	Read unspecified		RW /0	-	
12	Reserved for ICS	Read unspecified		RW /0	-	
11	Reserved for ICS	Read unspecified		RW /0	-	
10	PHY address bit 4	A		RO	P4RD	
9	PHY address bit 3	MII Management's		RO	P3TD	
8	PHY address bit 2	Register Address code		RO	P2LI	
7	PHY address bit 1	0 - 31 Read Only		RO	P1CL	
6	PHY address bit 0	Read unspecified		RO	P0AC	
5	Stream Cipher Scrambler Test Mode	normal	test mode	RW	0	
4	Reserved for ICS	Read unspecified		RW /0	-	
3	NRZ/NRZ1 Encoding	NRZ	NRZ1	RW	1	
2	Invalid Error Code Test	disabled	enabled	RW	0	
1	Reserved for ICS	Read unspecified		RW /0	-	
0	Stream Cipher Disable	enabled	disabled	RW	0	

Extended Control Register (register 16)

The Control Register is a 16-bit read/write register used to pre-program the **ICS1890**. At power-up and reset, this register will be loaded to the default values specified in the table above.

Command Register Override (bit 15)

If set to a logic one, this bit allows a subsequent write to any Command Writeable bit (CW) in any register. A write to any register after this bit is set will reset the bit, preventing subsequent writes to Command Write able bits from having any effect. Therefore, each write to a Command Writeable bit must be preceded by writing a logic one to this bit.

Bits Reserved for ICS use (14-11)

These bits are reserved for ICS use. These bits should only be written as logic zero. Writing a logic one to these bits may prevent the device from operating correctly. The value of these bits is unspecified and may be a logic zero or one.

PHY Address (Bits 10 through 6)

These five bits are used to indicate the address of the **ICS1890** on the management port of the MII (any number in the range 0 - 31). The connection of the LEDs to the LED pins sets the address. A read returns the address. A write is ignored.

Stream Cipher Scrambler Test Mode (Bit 5)

If set to a logic one, the scrambler will resynchronize after 252 bits of non-idle data instead of its normal time.

Bits Reserved for ICS use (Bit 4)

These bits are reserved for ICS use. These bits should only be written as logic zero. Writing a logic one to these bits may prevent the device from operating correctly. The value of these bits is unspecified and may be a logic zero or one.

NRZ/NRZ1 Encoding (bit 3)

When this bit is 1 normal NRZ1 encoding of data is performed for 100Base-TX. When this bit is 0 NRZ coding is used instead. NRZ encoding can be useful for system debug.

Invalid Error Code Test (bit 2)

If this bit is set to a logic one, the 4B5B encoder allows non-data symbols to be sent when TXER is asserted. See the Invalid Error Code Test table for the symbol mapping.

Reserved for ICS use (bit 1)

These bits are reserved for ICS use. These bits should only be written as logic zero. Writing a logic one to these bits may prevent the device from operating correctly. The value of these bits in unspecified and may be a logic zero or one.

Stream Cipher Disable (bit 0)

If this bit is set to a logic one, the stream cipher encoder and decoder are disabled. This will result in unscrambled IDLES and data streams being transmitted and received for ease of debug

QuickPoll Detailed Status Register (register 17 [0x11])

Bit	Definition	When bit=0	When bit=1	Access	Default	Hex
15	Data Rate	10 Mb/s negotiated	100 Mb/s negotiated	RO	*	
14	Duplex	half duplex negotiated	full duplex negotiated	RO	*	
13	Auto-Negotiation Progress Monitor bit 2	see decode table		RO /LL /LH	0	
12	Auto-Negotiation Progress Monitor bit 1	see decode table		RO /LL /LH	0	
11	Auto-Negotiation Progress Monitor bit 0	see decode table		RO /LL /LH	0	
10	Receive Signal Error	signal	loss of signal	RO /LH	0	
9	PLL Lock Error	PLL locked	PLL failed to lock	RO /LH	0	
8	False Carrier Detect	normal carrier or idle	false carrier detected	RO /LH	0	
7	Invalid Symbol	valid symbols	invalid symbol detected	RO /LH	0	
6	Halt Symbol	normal symbols	HALT symbol detected	RO /LH	0	
5	Premature End	normal stream	stream with two IDLE symbols	RO /LH	0	
4	Auto-Negotiation complete	Auto-Negotiation progress	Auto-Negotiation complete	RO	0	
3	Signal Detect 100Base-TX	SD active	SD inactive	RO	-	
2	Jabber Detect	no jabber detected	jabber detected	RO /LH	0	
1	Remote Fault	no remote fault detected	remote fault detected	RO /LH	0	
0	Link Status	link is not valid	link is valid	RO /LL	0	

QuickPoll Detailed Status (register 17)

The **ICS1890** detailed status register is a 16-bit read-only register used to indicate detailed status of the **ICS1890**. It is accessed via the management interface of the MII. It is initialized during a power-up or reset to pre-defined default values. A number of bits are duplicated in this register from others to make them more easily accessable when polling the device for status. This should be the only register that needs to be repeatedly polled in an application.

Data Rate (bit 15)

If set to a logic one, this bit indicates that has been selected 100 Mbps mode. If set to a logic zero, it indicates that the initial-10 Mbps mode has been selected. This bit's setting depends on the setting of the HW/SW pin, 10/100SEL pin, ANSEL pin, and the setting of bits 0:12, 0:13, and 1:5.

Duplex (bit 14)
If set to a logic one, this bit indicates that has been selected full duplex mode. If set to a logic zero, it indicates that the half duplex mode has been selected. This bit's setting depends on the setting of the HW/SW pin, DPXSEL pin, ANSEL pin, and the setting of bits 0:12, 0:8, and 1:5.

Auto-Negotiation Progress (bit 13 - 11)
These three bits are encoded to indicate the progress of the auto-negotiation cycle. These bits are initialized to zero. The values indicate the progress of auto-negotiation. See the Auto-Negotiation Progress Monitor section for the encodings and additional details.

Receive Signal Error (bit 10)
If set to a logic one, the receive channel signal (bit 15) indicates that the **ICS1890** read channel has, at some point, been unable to detect the receive channel signal (either the IDLE stream in 100Base-TX mode or link pulses in 10Base-T mode). This bit will remain set until cleared by reading the contents of register 17.

PLL Lock Error (bit 9)
If set to a logic one, the loss of PLL lock indicates that the **ICS1890** read channel PLL has failed to lock onto the read channel signal. This bit will remain set until cleared by reading the contents of register 17.

False Carrier (bit 8)
If set to a logic one, the false carrier indicates that the **ICS1890** has detected a false carrier sometime since this bit was last reset. This bit will remain set until cleared by reading the contents of register 17.

Invalid Symbol (bit 7)
If set to a logic one, the invalid symbol indicates that an invalid symbol has been detected in a received frame since the bit was last reset. This bit will remain set until cleared by reading the contents of register 17.

Halt Symbol (bit 6)
If set to a logic one, the halt symbol (bit 10) indicates that the **ICS1890** has detected the halt symbol in a frame since bit 11 was last reset. This bit will remain set until cleared by reading the contents of register 17.

Premature End (bit 5)
This bit is normally a logic zero indicating normal data streams. If two IDLE symbols are detected during the reception of a receive data stream, this bit is set to a logic one and the **ICS1890** returns to the idle state. This bit is initialized to a logic zero.

Auto-Negotiation Complete (bit 5)
When set to a logic one, this bit indicates that the **ICS1890** has completed the auto-negotiation process and that the contents of registers 4, 5 and 6 are valid. When set to a logic zero, this bit indicates that auto-negotiation is not complete or that auto-negotiation has been disabled in the command register (bit 12).

100Base_TX Signal Detect (bit 3)
The absence of 100Base_TX signaling on the TP_RX± pins will cause this bit to be asserted (1)

Jabber Detect (bit 2)
When operating in the 10Base-T mode, if set to a logic one, this bit indicates that a jabber condition occurred and that the transmit pair has been isolated.

Remote Fault (bit 1) This is a copy of the Remote Fault bit of the Status Register (register 1).

Link Status (bit 0) This is a copy of the Link Status bit of the Status Register (register 1).

10Base-T Operations Register (register 18 [0x12])

Bit	Definition	When bit=0	When bit=1	Access	Default	Hex
15	Reserved for ICS	Read unspecified	must be wirtten as a 0	RW /0	0	
14	Polarity Reversed	polarity normal	polarity reserved	RO /LH	0	
13	Reserved for ICS	Read unspecified		RW /0	-	
12	Reserved for ICS	Read unspecified		RW /0	-	
11	Reserved for ICS	Read unspecified		RW /0	-	
10	Reserved for ICS	Read unspecified		RW /0	-	
9	Reserved for ICS	Read unspecified		RW /0	-	
8	Reserved for ICS	Read unspecified		RW /0	-	
7	Reserved for ICS	Read unspecified		RW /0	-	
6	Reserved for ICS	Read unspecified		RW /0	-	
5	Jabber Inhibit	normal jabber behavior	no jabber check	RW	0	
4	Reserved for ICS	Read unspecified	must be written as a 1	RW /1	1	
3	Auto Polarity Inhibit	polarity automatically corrected	polarity not corrected	RW	0	0
2	SQE Test Inhibit	normal SQE test behavior	no SQE test	RW	0	
1	Link Loss Inhibit	normal Link Loss behavior	link always = Link Pass	RW	0	
0	Squelch Inhibit	normal Squelch	no Squelch	RW	0	

10Base-T Operations Register (register 18)

This register contains all of the extra status and control bits required for 10Base-T operation.

Bits Reserved for ICS use (15, 13, 6)

These bits are reserved for ICS use. These bits should only be written as logic zero. Writing a logic one to these bits may prevent the device from operating correctly. The value of these bits is unspecified and may be a logic zero or one.

Polarity Reversed (bit 14)

This bit is set to a logic one if the polarity of the receive data pair is reversed. This bit will be a logic zero if the polarity is correct.

Jabber Inhibit (bit 5)

Setting this bit to a logic one turns off the internal check for transmit jabber. When the jabber check is disabled, no action occurs when transmissions are longer than the jabber timer value. When this bit is set to a logic zero normal 10Base-T jabber checking is enabled.

Bit Reserved for ICS use (bit 4)

This bit must be written to a 1. The read value of this bit is undefined.

Auto Polarity Inhibit (bit 3)

When this bit is set to a logic one, correction for reversed receive data wires is disabled. When this bit is set to a logic Zero, reversed receive data wires are automatically corrected for internally.

SQE Test Inhibit (bit 2)

When this bit is set to a logic one, SQE testing is disabled. When this bit is set to a logic zero, a normal 10Base-T SQE test is performed by pulsing the Collision signal for a short time shortly after each packet transmission completes.

Note that the SQE Test is automatically inhibited in Full Duplex and Repeater modes.

Link Loss Inhibit (bit 1)

When this bit is set to a logic one, the 10Base-T Link Integrity Test state machine is forced into the Link Pass state regardless of the line conditions. This can be useful in debugging a bad link segment. When this bit is set to a logic zero, the state machine behaves normally.

Squelch Inhibit (bit 0)

When this bit is set to a logic one, the receive squelch circuitry is disabled. This can be useful in debugging a bad link segment or for link segments longer than 100 meters. When this bit is set to a logic zero, the normal Squelch circuitry is enabled to filter out spurious line noise.

Extended Control Register 2 (register 19 [0X13])

Bit	Definition	When bit=0	When bit=1	Access	Default	Hex
15	Node/Repeater Mode	Node Mode	Repeater Mode	RO	NOD/-REP	
14	Hardware/Software Priority	Hardware Priority	Software Priority	RO	HW/S-W	
13	Link Partner Supports Remote Fault	unknown	partner supports Remote Fault	RO	0	
12	Reserved for ICS	Read unspecified		RW /0	-	
11	Reserved for ICS	Read unspecified		RW /0	-	
10	Transmitted Remote Fault Status	RF bit in transmitted LCW=0	RF bit in transmitted LCW=1	RW /0	-	
9	Reserved for ICS	Read unspecified		RW /0	-	
8	Reserved for ICS	Read unspecified		RW /0	-	
7	Reserved for ICS	Read unspecified		RW /0	-	
6	Reserved for ICS	Read unspecified		RW /0	-	
5	Reserved for ICS	Read unspecified		RW /0	-	
4	A-N Power-up Remote Fault	Normal	Remote Fault on Power-up	RW	0	
3	Reserved for ICS	Read unspecified		RW /0	0	
2	Reserved for ICS	Read unspecified		RW /0	-	
1	Reserved for ICS	Read unspecified		RW /0	0	
0	Automatic 100Base-TX Power-down	Never Power-down automatically	Power-down automatically	RW	1	

Extended Control Register 2 (register 19)

Node/Repeater Configuration (bit 15)

This bit directly reflects the status of the NOD/REP pin.

When this bit is logic zero, the device will default to Node operation. SQE test will default to on. Carrier sense in half duplex mode will be on transmit or receive activity.

When this bit is logic one, the device will default to Repeater operation. SQE test will default to off. Carrier sense in half duplex mode will be on receive activity only.

Hardware/Software Priority Status (bit 14)

This bit directly reflects the status of the HW/SW pin.
When this bit is logic zero, hardware pins have priority over software settings. The 10/100SEL pin becomes an input and controls speed selection. The DPXSEL pin becomes an input and controls duplex selection. The ANSEL pin becomes an input and chooses configuration with or without Auto-Negotiation.
When configuration through Auto-Negotiation is selected, the DPXSEL and 10/100SEL settings control the Auto-Negotiation register 4 default settings and Auto-Negotiation is enabled. When configuration without Auto-Negotiation is selected, DPXSEL controls the duplex setting and 10/100SEL controls the data rate setting.

When this bit is a logic one, software bits have priority over hardware pin settings. The 10/100SEL pin becomes an output indicating the link speed when LSTA the link is established and parallels bit (17:15). The DPXSEL pin becomes an output indicating the link duplex state when the link is established and parallels bit (17:14). The ANSEL pin becomes an output indicating whether auto-negotiation is being used and parallels bit (0:12).

Link Partner Remote Fault Capable (bit 13)
This bit tries to indicate if the link partner supports indication of a remote fault. If the **ICS1890** observes the link partner Auto-Negotiating with the Remote Fault bit set, this status bit will be set to a logic one. Otherwise, this bit will be a logic zero.

Note that a logic zero can not definitively mean that the link partner does not support remote fault indications.

Reserved (bits 12-11)
These bits are reserved for ICS use. They must only be written as logic zero. Writing a logic one to any of these bits may prevent the device from operating normally. The value of these bits when read is unspecified and may be a logic zero or one.

Transmitted Remote Fault Status (bit 10)
This bit reflects the current status of the Remote Fault bit in the Transmitted Link Code Word. This bit is set when bit 4:15 is set or when bit 19:4 is set and the link partner is not transmitting.

Reserved (bits 9-5)
These bits are reserved for ICS use. They must only be written as logic zero. Writing a logic one to any of these bits may prevent the device from operating normally. The value of these bits when read is unspecified and may be a logic zero or one.

Power-up Remote Fault (bit 4)
When this bit is set to a logic one, the RF bit in the outgoing Auto-Negotiation Link Code Word will automatically be set to a logic one until receive activity is detected (Normal Link Pulses, Fast Link Pulses, 100Base-TX data, ...).

Bits Reserved for ICS use (bits 3-1)
These bits are reserved for ICS use. These bits should only be written as logic zero. Writing a logic one to these bits may prevent the device from operating correctly. The value of these bits is unspecified and may be a logic zero or one.

Automatic 100Base-TX Power-down (bit 0)
When this bit is set to a logic one and 10Base-T is selected for the network connection, the 100Base-TX transceiver will automatically turn off to save power.

When this bit is set to a logic zero, the 100Base-TX transceiver will never power-down by itself. The 100Base-TX transceiver will still power-down when the entire device is isolated using bit (0:10).

Pin Descriptions

Signal	Meaning	Signal	Meaning
TXCLK*	Transmit Clock	NOD/REP	Node/Repeater Mode
TXEN*	Transmit Enable	MII/SI	MII Data/Stream Interface
TXD3*	Transmit Data 3	10/LP	10M Serial/Link Pulse Interface
TXD2*	Transmit Data 2	HW/SW	Hardware/Software Priority
TXD1*	Transmit Data 1	10/100SEL	10/100 Select
TXD0*	Transmit Data 0	DPXSEL	Duplex Select
TXER*	Transmit Error	ANSEL	Auto-Negotiation Select
		ITCLS~	Invert Transmit Clock Latching Setting
RXCLK*	Receive Clock	TPTRI	Twisted Pair Tristate
RXDV*	Receive Data Valid	RXTRI	Receive MAC-PHY Interface Tristate
RXD3	Receive Data 3	LSTA*	Link Status
RXD2*	Receive Data 2	LOCK	Cipher Lock
RXD1*	Receive Data 1	RESET~	System Reset
RXD0*	Receive Data 0		
RXER*	Receive Error		
CRS*	Carrier Sense		
COL*	Collision Detect		
		P4RD	PHY ID 4/Receive data LED
MDC	Management Data Clock	PSTD	PHY ID 3/Transmit data LED
MDIO	Management Data Input/Output	P2LI	PHY ID 2/Link Integrity LED
		P1CL	PHY ID 1/Collision det LED
REF_IN	Frequency reference	P0AC	PHY ID 0/Activity LED
REF_OUT	Frequency reference		
TP_TX+	Twisted Pair Transmit Data+		
TP_TX-	Twisted Pair Transmit Data-	NC	5 No Connect Pins
TP_RX+	Twisted Pair Receive Data+		
TP_RX-	Twisted Pair Receive Data-		
10TCSR	10M transmit Current Set Resistor	VDD	8 VDD Pins
100TCSR	100M Transmit Current Set Resistor	VSS	7 VSS Pins
*Re-defined for other MAC-PYY interfaces			

Pin Descriptions

MII Data Interface

The following pin descriptions apply in either 10 or 100 Mbps mode when the MII Data Interface is selected. These pins are re-used for the 100M Stream Interface, 10M Serial Interface, and the Link Pulse Interface. These extra pin meanings are described in separate interface sections with the “pseudo” pin name followed by the actual pin name that the function is mapped onto.

Transmit Clock TXCLK

The Transmit Clock (TXCLK) is a continuous clock signal generated by the **ICS1890** to synchronize information transfer on the Transmit Enable, Transmit Data and Transmit Error lines. The **ICS1890** clock frequency is 25% of the nominal transmit data rate. At 10 Mbps, its frequency is 2.5 MHz and at 100 Mbps is 25 MHz.

Transmit Enable TXEN

Transmit Enable (TXEN) indicates to the **ICS1890** that the MAC is sending valid data nibbles for transmission on the physical media. Synchronous with its assertion, the **ICS1890** will begin reading the data nibbles on the transmit data lines. It is the responsibility of the MAC to order the nibbles so that the preamble is sent first, followed by destination, source, length, data and CRC fields since the **ICS1890** has no knowledge of the frame structure and is merely a “nibble” processor. The **ICS1890** terminates transmission of nibbles following the de-assertion of Transmit Enable (TXEN).

Transmit Data 3 TXD3

Transmit Data 3 (TXD3) is the most significant bit of the transmit data nibble. TXD3 is sampled by the **ICS1890** synchronously with the Transmit Clock when TXEN is asserted. When TXEN is de-asserted, the **ICS1890** is unaffected by the state of TXD3.

Transmit Data 2 TXD2

Transmit Data 2 (TXD2) is sampled by the **ICS1890** synchronously with the Transmit Clock when TXEN is asserted. When TXEN is de-asserted, the **ICS1890** is unaffected by the state of TXD2.

Transmit Data 1 TXD1

Transmit Data 1 (TXD1) is sampled by the **ICS1890** synchronously with the Transmit Clock when TXEN is asserted. When TXEN is de-asserted, the **ICS1890** is unaffected by the state of TXD1.

Transmit Data 0 TXD0

Transmit Data 0 (TXD0) is the least significant bit of the transmit data nibble. TXD0 is sampled by the **ICS1890** synchronously with the Transmit Clock when TXEN is asserted. When TXEN is de-asserted, the **ICS1890** is unaffected by the state of TXD0.

Transmit Error TXER

When operating in the 100 Mbps mode, the assertion of Transmit Error (TXER) for one or more clock periods will cause the **ICS1890** to emit one or more invalid symbols. The signal must be synchronous with TXCLK. In the normal operating mode, a HALT symbol will be substituted for the next nibble decoded.

If the Invalid Error Code Test bit (16:2) is set, the 5-bit code group shown in the 4B5B encoding table will be substituted for the transmit data nibble presented.

The value of TXER during 10 Mbps operation has no effect on the **ICS1890**.

Receive Clock RXCLK

The Receive Clock (RXCLK) is sourced by the **ICS1890**. There are two possible sources for the Receive Clock (RXCLK). When a carrier is present on the receive pair, the source is the recovered clock from the data stream. When no carrier is present on the receive pair, the source is the Transmit Clock (TXCLK). In 10Base-T mode, the receive data pair will be quiescent during periods of inactivity and the Transmit Clock will be selected. In 100Base-T mode, the IDLE symbol is sent during periods of inactivity and the Recovered clock will be selected.

The **ICS1890** will only switch between clock sources when Receive Data Valid (RXDV) is de-asserted. During the period between Carrier Sense (CRS) being asserted and Receive Data Valid being asserted, a clock phase change of up to 360 degrees may occur. Following the de-assertion of Receive Data Valid a clock phase of 360 degrees may occur.

When Receive Data Valid is asserted, the Receive Clock frequency is 25% of the data rate, 2.5 MHz in 10Base-T mode and 25 MHz in 100Base-T mode. The **ICS1890** synchronizes Receive Data Valid, Received Data and Receive Error with Receive Clock (RXCLK).

Receive Data Valid **RXDV**

Receive Data Valid (RXDV) is generated by the **ICS1890**. It indicates that the **ICS1890** is recovering and decoding data nibbles on the Receive Data (RXD) data lines synchronous with the Receive Data Clock (RXCLK). It is the responsibility of the MAC to frame the nibbles since the **ICS1890** has no knowledge of the frame structure and is merely a “nibble” processor. The **ICS1890** asserts RXDV when it detects and recovers the pre-amble or the start of stream delimiter (SSD) and de-asserts it following the last data nibble or upon detection of a signal error. RXDV is synchronous with the Receive Data Clock (RXCLK).

Receive Data 3 **RXD3**

Receive Data 3 (RXD3) is the most significant bit of the receive data nibble. RXD is sourced by the **ICS1890**. When Receive Data Valid (RXDV) is asserted by the **ICS1890**, it will transfer the 4th bit of the symbol synchronously with Receive Clock (RXCLK).

Receive Data 2 **RXD2**

Receive Data 2 (RXD2) is sourced by the **ICS1890**. When Receive Data Valid (RXDV) is asserted by the **ICS1890**, it will transfer the 3rd bit of the symbol synchronously with Receive Clock (RXCLK).

Receive Data 1 **RXD1**

Receive Data 1 (RXD1) is sourced by the **ICS1890**. When Receive Data Valid (RXDV) is asserted by the **ICS1890**, it will transfer the 2nd bit of the symbol synchronously with Receive Clock (RXCLK).

Receive Data 0 **RXD0**

Receive Data 0 (RXD0) is the least significant bit of the receive data nibble. RXD0 is sourced by the **ICS1890**. When Receive Data Valid (RXDV) is asserted by the **ICS1890**, it will transfer the 1st bit of the symbol synchronously with Receive Clock (RXCLK).

Receive Error **RXER**

In 100 Mbps mode, the **ICS1890** detects two types of receive errors, errors occurring during the reception of valid frames and an error condition known as false carrier detect. False carrier detect is signaled so that repeater applications can prevent the propagation of false carrier detection. RXER always transitions synchronously with RXCLK.

The assertion of Receive Error (RXER) for one or more clock periods during the period when RXDV is asserted (receiving a frame) indicates that the **ICS1890** has detected a read channel error. There are three sources of read channel error: loss of receive signal, failure of the PLL to lock and invalid symbol detection. RXER may also be asserted when RXDV is de-asserted. The **ICS1890** will assert RXER and set RXD(3:0) to 1110 if a false carrier is detected. For a good carrier to be detected, the **ICS1890** looks continuously at the incoming IDLE stream (1111...) for two non-contiguous logic zeroes and then checks for the SSD of “JK.” In the event that two non-contiguous logic zeroes are detected but the JK symbol pair is not, then a false carrier condition is signaled and the IDLE condition is re-entered.

Carrier Sense **CRS**

The **ICS1890** asserts Carrier Sense (CRS) when it detects that either the transmit or receive lines are non-idle in half duplex mode. It is de-asserted when both the transmit and receive lines are idle in half duplex mode. CRS is not synchronous to either the transmit or receive clocks.

In full duplex mode and repeater mode, CRS is asserted only on receive activity.

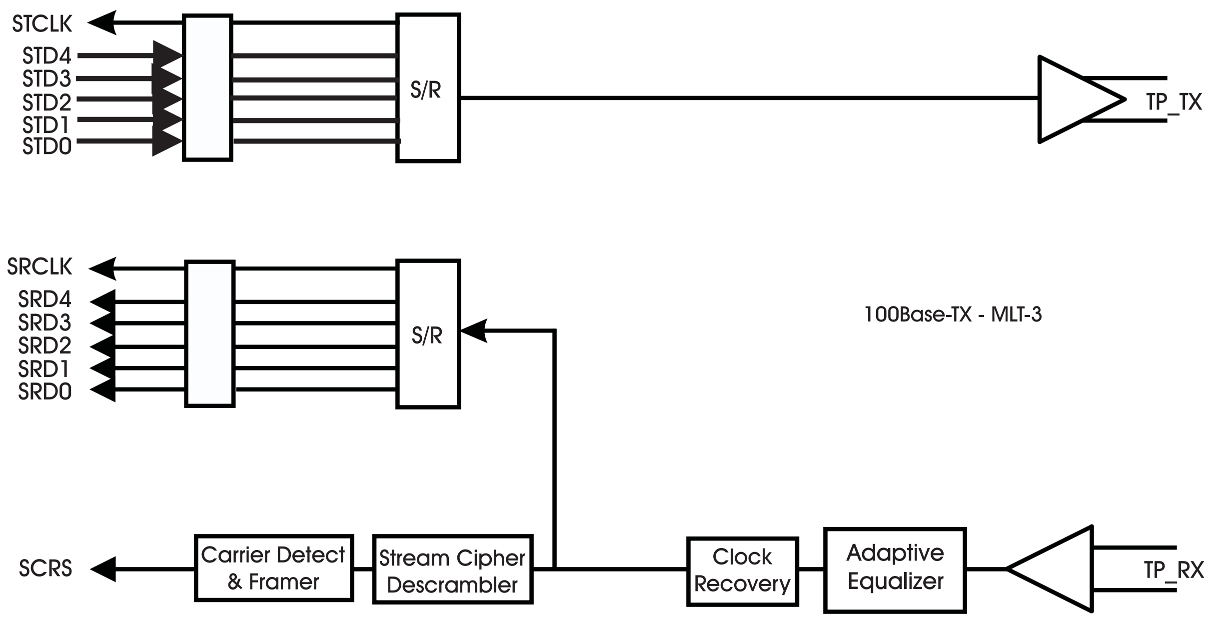
Collision Detected **COL**

The **ICS1890** asserts Collision Detected (COL) when it detects a receive carrier (non-idle condition) while transmitting (TXEN asserted).

In the 10 Mbps mode, the non-idle condition is detected by monitoring the unsquelched receive signal. In the 100 Mbps mode, the non-idle condition is detected by two non-contiguous zeros in any 10-bit code group. COL is not synchronous to either the transmit or receive clocks.

In full duplex mode, COL is disabled and always remains low.

In the 10 Mbps Node mode, COL will also be asserted as part of the signal quality error test (SQE). This behavior can be suppressed with the SQE Test Inhibit bit (18:2).



100M Stream Interface

100M Stream Interface - Pin Mapping

When the **ICS1890** is operating in the stream mode, the MII Data Interface is remapped to accommodate the 100M Stream Interface. The following table details the exact pin mapping. Each individual pin description also contains the "new 100M Stream Interface pseudo pin name" followed by the real MII Data Interface pin name that it is mapped onto.

100M Stream Interface provides a lower latency parallel interface producing an AMD PDR/PDT and twister type 5 bit unscrambled interface when the data is scrambled by the upper layer.

MII	Stream
TXCLK	STCLK
TXEN	(1)
TXER	STD4
TXD3	STD3
TXD2	STD2
TXD1	STD1
TXD0	STD0
RXCLK	SRCLK
RXDV	(2)
RXER	SRD4
RXD3	SRD3
RXD2	SRD2
RXD1	SRD1
RXD0	SRD0
CRS	SCRS
COL	(3)
LSTA	SD

(1) 100Base-TX is a continuous transmission system and the MAC/Repeater is responsible for sourcing IDLE symbols when it is not transmitting data when using the Stream Interface.

(2) Since data is not framed when this interface is used, RXDV has no meaning.

(3) Since the MAC/Repeater is responsible for sourcing both active and idle data, the PHY can not tell when it is transmitting in the traditional sense so collisions can not be detected.

Other mode configuration pins behave identically regardless of which data interface is used.

Transmit Clock STCLK/(TXCLK)

The Transmit Clock (STCLK) is a continuous clock signal generated by the **ICS1890** to synchronize the Transmit Data lines. In the 100M Stream Interface mode, the **ICS1890** clock frequency is 25 MHz.

Transmit Data 4 STD4/(TXER)

Transmit Data 4 (STD4) is the most significant bit and is sampled continuously by the **ICS1890** synchronously with the Transmit Clock.

Transmit Data 3 STD3/(TXD3)

Transmit Data 3 (STD3) is sampled continuously by the **ICS1890** synchronously with the Transmit Clock.

Transmit Data 2 STD2/(TXD2)

Transmit Data 2 (STD2) is sampled continuously by the **ICS1890** synchronously with the Transmit Data Clock.

Transmit Data 1 STD1/(TXD1)

Transmit Data 1 (STD1) is sampled continuously by the **ICS1890** synchronously with the Transmit Clock.

Transmit Data 0 STD0/(TXD0)

Transmit Data 0 (STD0) (the least significant bit) is sampled continuously by the **ICS1890** synchronously with the Transmit Clock.

Receive Clock SRCLK/(RXCLK)

The Receive Clock (SRCLK) is sourced by the **ICS1890**. There are two possible sources for the Receive Clock (SRCLK). When a carrier is present on the receive pair, the source is the recovered clock from the data stream. When no carrier is present on the receive pair, the source is the Transmit Clock (STCLK).

The Receive Clock frequency is 25 MHz in the 100M Stream Interface mode.

Receive Data 4 SRD4/(RXER)

Receive Error (SRD4) is the most significant bit of the receive data nibble and is continuously asserted by the **ICS1890**.

Receive Data 3 SRD3/(RXD3)

Receive Data 3 (SRD3) is continuously asserted by the **ICS1890**.

Receive Data 2 SRD2/(RXD2)

Receive Data 2 (SRD2) is continuously asserted by the **ICS1890**.

Receive Data 1 SRD1/(RXD1)

Receive Data 1 (SRD1) is continuously asserted by the **ICS1890**.

Receive Data 0 SRD0/(RXD0)

Receive Data 0 (SRD0) is the least significant bit of the receive data nibble.

Carrier Sense SCRS/(CRS)

Carrier Sense is provided in the 100M Stream Interface mode as a fast receive carrier look-ahead for optional application use. Carrier is detected using the same circuitry used in the MII Data Interface mode that is “bypassed” in this mode.

The **ICS1890** asserts Carrier Sense (SCRS) when it detects that either the transmit or receive lines are non-idle in half duplex mode. It is de-asserted when both the transmit and receive lines are non-idle in half duplex mode. SCRS is not synchronous to either the transmit or receive clocks.

In full duplex mode and repeater mode, SCRS is asserted only on receive activity.

Signal Detect SD/(LSTA)

This signal is asserted when the PLL detects 100Base-T activity on the receive channel.

10M Serial Interface

10M Serial Interface - Pin Mapping

When the **ICS1890** is operating in the 10M Serial mode, the MII Data Interface is remapped to accommodate the 10M Serial Interface. The following table details the exact pin mapping. Each individual pin description also contains the "new 10M Serial Interface pseudo pin name" followed by the real MII Data Interface pin name that it is mapped onto.

MII	10M Serial
TXCLK	10TCLK
TXEN	10TXEN
TXER	(1)
TXD3	
TXD2	
XD1	
TXD0	10TD
RXCLK	10RCLK
RXDV	10RXDV
RXER	(1)
RXD3	
RXD2	
RXD1	
RXD0	10RD
CRS	10CRS
COL	10COL
LSTA	LSTA

(1) Error generation and detection is not supported by 10Base-T. Other mode configuration pins behave identically regardless of which data interface is used.

Transmit Clock 10TCLK/(TXCLK)

The Transmit Clock (10TCLK) is a continuous clock signal generated by the **ICS1890** to synchronize the Transmit Data lines. In the 10M Serial Interface mode, the **ICS1890** clock frequency is 10 MHz.

Transmit Enable 10TXEN/(TXEN)

Transmit Enable (10TXEN) indicates to the **ICS1890** that the MAC is sending valid data nibbles for transmission on the physical media. Synchronous with its assertion, the **ICS1890** will begin reading the serial data on the transmit data line. The **ICS1890** terminates transmission of data following the de-assertion of Transmit Enable.

Transmit Data 10TD/(TXD0)

Transmit Data 0 (10TD) is the serial transmit data bit and is sampled continuously by the **ICS1890** synchronously with the Transmit Clock.

Receive Clock 10RCLK/(RXCLK)

The Receive Clock (10RCLK) is sourced by the **ICS1890** and is 10 MHz in frequency. There are two possible sources for the Receive Clock. When a carrier is present on the receive pair, the source is the recovered clock from the data stream. When no carrier is present on the receive pair, the source is the Transmit Clock. In 10Base-T mode, the receive data pair will be quiescent during periods of inactivity and the Transmit Clock will be selected.

The **ICS1890** will only switch between clock sources when Receive Data Valid is de-asserted. During the period between Carrier Sense (CRS) being asserted and Receive Data Valid being asserted, a clock phase change of up to 360 degrees may occur. Following the de-assertion of Receive Data valid, a clock phase of 360 degrees may occur.

Receive Data Valid 10RXDV/(RXDV)

Receive Data Valid (10RXDV) is generated by the **ICS1890**. It indicates that the **ICS1890** is recovering serial data on the Receive Data (10RD) line synchronous with the Receive Data Clock.

The **ICS1890** asserts RXDV when it detects and recovers the preamble or the start of stream delimiter (SSD) and de-asserts it following the last data nibble or upon detection of a signal error. RXDV is synchronous with the Receive Data Clock (10RCLK).

Receive Data 10RD/(RXD0)

Receive Data 0 (10RD) is the received serial data stream.

Carrier Sense 10CRS/(CRS)

The **ICS1890** asserts Carrier Sense (CRS) when it detects that either the transmit or receive lines are non-idle in half duplex mode. It is de-asserted when both the transmit and receive lines are idle in half duplex mode. CRS is not synchronous to either the transmit or receive clocks.

In full duplex mode and repeater mode, CRS is asserted only on receive activity.

Collision Detected **10COL/(COL)**

The **ICS1890** asserts Collision Detected (COL) when it detects a receive carrier (non idle condition while transmitting (TXEN asserted).

In the 10 Mbps mode, the non-idle condition is detected by monitoring the un-squelched receive signal. COL is not synchronous to either the transmit or receive clocks.

In full duplex mode, COL is disabled and always remains low.

In the 10 Mbps Node mode, COL will also be asserted as part of the signal quality error test (SQE). This behavior can be suppressed with the SQE Test Inhibit bit (18:2).

Link Pulse Interface

Link Pulse Interface - Pin Mapping

When the **ICS1890** is operating in the Link Pulse mode, the MII Data Interface is remapped to accommodate the Link Pulse Interface. The following table details the exact pin mapping. Each individual pin description also contains the “new Link Pulse Interface pseudo pin name” followed by the real MII Data Interface pin name that it is mapped onto.

MII	Link Pulse
TXCLK	LTCLK
TXEN	TXER
LPTX	
TXD3	
TXD2	
XD1	
TXD0	
RXCL	K LRCLK
RXDV	
RXER	LPRX
RXD3	
RXD2	
RXD1	
RXD0	
CRS	
COL	
LSTA	SD

Other mode configuration pins behave identically regardless of which data interface is used.

Transmit Clock **LTCLK/(TXCLK)**

The Transmit Clock (10TCLK) is a continuous clock signal generated by the **ICS1890** with a frequency of 25 MHz.

Transmit Link Pulse **LPTX/(TXER)**

Data presented on this input will be transmitted as a Link Pulse of approximately the same duration.

Receive Clock **LRCLK/(RXCLK)**

The Receive Clock (LRCLK) is sourced by the **ICS1890** and is 25 MHz in frequency.

Receive Link Pulse **LPRX/(RXER)**

Receive activity that is qualified as a Link Pulse will be output on this pin as a high level of approximately the same duration as the Link Pulse.

Signal Detect **SD/(LSTA)**

This signal is asserted when the PLL detects 100Base-T activity on the receive channel.

MII Management Interface

Management Data Clock MDC

The Management Data Clock (MDC) is used by the **ICS1890** to synchronize the transfer of management information to or from the **ICS1890** using the serial MDIO data line.

Management Data Input/Output MDIO

The Management Data Input/Output (MDIO) is a tri-statable line driven by station management to transfer command information or driven by the **ICS1890** to transfer status information. All transfers and sampling are synchronous with MDC. If the **ICS1890** is to be used in an application which uses the mechanical MII specification, MDIO must have a 1.5KΩ±5% pull-up at the **ICS1890** end and a 2KΩ±5% pull-down at the station management end. This enables station management to deter-mine if the connection is intact.

Twisted Pair Interface

Transmit Pair TP_TX+ & TP_TX-

The Transmit pair TP_TX+ and TP_TX- carries the serial bit stream for transmission over the UTP cable. The current-driven differential driver is programmed to produce two-level (10Base-T, Manchester) or three-level (100Base-TX, MLT-3) signals depending on the mode of operation selected (manually or by Auto-Negotiation). These output signals interface directly with an isolation transformer.

Note that these pins may be tristated using the TPTRI control pin.

Receive Pair TP_RX+ & TP_RX-

The Receive pair TP_RX+ and TP_RX- carries the serial bit stream from the mandatory isolation transformer. The serial bit stream may be two-level (10Base-T, Manchester) or three-level (100Base-TX, MLT-3) signals depending on the ICS mode of operation

10M Transmit Current Set Resistor 10TCSR

A resistor is required to be connected between this pin and the nearest transmit ground to set the value of the transmit current used in 10M mode.

The value and tolerance of this resistor is specified in the Electricals section.

100M Transmit Current Set Resistor 100TCSR

A resistor is required to be connected between this pin and the nearest transmit ground to set the value of the transmit current used in 100M mode.

The value and tolerance of this resistor is specified in the Electricals section.

Clock Reference Interface

Frequency Reference (REF_IN & REF_OUT)

These pins connect to the 25 MHz crystal or the frequency reference source.

When a frequency reference source like a crystal oscillator module is used, its output should be connected to REF_IN and REF_OUT should be left unconnected.

Configuration and Status Interface

Node/Repeater Mode NOD/REP

When this input is logic zero, the device will default to Node operation. SQE test will default to on for 10Base-T.

When this input is logic one, the device will default to Repeater operation. SQE test will default to off and Carrier Sense will be determined by receive activity only.

This pin setting also affects which clock, TXCLK or REF_IN, is used to latch the transmit data, TXD. See the description of the ITCLS pin for the details.

MII Data/Stream Interface Select MII/SI

This input pin selects the MAC to PHY interface to be used. When the input is low the MII Data Interface is selected.

When this input is high, the "Stream" Interface is selected. The "Stream" Interface that is used depends on the settings of the 10/100SEL and 10/LP pins which allow selection of the 100M Stream Interface, 10M/Serial Interface, or Link Pulse Interface.

10M Serial/Link Pulse Interface Select 10/LP

This input selects between the 10M Serial and Link Pulse Interfaces when Stream Interface mode is selected with the MII/SI pin. When this input is low and Stream Interface mode is selected, the 10M Serial Interface is selected. When this input is high and Stream Interface mode is selected, the Link Pulse Interface is selected.

Hardware/Software Priority Select HW/SW

When this pin is logic zero, hardware pins have priority over software settings. The 10/100SEL pin becomes an input and controls speed selection. The DPXSEL pin becomes an input and controls duplex selection. The ANSEL pin becomes an input and chooses configuration with or without Auto-Negotiation.

When configuration through Auto-Negotiation is selected, the DPXSEL and 10/100SEL settings control the Auto-Negotiation register 4 default settings and Auto-Negotiation is enabled. When configuration without Auto-Negotiation is selected DPXSEL controls the duplex setting and 10/100SEL controls the data rate setting.

When this pin is a logic one, software bits have priority over hardware pin settings. The 10/100SEL pin becomes an output indicating the link speed when the link is established and parallels bit (17:15). The DPXSEL pin becomes an output indicating the link duplex state when the link is established and parallels bit (17:14). The ANSEL pin becomes an output indicating whether auto-negotiation is being used and parallels bit (0:12).

10/100 Select 10/100SEL

This pin is an input or an output depending on the setting of the HW/SW pin.

In HW mode, it is an input and controls speed selection directly or through Auto-Negotiation. When the input is low, 10Base-T is selected. When the input is high, 100Base-TX is selected.

In SW mode, this pin is an output and correctly reflects the selected speed when the link is established (LSTA is asserted). The output is low when 10Base-T is selected and high when 100Base-TX is selected which gives the same indication as register bit (17:15).

Note this pin also affects the MAC - PHY interface that is used in conjunction with the MII/SI pin.

Duplex Select DPXSEL

This pin is an input or an output depending on the setting of the HW/SW pin.

In HW mode, it is an input and controls duplex selection directly or through Auto-Negotiation. When the input is low, Half Duplex is selected. When the input is high, Full Duplex is selected.

In SW mode, this pin is an output and correctly reflects the selected duplex mode when the link is established (LSTA is asserted). The output is low when Half Duplex is selected and high when Full Duplex is selected which gives the same indication as register bit (17:14).

In Full Duplex mode, CRS is asserted only on receive activity. In Full Duplex mode, COL is disabled and always remains low.

Auto-Negotiation Select ANSEL

This pin is an input or output depending on the setting of the HW/SW pin.

In HW mode, it is an input and controls the enabling of Auto-Negotiation. When the input is low, Auto-Negotiation is disabled. When the input is high, Auto-Negotiation is enabled and the single technology selected by 10/100SEL and DPXSEL is advertised.

In SW mode, this pin is an output and reflects whether Auto-Negotiation has been enabled or disabled. The output is low when Auto-Negotiation is disabled and high when Auto-Negotiation is enabled which gives the same indication as register bit (0:12).

Invert Transmit Clock Latching Setting ITCLS~

The **ICS1890** allows transmit data to be latched relative to either TXCLK or REF_IN. Latching the data to TXCLK is the behavior specified in the 100Base-T MII specification, but in some applications it is desirable to latch data with the REF_IN clock. An example of where this might be beneficial is in a repeater application where all data transmission on multiple 1890s need to be synchronized to a common clock.

To select the proper setting of this pin, first choose the setting of the NOD/REP pin. Then select the setting of the ITCLS pin that latches the transmit data with the clock of your choice. The following table shows the possible combinations. This pin has an internal pull-up so it may be left not connected for some applications.

NOD/REP	ITCLS	Latching Clock
NOD (0)	0	REF_IN
	1	TXCLK
REP (1)	0	TXCLK
	1	REF_IN

TP_TXTristate **TPTRI**

When this pin is set to a logic zero, the twisted pair transmitter output pins will be enabled normally to source 100Base-TX or 10Base-T data.

When this pin is set to a logic one, the twisted pair transmitter output pins will be tristated.

MAC - PHY Receive Interface Tristate **RXTRI**

When this input is a logic zero the selected MAC-PHY interface behaves normally.

When this input is a logic one, the RXCLK, RXD[3:0], RXER, and RXDV pins are tristated. This allows repeater designs to bus the shared receive lines without requiring extra tristatable buffers on each port.

Note that the CRS and COL pins are not tristated. This allows repeater logic to use these signals to determine which receive port to enable.

Link Status **LSTA**

This output reflects the current Link Status. It is similar to bit (1:2) but changes dynamically instead of latching on a link failure. The output is low when the link is invalid and is high when a valid link has been established.

When this bit is high, the 10/100SEL and DPXSEL bits can be observed to determine what type of link has been established.

Cipher Locked Status **LOCK**

This output reflects the status of the Stream Cipher decoder block. When the Stream Cipher has not locked onto the incoming data stream, this output will be a logic zero. When the Stream Cipher has locked onto the incoming data stream, this output will be a logic one.

Note that the Stream Cipher will only lock onto 100Base-TX data (or IDLE symbols) and will not lock when 10Base-T data is present.

System Reset **RESET~**

When grounded, this pin causes the **ICS1890** to enter a re-set/ low power state. On the low to high transition of RESET, the device will begin to complete its reset cycle. Upon comple-tion, the **ICS1890** will be initialized its default state.

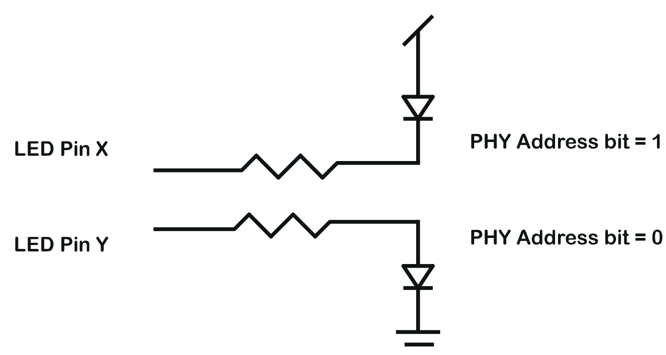
While this pin is held low, the device is kept in its low power mode. Power savings and timings are shown in the Electricals section.

LED/PHY Address Usage

The **ICS1890** device uses a unique pin sharing scheme that allows the 5 LED pins to also be used to set the PHY address. At power-up and reset they define the MII PHY address of the device. Subsequent to power-up and reset, they become LED status indicators.

The PHY address can be any number between 0 and 31. When PHY address 0 is used, the device's MII interface starts out Isolated and must be enabled through the MII management port (Reg 0 bit 10), as defined by the IEEE specification. All other addresses leave the MII interface active.

The actual value used for the individual PHY address bits depends on the configuration of the LED components. This is shown in the figure below. When a "1" value is desired the LED and resistor are connected between the LED pin and Vdd (LED Pin X). When a "0" value is desired the LED and resistor are connected between the LED pin and Ground (LED Pin Y). The special driver will sense the polarity and adjust its drive logic to appropriately turn the LED light on or off.



Resistor values should be in the range of 510Ω to 10kΩ. A 1kΩ resistor is recommended.

If LEDs are not required for the application, only a resistor is required to set the PHY address.

If LEDs are not required for the application and the **ICS1890** will not be accessed with the serial MII management interface, then only a single resistor to VDD on any one of the LED pins is required. This will ensure that the PHY address is not zero, which would cause the **ICS1890** to power up in the isolated state with no way for management to enable the MII interface.

Phy Address 4 - Receive Data LED P4RD

At power-up and reset, this pin is sampled for a logic high or zero. If a logic one is detected, a value of 16 is set in the configuration register.

The **ICS1890** sets this bit to the appropriate value to turn on the LED when receive data is detected. This signal is stretched ensure that a single packet will be seen. If the packet stream is continuous, the LED will appear permanently on.

Phy Address 3 - Transmit Data LED P3TD

At power-up and reset, this pin is sampled for a logic high or zero. If a logic one is detected, a value of 8 is set in the configuration register.

The **ICS1890** sets this bit to the appropriate value to turn on the LED when transmit data is detected. This signal is stretched to ensure that a single packet will be seen. If the packet stream is continuous, the LED will appear permanently on.

Phy Address 2 - Link Integrity LED P2LI

At power-up and reset, this pin is sampled for a logic high or zero. If a logic one is detected, a value of 4 is set in the configuration register.

The **ICS1890** sets this bit to the appropriate value to turn on the LED when the Link Integrity status is OK.

Phy Address 1 - Collision LED P1CL

At power-up and reset, this pin is sampled for a logic high or zero. If a logic one is detected, a value of 2 is set in the configuration register.

The **ICS1890** sets this bit to the appropriate value to turn on the LED when a collision is detected. This signal is stretched to ensure that a single collision will be seen. If the collisions are continuous, the LED will appear permanently on.

Phy Address 0 - Activity LED P0AC

At power-up and reset, this pin is sampled for a logic high or zero. If a logic one is detected, a value of 1 is set in the configuration register.

The **ICS1890** sets this bit to the appropriate value to turn on the LED when either transmit or receive activity is detected. This signal is stretched to ensure that a single activity event will be seen. If the activity is continuous, the LED will appear permanently on.

Power Supply

These 7 VDD and 8 VSS pins supply power to the **ICS1890** device.

ICS1890 Power Supply Isolation and Filtering

It is important to properly isolate the **ICS1890** 10/100Base-TX Physical Layer Device from noise sources in a system design. There are two key areas to consider, isolation from digital noise and noise coupling between the transmitter and receiver.

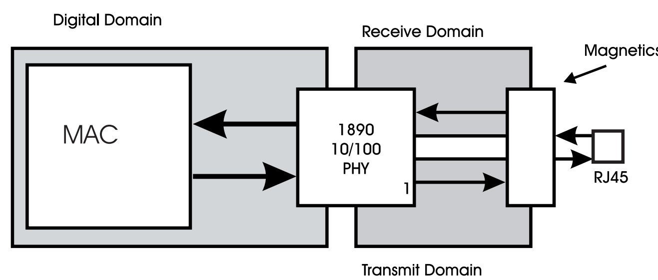
Filtering for the **ICS1890** is accomplished by separating the power supply into three domains: digital, transmit, and receive. All supply pins on the device fall into one of these three categories as shown in the table below.

In the above table, each supply pin is followed directly by its ground pin. Each supply pair should be bypassed with a 0.1µF capacitor located as close to the device as possible.

Digital Domain	Transmit Domain	Receive Domain
41 VDD 8 VDD 40 VSS 7VSS		16 VDD 18 VDD 17 VSS
54 VDD 51 VSS	56 VDD 55 VSS	25 VDD 29 VSS
57 VDD 63 VSS		

The PCB board may have separate power and ground planes for the **ICS1890**. The power planes could be split into three domains following the pin isolation. A single, uniform plane should be used for ground. Power plane placement is illustrated in the figure below.

Point-to-point trace routing for power connections may be used instead of actual power "planes" if required by printed circuit board constraints.



Both the Receive and Transmit Domains should be connected to the Digital Domain or main supply through a ferrite bead or inductor, with a value of .1µH to 1µH. The best filter configuration is a pi filter composed of a .1µH capacitor, .1µH ferrite bead, and a .1µH capacitor at the device pin.

Reserved & N/C Pins

Four pins are labeled "Reserved" or "N/C." These pins should be left unconnected. Connecting these pins to ground or power may prevent the device from operating properly

Pin Descriptions

PIN NUMBER	PIN NAME	I/O	TYPE	Description
1	NOD/REP	I	TTL-compatible	Node/Repeater Mode
2	10/100SEL	I/O	TTL-compatible	10/100 Select
3	10TCSR	I		10M Transmit Current Set Resistor
4	100TCSR	I		100M Transmit Current Set Resistor
5	TP_TX	O		Twisted Pair Transmit Data+
6	TP_TX-	O		Twisted Pair Transmit Data-
7	VSS			
8	VDD			Ditigal Domain Power (Transmitter)
9	TPTRI	I	TTL-compatible	Twisted Pair Tristate
10	TP_RX+	I		Twisted Pair Receive Data+
11	TP_RX-	I		Twisted Pair Receive Data-
12	N/C			
13	ITCLS~	I	TTL-compatible	Invert Transmit Clock Latching Setting
14	N/C			
15	N/C			
16	VDD			Receive Domain Power (Receiver)
17	VSS			
18	VDD			Receive Domain Power (Receiver)
19	MII/SI	I	TTL-compatible	MII Data/Stream Interface
20	REG	I	TTL-compatible	Ground for high order register access
21	LSTA*	O	TTL-compatible	Link Status
22	RESET~	I	TTL-compatible	System Reset
23	HW/SW	I	TTL-compatible	Hardware/Software Priority
24	DPXSEL	I/O	TTL-compatible	Duplex Select
25	VDD			Receive Domain Power (RPLL)
26	N/C			
27	LOCK	O	TTL-compatible	Cipher Lock
28	10/LP	I	TTL-compatible	10M Serial/Link Pulse Interface
29	VSS			
30	MDIO	I/O	TTL-compatible	Management Data Input/Output
31	MDC	I	TTL-compatible	Management Data Clock
32	RXD3*	O	TTL-compatible	Receive Data 3

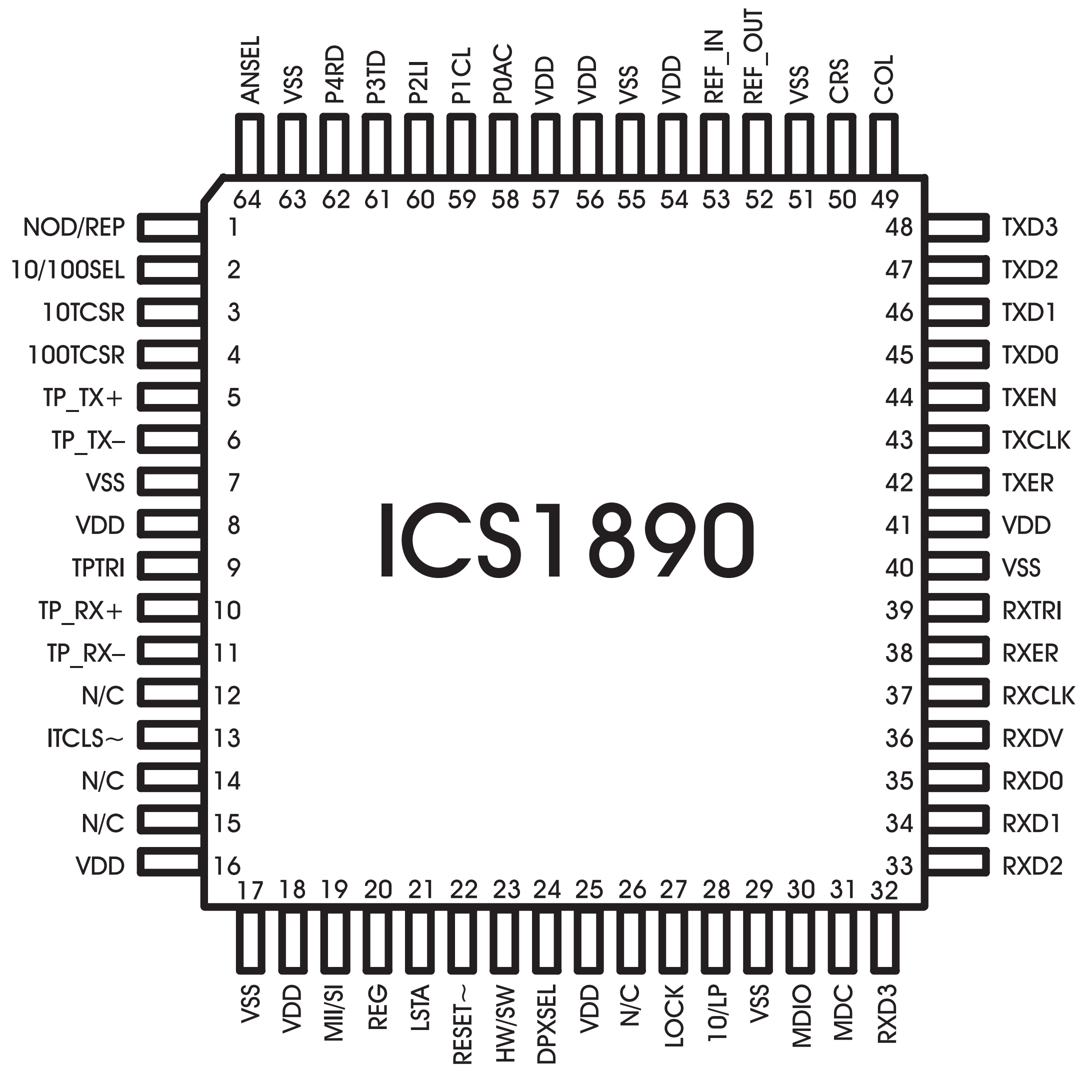
* Redefined for other MAC-PHY interfaces.

Pin Descriptions

PIN NUMBER	PIN NAME	I/O	TYPE	DESCRIPTION
33	RXD2*	O	TTL-compatible	Receive Data 2
34	RXD1*	O	TTL-compatible	Receive Data 1
35	RXD0*	O	TTL-compatible	Receive Data 0
36	RXDV*	O	TTL-compatible	Receive Data Valid
37	RXCLK*	O	TTL-compatible	Receive Clock
38	RXER	O	TTL-compatible	Receive Error
39	RXTRI	I	TTL-compatible	Receive MAC-PHY Interface Tristate
40	VSS			
41	VDD			Digital Domain Power
42	TXER*	I	TTL-compatible	Transmit Error
43	TXCLK*	O	TTL-compatible	Transmit Error
44	TXEN*	I	TTL-compatible	Transmit Enable
45	TXD0*	I	TTL-compatible	Transmit Data 0
46	TXD1*	I	TTL-compatible	Transmit Data 1
47	TXD2*	I	TTL-compatible	Transmit Data 2
48	TXD3*	I	TTL-compatible	Transmit Data 3
49	COL*	O	TTL-compatible	Collision Detect
50	CRS*	O	TTL-compatible	Carrier Sense
51	VSS			
52	REF_OUT	O		Frequency Reference Output
53	REF_IN	I	CMOS-compatible	Frequency Reference Input
54	VDD			Digital Domain Power
55	VSS			
56	VDD			Transmit Domain Power (TPLL)
57	VDD			Digital Domain Power
58	P0AC	I/O	LED	Special PHY ID 0/Activity LED
59	P1CL	I/O	LED	Special PHY ID 1/Collision det LED
60	P2LI	I/O	LED	Special PHY ID 2/Link Integrity LED
61	P3TD	I/O	LED	Special PHY ID 3/Transmit data LED
62	P4RD	I/O	LED	Special PHY ID 4/Receive data LED
63	VSS			
64	ANSEL	I/O	TTL-compatible	Auto-Negotiation Select

* Redefined for other MAC-PHY interfaces.

Pin Configuration



Absolute Maximum Ratings

V_{DD} (measured to V_{SS}) 7.0V
Digital Inputs/Outputs . . . . V_{SS}-0.5 to V_{DD}+0.5V
Storage Temperature. . . . . -65 to 150°C
Junction Temperature . . . . 175°C
Soldering Temperature . . . . 260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Ambient Operating Temp.	TA		0	+70	°C
Power Supply	VSS VDD		0.0 +4.75	0.0 +5.25	V V

Recommended Component Values

PARAMETER	MIN	TYP	MAX	UNITS
Crystal Oscillator Frequency*		25		MHz
Crystal Oscillator Frequency Tolerance	-50		+50	ppm
10TCSR Resistor Value	1.4	2.0	2.61	KΩ
100TCSR Resistor Value	6.49	6.81	7.50	KΩ
LED Resistor Value	510	1000	10,000	Ω

* CMOS output drive recommended

Note: This matches the IEEE requirement in the 100Base-X standard definition for the code-bit-timer (24.2.3.4) which is more stringent than the basic media independent interface (MII) specification for the TX_CLK of ±100ppm (22.2.2.1).

DC Characteristics

$V_{DD} = V_{MIN}$ to V_{MAX}, V_{SS} = OV, $T_A = T_{MIN}$ to T_{MAX}

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
IC Supply Current	I_{DD}	V_{DD}=5.25V	-	195	mA

TTL Input/Output

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
TTL Input High Voltage	V_{IH}	VDD=5V, VSS=0V	2.0	-	V
TTL Input Low Voltage	V_{IL}	VDD=5V, VSS=0V	-	0.8	V
TTL Output High Voltage	V_{OH}	VDD=5V, VSS=0V	2.4	-	V
TTL Output Low Voltage	V_{OL}	VDD=5V, VSS=0V	-	0.4	V
TTL Driving CMOS, Output High Voltage	V_{OH}	VDD=5V, VSS=0V	3.68	-	V
TTL Driving CMOS, Output Low Voltage	V_{OL}	VDD=5V, VSS=0V	-	0.4	V
TTL/CMOS Output Sink Current	I_{OL}	VDD=5V, VSS=0V	8	-	mA
TTL/CMOS Output Source Current	I_{OH}	VDD=5V, VSS=0V	-	-0.4	mA

REF_IN Input

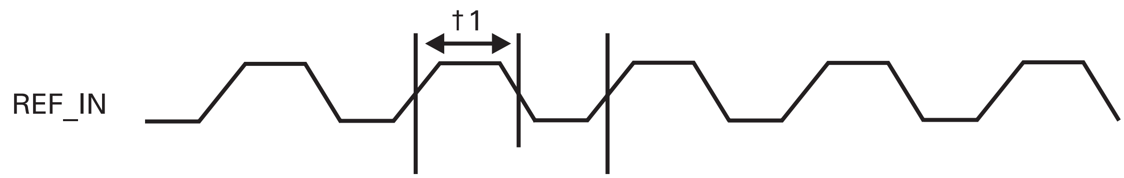
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	V_{IH}	VDD=5V, VSS=0V	3.5	-	V
Input Low Voltage	V_{IL}	VDD=5V, VSS=0V	-	1.5	V

Note: REF_IN Input switch point is 50% of VDD.

PARAMETER (condition)	MIN	TYP	MAX	UNITS
MII Input Pin Capacitance	-	8	-	pF
MII Output Pin Capacitance	-	14	-	pF
MII Output Pin Impedance	-	38	-	Ohms

Note: Total system operating current will include load current required by the Tx transformer.

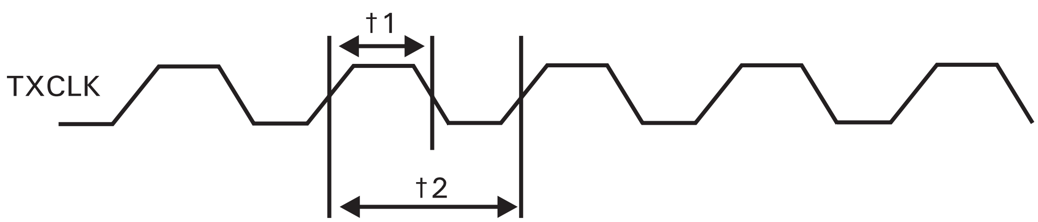
Clock - Reference In (REF_IN)



T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	REF_IN Duty Cycle	45	50	55	%
t2	REF_IN Period	-	40	-	ns

Note: REF_IN switching point is 50% of VDD.

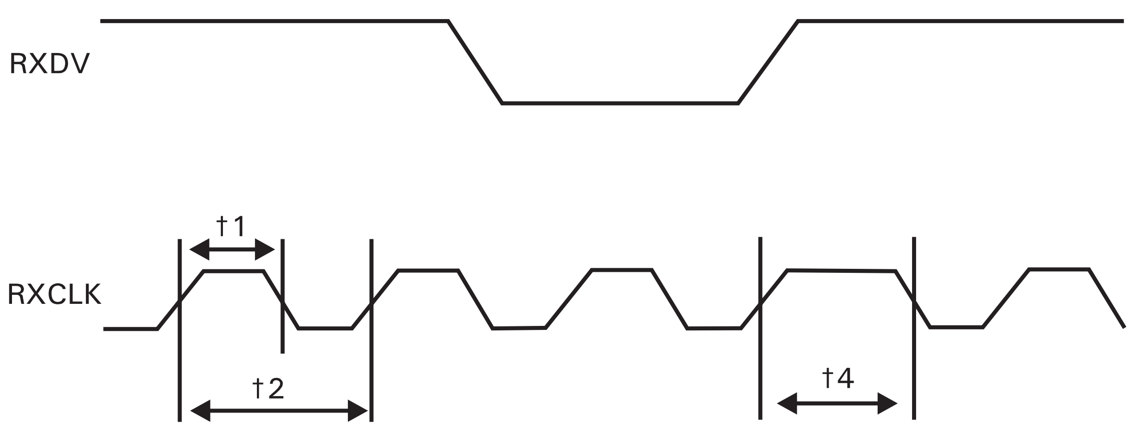
MII - Transmit Clock Tolerance



T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	TXCLK Duty Cycle	35	50	65	%
t2a	TXCLK Period (100Base-T/MII Interface)	-	40	-	ns
t2b	TXCLK Period (10Base-T/MII Interface)	-	400	-	ns
t2c	TXCLK Period (100Base-T/100M Stream Interface)	-	40	-	ns
t2d	TXCLK Period (10Base-T/10M Serial Interface)	-	100	-	ns

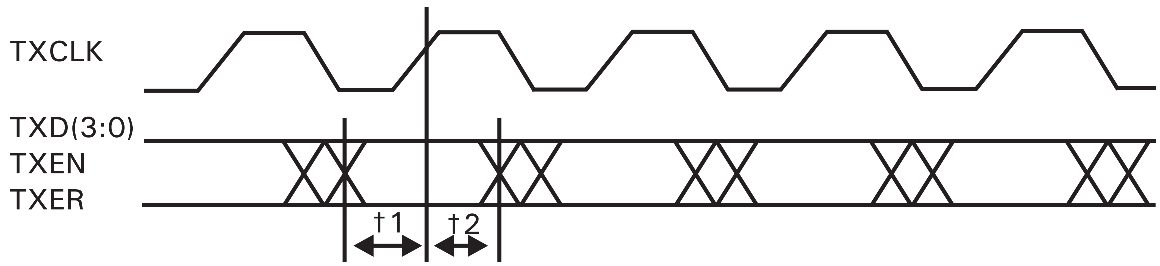
Note: TXCLK Duty Cycle = REF_IN Duty Cycle ±5%.

MII - Receive Clock Behavior



T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	RXCLK Duty Cycle	45	50	55	%
t2a	RXCLK Period (100Base-T/MII Interface)	-	40	-	ns
t2b	RXCLK Period (10Base-T/MII Interface)	-	400		ns
t2c	RXCLK Period (100Base-T/100M Stream Interface)	-		40	ns
t2d	RXCLK Period (10Base-T/10M Serial Interface)	-		100	ns
t4	RXDV Asserted Nominal Clock to Recovered Clock Cycle Extension	-	-	65	ns

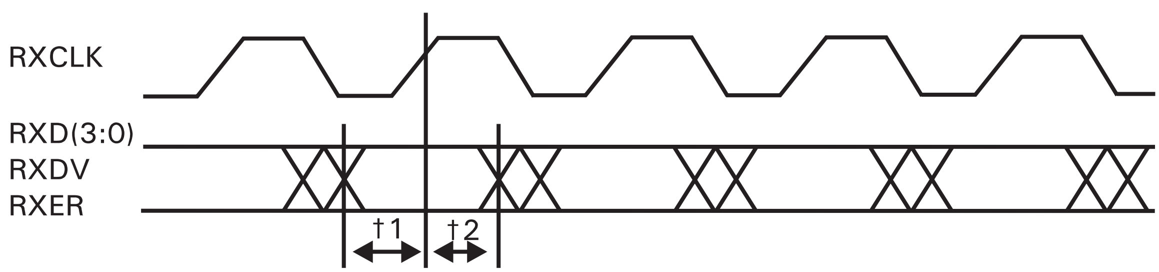
MII/100M Stream - Synchronous Transmit Timing



T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	TXD, TXEN, TXER Setup to TXCLK rise	10	-	-	ns
t2	TXD, TXEN, TXER Hold after TXCLK rise	0	-	-	ns

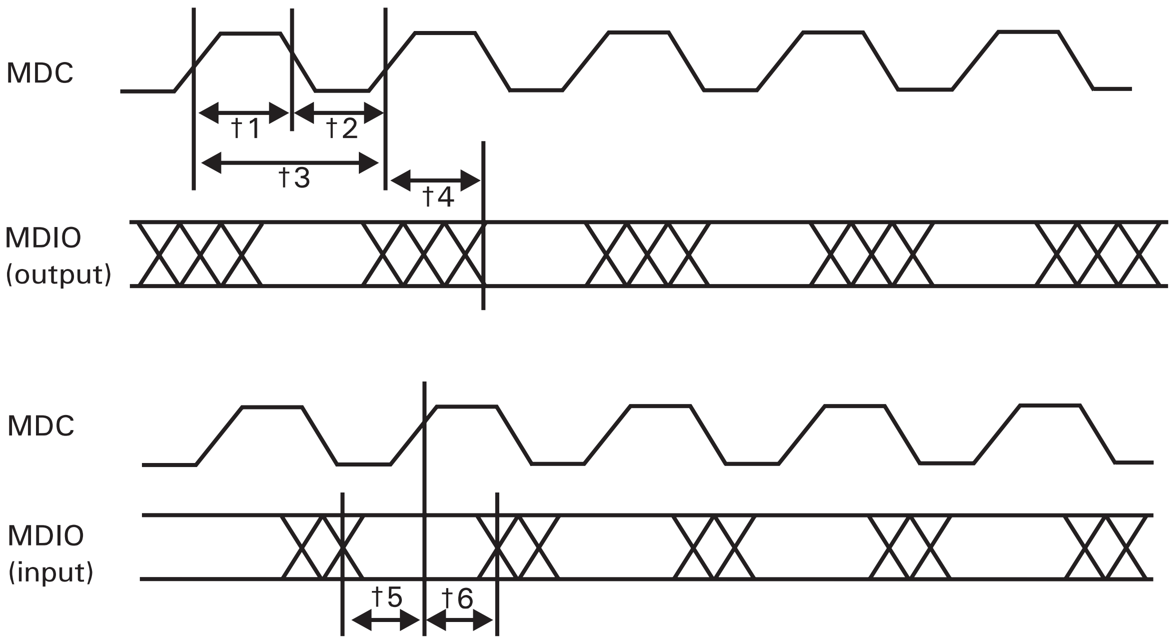
Note: With ITCLS low (or in repeater mode) timing is with respect to REF_IN

MII/100M Stream - Synchronous Receive Timing



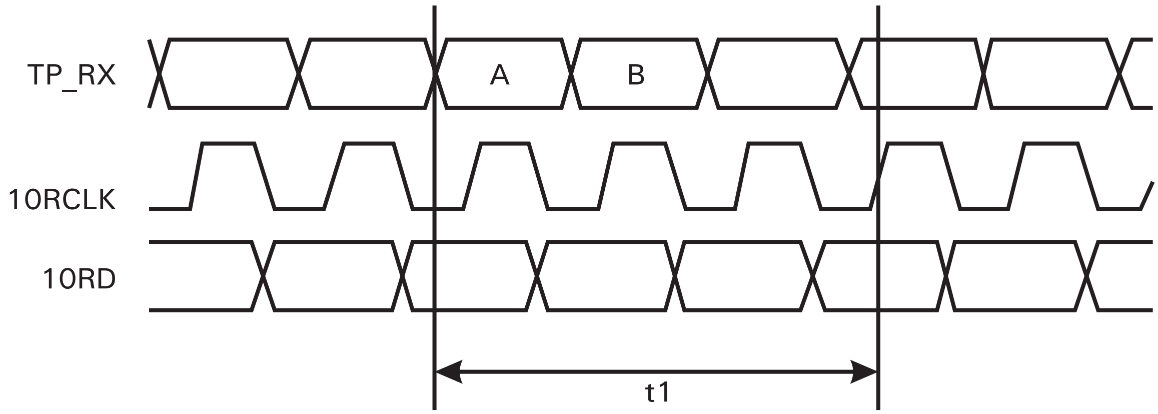
T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	RXD, RXDV, RXER Setup to RXCLK rise	10.0	-	-	ns
t2	RXD, RXDV, RXER Hold after RXCLK rise	10.0	-	-	ns

MII - Management Interface Timing



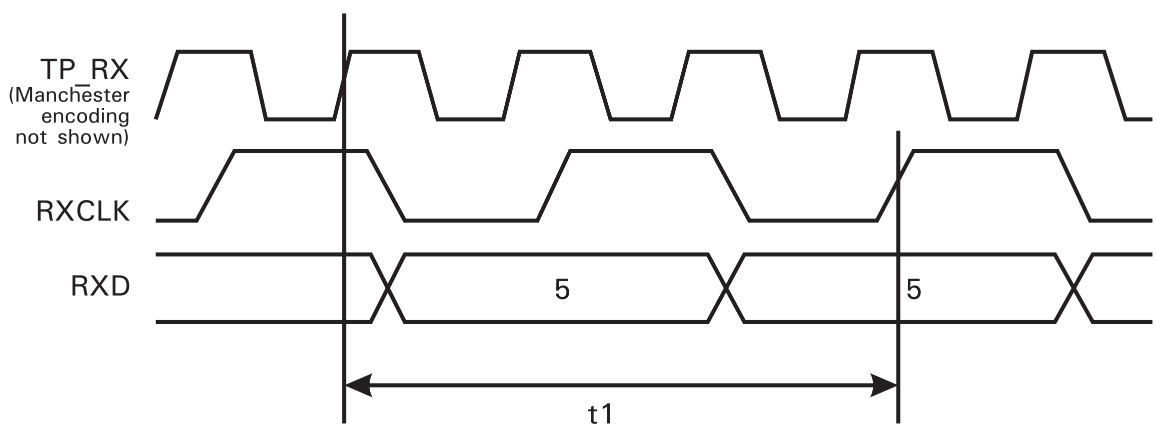
T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	MDC Minimum High Time	160	-	-	ns
t2	MDC Minimum Low Time	160	-	-	ns
t3	MDC Period	400	-	-	ns
t4	MDC rise to MDIO valid	0	-	300	ns
t5	MDIO Setup to MDC	10	-	-	ns
t6	MDIO Hold after MDC	10	-	-	ns
t7	Maximum allowable frequency (50pF Loading)	-	-	10	MHz

Receive Latency (10M Serial)



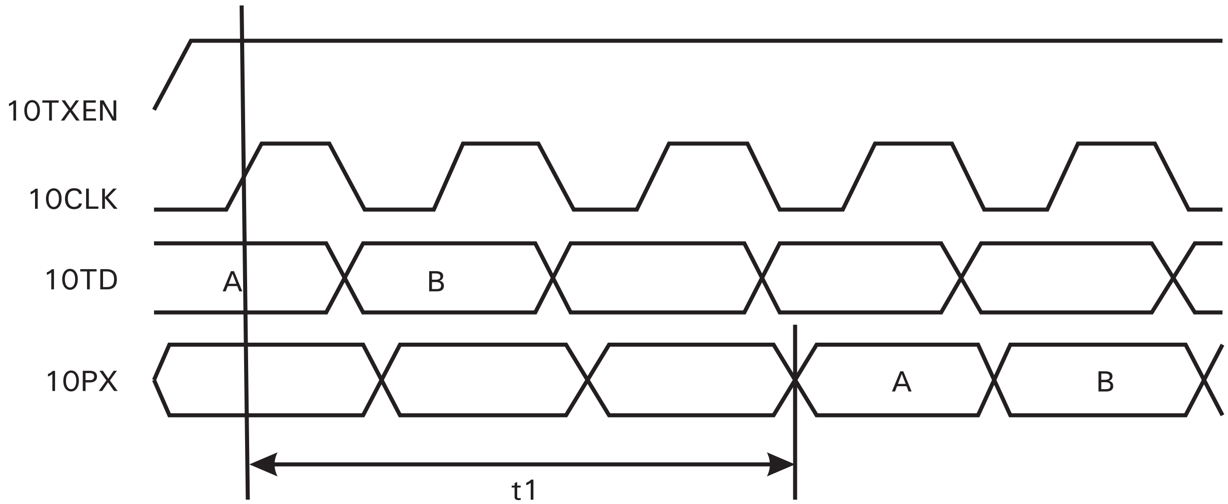
T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	TP_RX input to 10RD delay (10M Serial Interface)	15	-	16.5	bits

Receive Latency (10M MII)



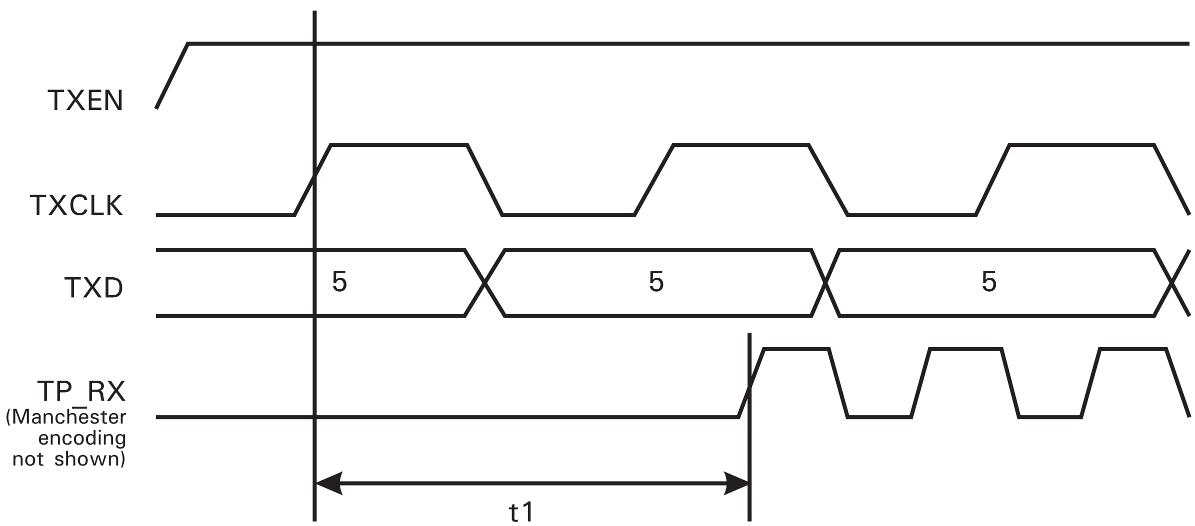
T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	1st bit of /5/ on TP_RX to /5/ on RXD (10M MII)	18	-	19.5	bits

Transmit Latency (10M Serial)



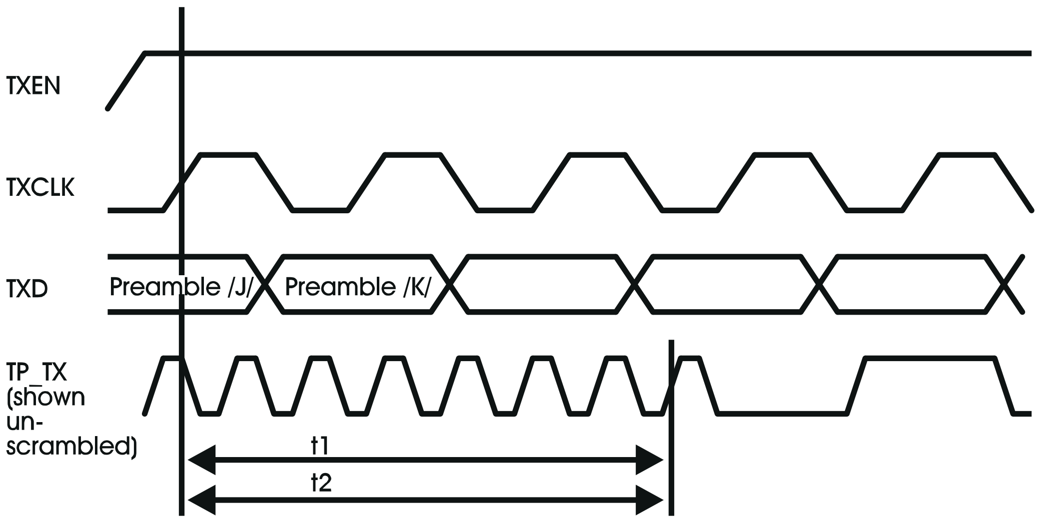
T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	10TD in to TP_TX out delay (10M Serial Interface)	-	1.5	-	bits

Transmit Latency (10M MII)



T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	TXD sampled to MDI Output of 1st bit (10M MII)	-	1.5	-	bits

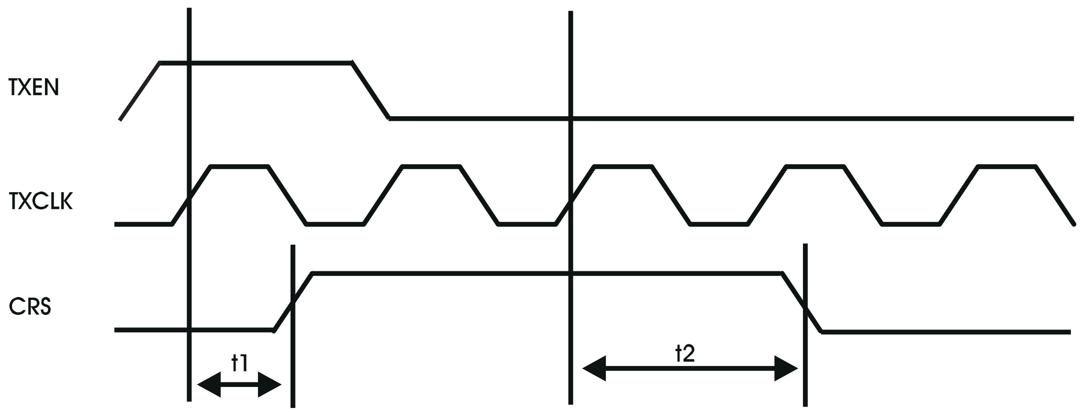
Transmit Latency (MII/100M Stream)



T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	TXEN sampled to MDI Output 1st bit of /J/ (MII IF)*	-	-	4BT	bits
t2	TXD sampled to MDI Output of 1st bit (100M Stream IF)	-	-	5	bits

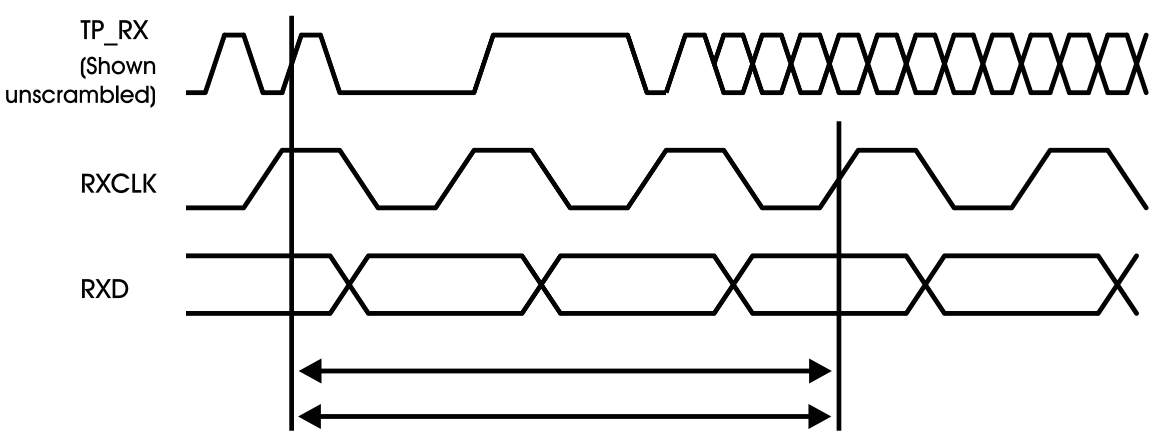
* Note that the IEEE maximum is 18 bits.

MII - CarrierAssertion/De-assertion on Transmission



T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	TXEN sampled to CRS assert	0	-	4	bits
t2	TXD sampled to CRS de-assert	0	-	4	bits

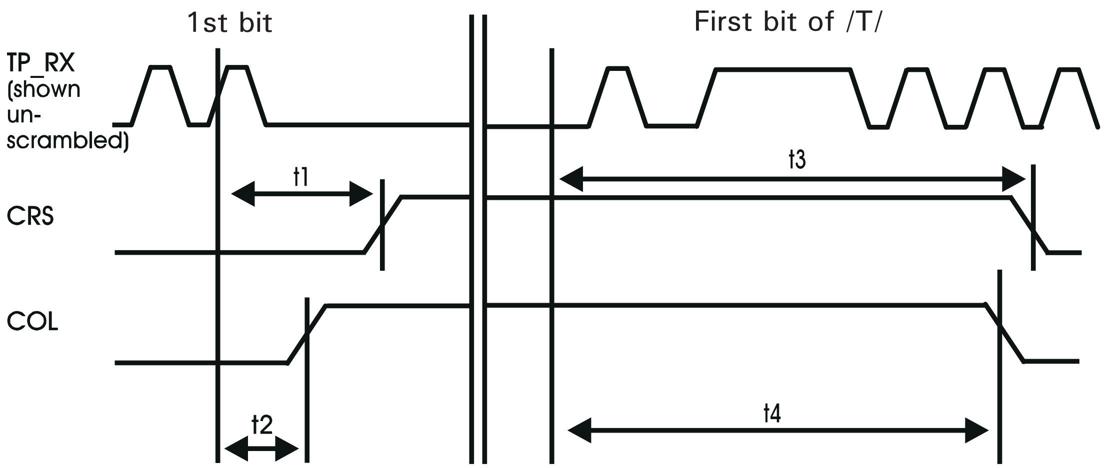
MII - Receive Latency (MII/100M Stream)



T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	1st bit of /J/ into TP_RX to /J/ on RXD (100M MII IF)	-	-	19BT	bits
t2	1st bit of /J/ into TP_RX to /J/ on RXD (100M Stream IF)	-	-	12.5	bits

* Note that the IEEE maximum is 23 bits.

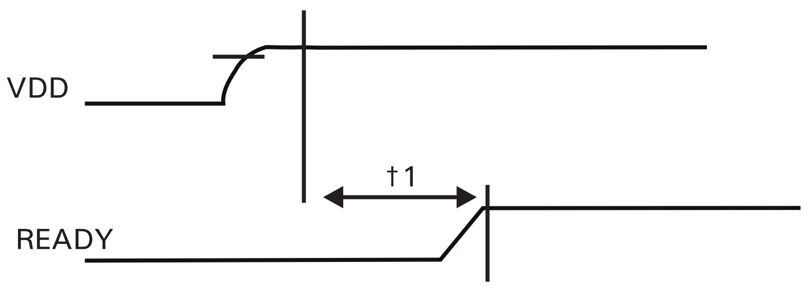
MDI Input to Carrier Assertion/De-assertion



T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	1st bit of /J/ into TP_RX to CRS assert*	-	-	124ns/13BT	bits
t2	1st bit of /J/ into TP_RX while transmitting data to COL assert (Half Duplex Mode)*	-	-	13	bits
t3	First bit of /T/ into TP_RX to CRS de-assert**	-	-	130ns/13BT	bits
t4	First bit of /T/ received into TP_RX to COL de-assert (Half Duplex Mode)**	-	-	14	bits

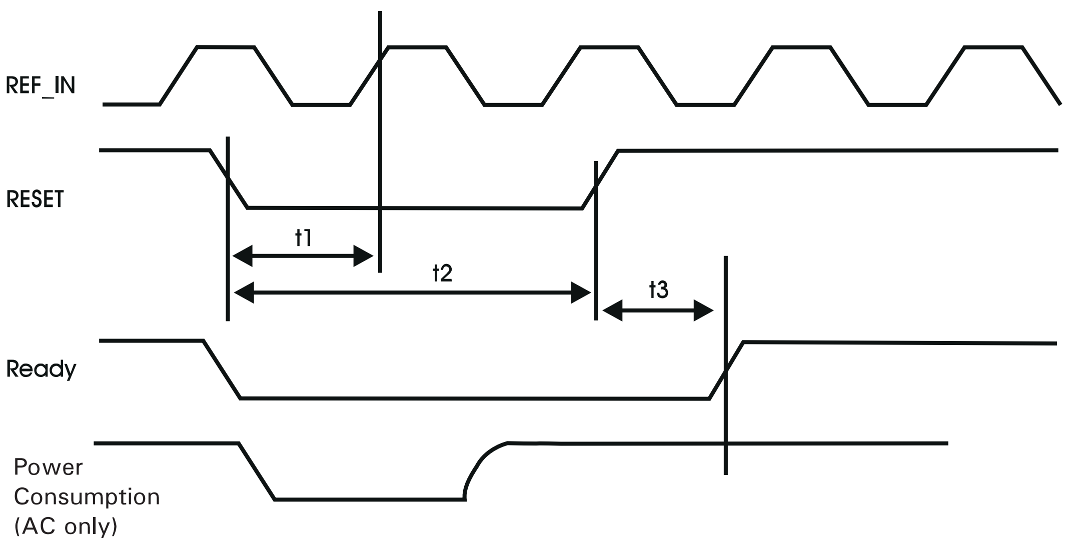
* Note that the IEEE maximum is 20 bit times.
** Note that the IEEE minimum is 13 bit times and the maximum is 24 bit times.

Reset - Power on Reset



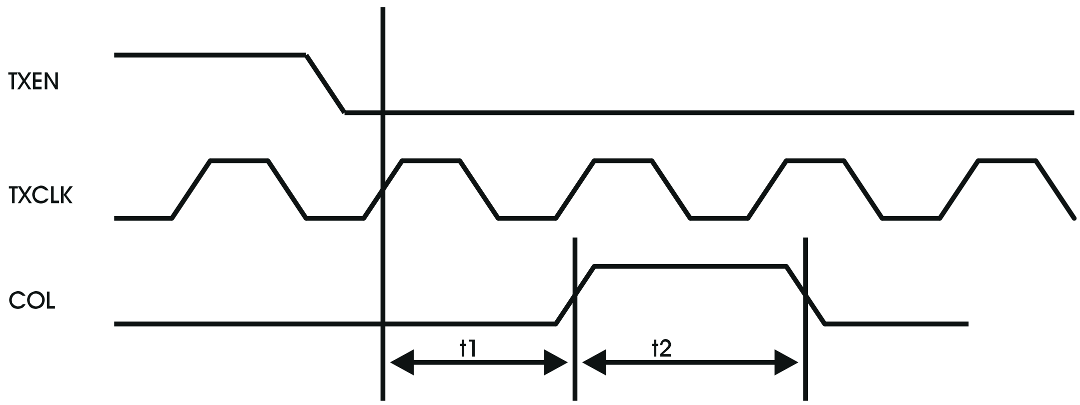
T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	VDD to 4.5V to Reset Complete	-	-	20	µs

Reset - Hardware Reset & Power-down



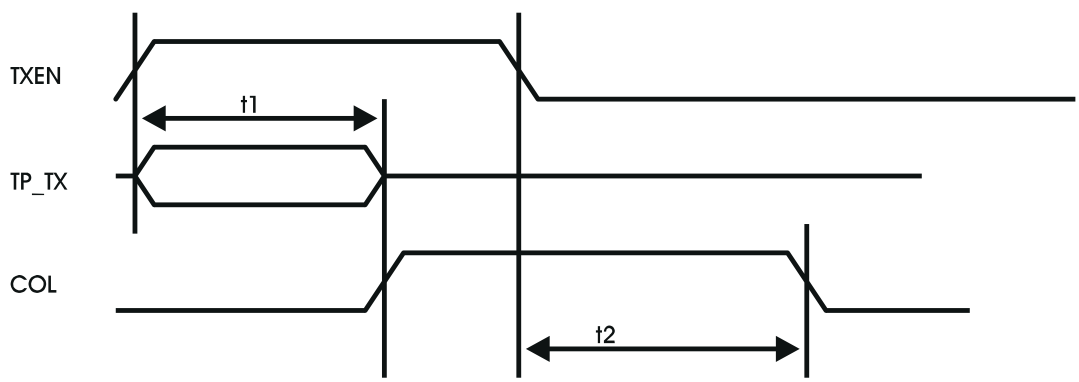
T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	RESET active to device isolation and initialization	-	-	200	ns
t2	Minimum RESET pulse width	80	-	-	ns
t3	RESET released to device ready	-	-	640	ns

10Base-T Heartbeat Timing



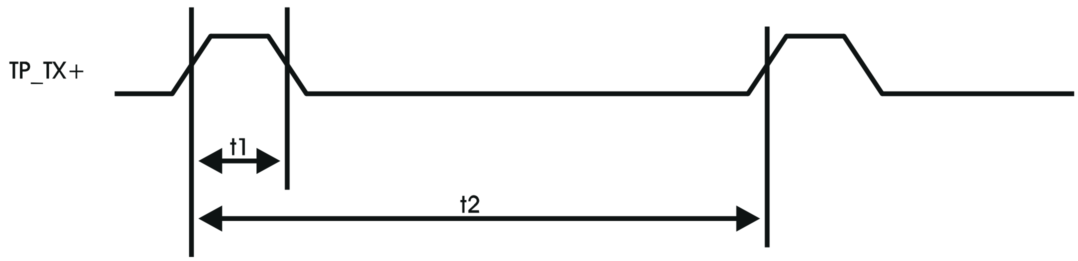
T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	COL Heartbeat assertion delay from TXEN de-assertion (10Base-T Half Duplex)	-	-	1210	ns
t2	COL Heartbeat assertion duration (10Base-T Half Duplex)	-	-	1170	ns

10Base-T Jabber Timing



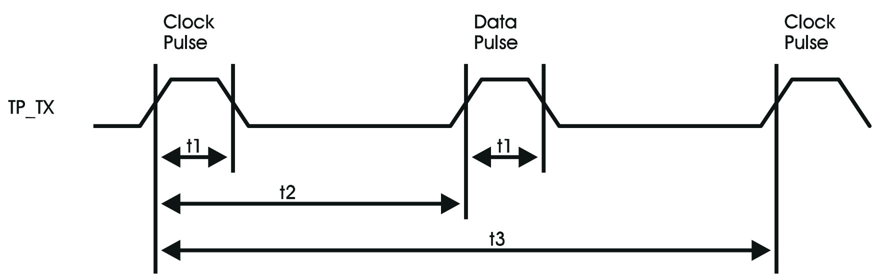
T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	Jabber activation time (10Base-T Half Duplex)	-	26	-	ms
t2	Jabber deactivation time (10Base-T Half Duplex)	-	410	-	ms

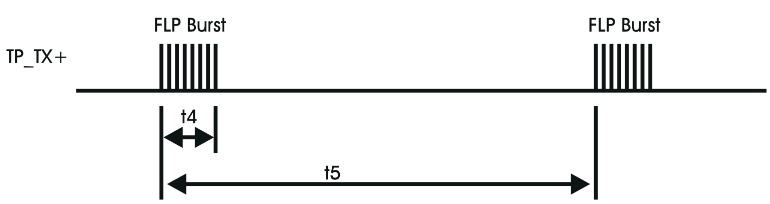
10Base-T Normal Link Pulse Timing



T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	Normal Link Pulse Width (10Base-T)	-	100	-	ns
t2	COL Heartbeat assertion duration (10Base-T Half Duplex)	8	-	24	ms

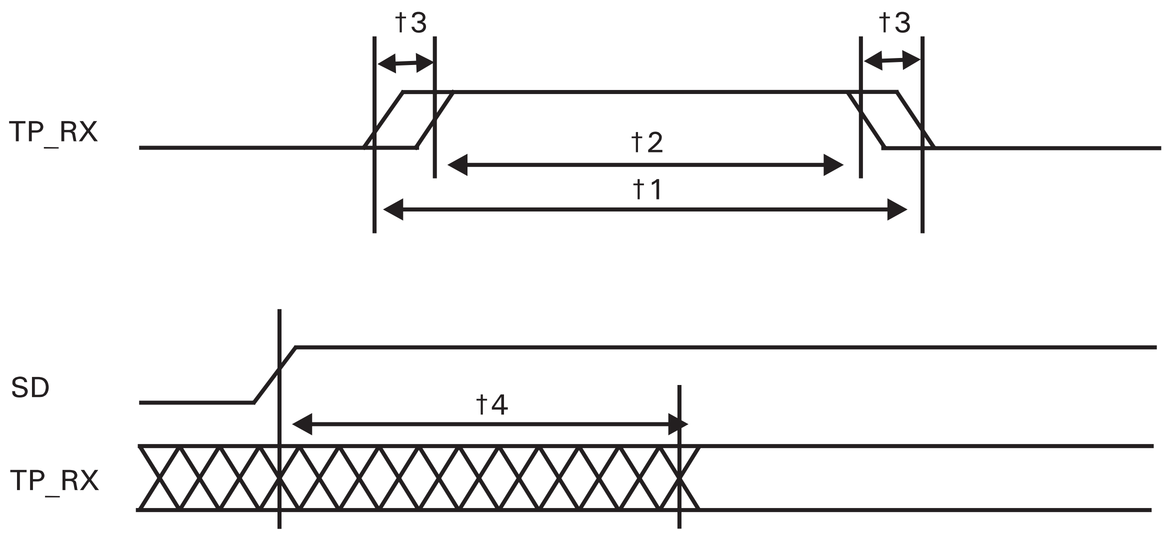
Auto-Negotiation Fast Link Pulse Timing



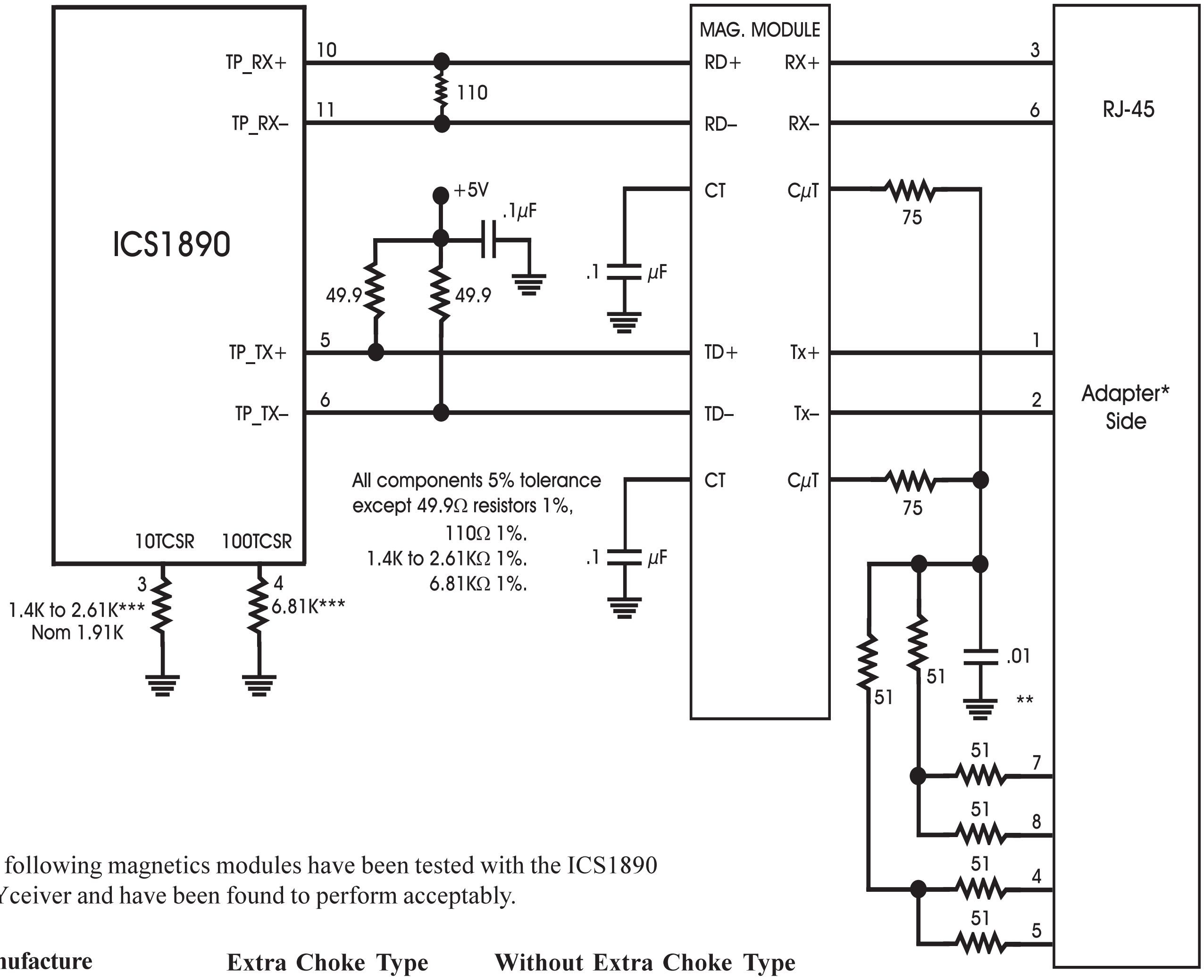


T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	Clock/Data pulse width	-	100	-	ns
t2	Clock pulse to Data pulse timing	55.5	62.5	69.5	µs
t3	Clock pulse to Clock pulse	111	125	139	µs
t4	FLP Burst width	-	2	-	ms
t5	FLP burst to FLP burst timing	8	16	24	ms
t6	Number of Clock/Data pulses in a burst	17	-	33	pulses

Clock Recovery



T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	Ideal data recovery window	-	-	8	ns
t2	Actual data recovery window	6	-	8	ns
t3	Data recovery window truncation	0	-	1	ns
t4	SD assert to data acquired	-	-	100	ns



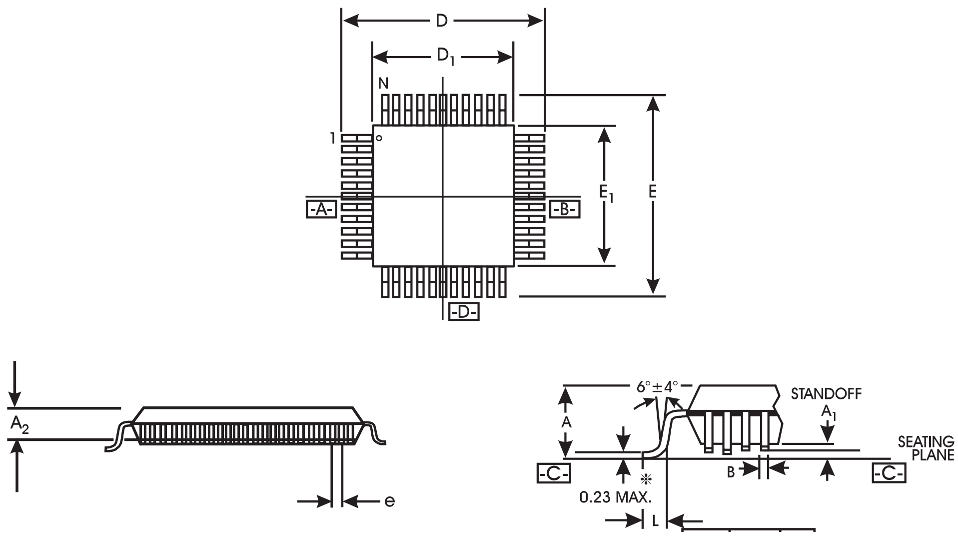
The following magnetics modules have been tested with the ICS1890 PHYceiver and have been found to perform acceptably.

Manufacture	Extra Choke Type	Without Extra Choke Type
Nano Pulse (NPI)	NP16120-30	NP16170-30
Pulse	PE-68517	PE-68515
Valor	ST6114	STG118
Bell Fuse	S558-5999-01	S558-5999-00
Halo	TG22-SO10ND	TG22-SO20ND
Innet	T0027S	T0019S
Unicom	2HT16-27	

* Repeaters and Hubs are generally responsible for including a cable crossover. One way of doing this is to exchange transmit (1 & 2) and receive (3 & 6) connections to the RJ-45.

** A minimum of 2KV capacitor should be used to make the connection to the chasis ground.

*** These are close starting values. These resistors need to be tailored to individual system insertion losses, these values can go as low as 1KΩ. Average 10TCSR value (pin 3) is 1.91KΩ.



TQFP/MQFP Package

DIMENSION NAME	LEAD COUNT (N) 64L			TQFP	MQFP
	BODY THICKNESS			1.4	2.7
	FOOTPRINT (BODY+) Nominal			2.0	3.20
	DIMENSIONS	TOLERANCE TQFP	TOLERANCE MQFP		
Full Package Height	A	MAX.	MAX.	1.60	3.00
Package Standoff	A_1	MAX.	MAX.	0.15	0.25
Package Thickness	A_2	±0.05	+0.10/-0.05	1.4	2.7
Tip-to-Tip Width	D	BASIC	±0.25	16.0	17.20
Body Width	D_1	BASIC	±0.10	14.0	14.00
Tip-to-Tip Width	E	BASIC	±0.25	16.0	17.20
Body Width	E1	BASIC	±0.10	14.0	14.00
Footlength	L	±0.15	+0.10/-0.10	0.60	0.88
Lead Pitch	e	BASIC	BASIC	0.80	0. 80
Lead Width w/Plate	B	+0.08/-0.05	+0.10/-0.05	0.37	0.35
Lead Height w/Plate	*	+0.04/-0.07	MAX.	0.16	0.23

Dimensions in millimeters.

Ordering Information

ICS1890Y

ICS1890Y-14

Example:

ICS XXXXY

Package Type
Y=MQFP Y-14=TQFP

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS,AV=Standard Device