High Performance DEC Alpha™ CPU Clock

Description

The **ICS1577** is a high performance monolithic phase locked loop (PLL) frequency synthesizer. Utilizing ICS's advanced CMOS mixed mode technology, the **ICS1577** provides a low cost solution for high-end DEC Alpha CPU clock generation.

The **ICS1577** has differential CPU clock outputs (CLK+ and CLK-) that are compatible with the DEC Alpha CPU operating up to 466 MHz. The differential output frequency on this version of the **ICS1577** is set to an exact multiple (28 times) of the crystal oscillator or reference frequency.

Features

- CLK operation to 466 MHz
- Operates from a single crystal or reference frequency
- User-programmable output voltage levels
- Independent PLL synthesizer and output driver power supply inputs - provides voltage isolation for improved high frequency operation
- Fully user-programmable version available - allows "on-the-fly" output frequency changes useful for 'power-down' modes or 'low power' applications. Contact factory for information.
- 100ps max cycle-to-cycle jitter
- Low power consumption CMOS technology
- 14-pin DIP package

Simplified Block Diagram - ICS1577

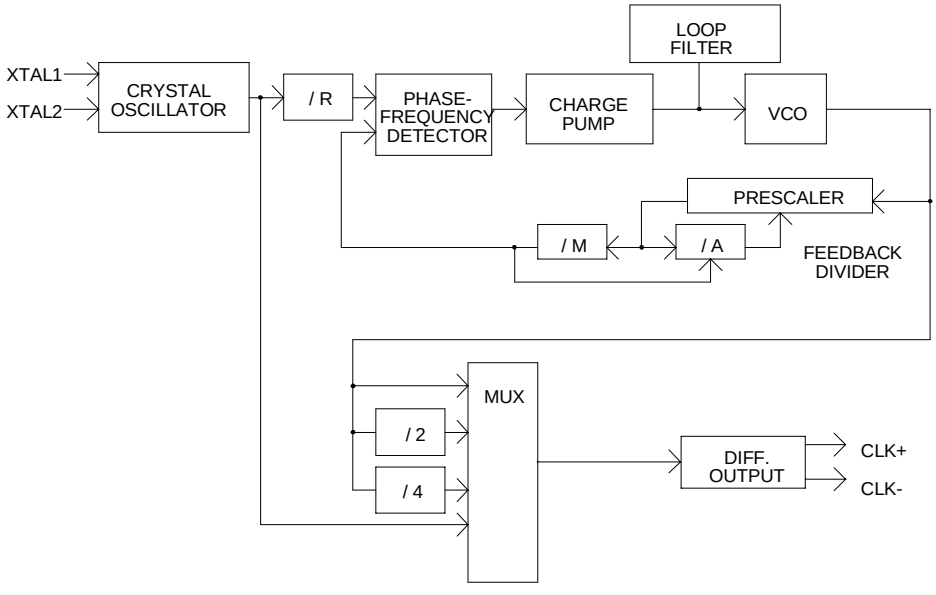
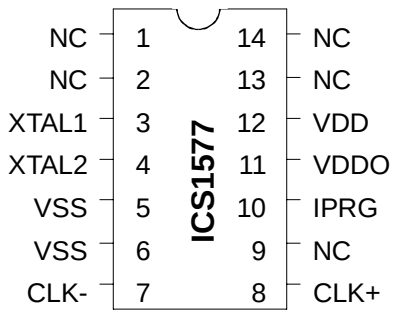


Figure 1



14-Pin DIP package

Alpha is a trademark of Digital Equipment Corporation.

Overview

The **ICS1577** is ideally suited to provide the CPU clock signals required by high-performance Alpha processors. The **ICS1577** provides up to a 466 MHz (Fxtal x 28) low jitter clock.

Output Description

The differential output drivers, CLK+ and CLK, are current-mode and are designed to drive resistive terminations in a complementary fashion. The outputs are current-sinking only, with the amount of sink current programmable via the IPRG pin. The sink current, which is steered to either CLK+ or CLK-, is approximately four times the current supplied to the **IPRG** pin. For most applications, a resistor from VDDO to IPRG will set the current to the necessary precision. See Figure 2 for output characteristics.

Reference Oscillator and Crystal Selection

The **ICS1577** has circuitry on-board to implement a Pierce oscillator with the addition of only one external component, a quartz crystal. Pierce oscillators operate the crystal in anti- (also called parallel-) resonant mode. See the AC Characteristics for the effective capacitive loading to specify when ordering crystals.

Series-resonant crystals may also be used with the **ICS1577**. Be aware that the oscillation frequency will be slightly higher than the frequency that is stamped on the can (typically 0.025-0.05%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. Avoid routing digital signals or the **ICS1577** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

If an external reference frequency source is to be used with the **ICS1577**, it is important that it be jitter-free. The rising and falling edges of that signal should be fast and free of noise for best results.

The loop phase is locked to the falling edges of the XTAL1 input signals.

Power-On Initialization

The **ICS1577** version has a fixed internal power-on reset circuit that performs the following function:

Sets the multiplexer to pass the VCO frequency (Fxtal x 28).

Power Supplies and Decoupling

The **ICS1577** has two VSS pins to reduce the effects of package inductance. Both pins are connected to the same potential on the die (the ground bus). BOTH of these pins should connect to the ground plane of the CPU board as close to the package as is possible.

The **ICS1577** has a VDDO pin which is the supply of +5 volt power to all output drivers. This pin should be connected to the power plane (or bus) using standard high-frequency decoupling practice. That is, capacitors should have low series inductance and be mounted close to the **ICS1577**.

The VDD pin is the power supply pin for the PLL synthesizer circuitry and other lower current digital functions. We recommend that RC decoupling or zener regulation be provided for this pin (as shown in the recommended application circuitry). This will allow the PLL to "track" through power supply fluctuations without visible effects. See Figure 3 for typical external circuitry.

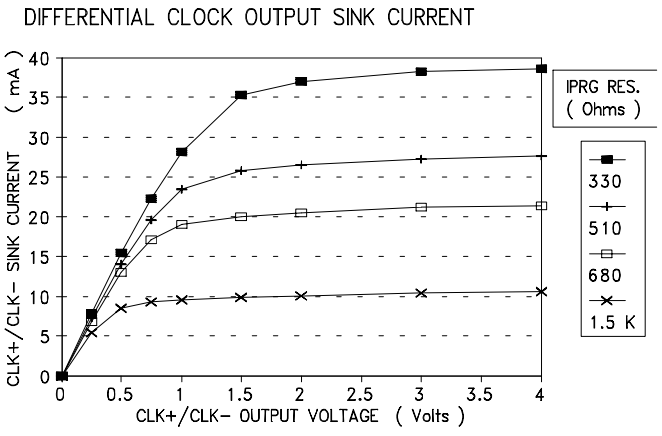


Figure 2

ICS1577 Typical Interface

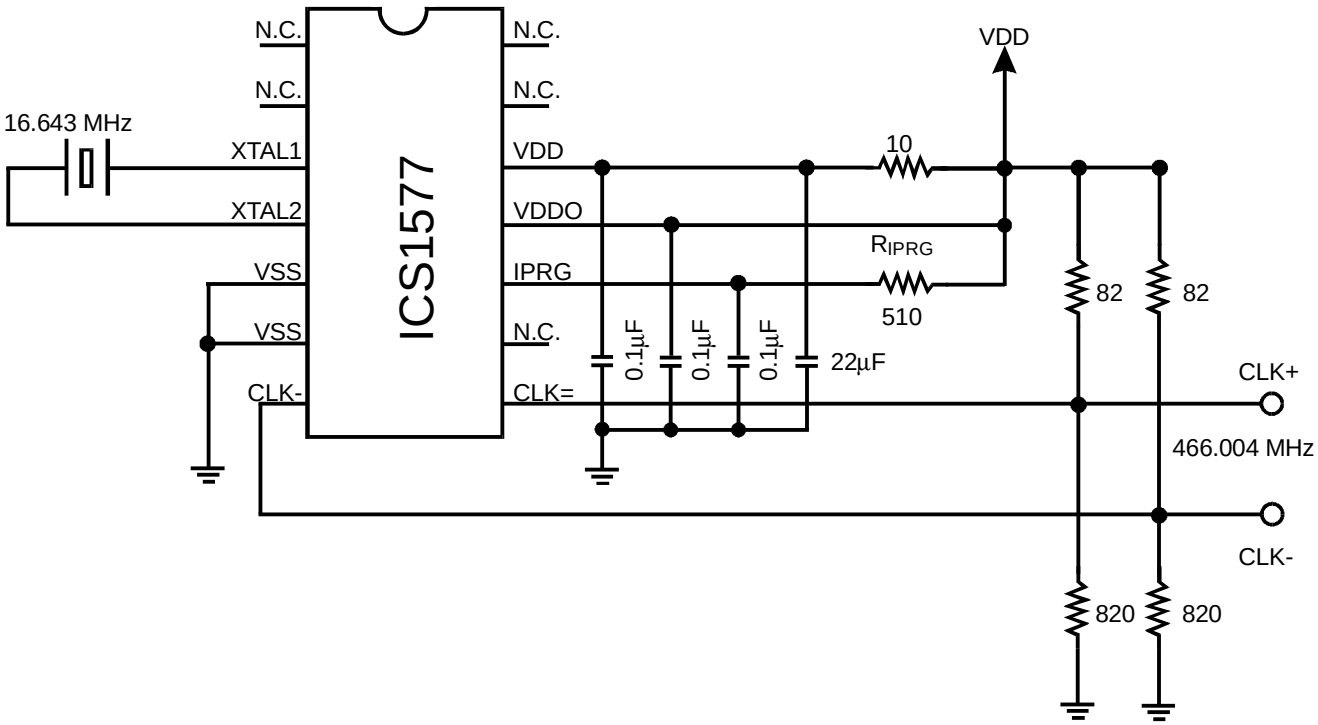


Figure 3

f_{XTAL}	f_{OUT}
11.786 MHz	330.000 MHz
14.318 MHz	400.904 MHz
16.643 MHz	466.004 MHz

Pin Description

PIN NUMBER	NAME	DESCRIPTION
3	XTAL1	Quartz crystal connection 1/external reference frequency input.
4	XTAL2	Quartz crystal connection 2/No connect for EXT REF.
5, 6	V_{SS}	Device Ground. Both pins must be connected.
7	CLK-	Clock Out (inverted).
8	CLK+	Clock Out.
10	IPRG	Output stage current/voltage set.
11	V_{DDO}	Output stage power (+5.0V).
12	V_{DD}	PLL system power (+5V. See application diagram.).
1, 2, 9, 13, 14	N.C.	No connection.

Absolute Maximum Ratings

VDD, VDDO (measured to V_{SS}) . . . . . 7.0 V
Digital Inputs . . . . . V_{SS}-0.5 to V_{DD} + 0.5 V
Digital Outputs . . . . . V_{SS}-0.5 to V_{DDO} + +0.5 V
Ambient Operating Temperature . . . . . -55 to 125°C
Storage Temperature . . . . . -65 to 150°C
Junction Temperature . . . . . 175°C
Soldering Temperature . . . . . 260°C

Recommended Operating Conditions

VDD, VDDO (measured to V_{SS}) . . . . . 4.75 to 5.25 V

Operating Temperature (Ambient) . . . . . 0 to 50°C

The **ICS1577** can be operated at 3.3V with reduced operating performance. Contact factory for information.

DC Characteristics

XTAL1 Input (External reference)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	V_{xh}		3.75	V_{DD}+0.5	V
Input Low Voltage	V_{xl}		V_{SS}-0.5	1.25	

CLK+, CLK- Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Differential Output Voltage			0.6	-	V

AC Characteristics @ 25°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
F_{vco}	VCO Frequency	140		500	MHz
F_{xtal}	Crystal Frequency	5		18	MHz
Cpar	Crystal Oscillator Loading Capacitance		20		pF
T_{xhi}	XTAL1 High Time (when driven externally)	8			ns
T_{xlo}	XTAL1 Low Time (when driven externally)	8			ns
T_{high}	Differential Clock Output Duty Cycle (see Note 1)	40		60	%
J_{clk}	Differential Clock Output Cumulative Jitter (see Note 2)		<.06	.075	VCO cycle
	Differential Clock Output Cumulative Jitter @ 466 MHz			375	ps peak to peak
J_p	Differential Clock Output Cycle-to-Cycle Jitter			100	ps peak to peak
T_{lock}	PLL Acquire Time (to within 1%)		500		µs
I_{dd}	VDD Supply Current (excluding external CLK+/– output termination), 466 MHz.			50	mA

Note 1: Using load circuit of Figure 3. Duty cycle measured at zero crossings of difference voltage between CLK+ and CLK-.

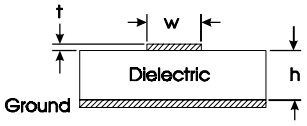
Note 2: Cumulative jitter is defined as the maximum error (in the domain) if any CLK edge, at any point in time, compared with the equivalent edge generated by an ideal frequency source.
ICS laboratory testing indicates that the typical value shown above can be treated as a maximum jitter specification in virtually all applications. Jitter performance can depend somewhat on circuit board layout, decoupling, and register programming.

Output Circuit Considerations for the ICS1577

Output Circuitry

The dot clock signals CLK and CLK- are typically the highest frequency signals present in the workstation. To minimize problems with EMI, crosstalk, and capacitive loading extra care should be taken in laying out this area of the PC board. The **ICS1577** is packaged in a 0.2"-wide 16-pin SOIC package. This permits the clock generator, crystal, and related components to be laid out in an area the size of a postage stamp. The **ICS1577** should be placed as close as possible to the CPU. The CLK and CLK- pins are running at VHF frequencies; one should minimize the length of PCB trace connecting them to the termination so that they don't become radiators of RF energy.

At the frequencies that the **ICS1577** is capable of, PC board traces may be long enough to be a significant portion of a wavelength of that frequency. PC traces for CLK and CLK- should be treated as transmission lines, not just interconnecting wires. These lines can take two forms: microstrip and stripline. A microstrip line is shown below:



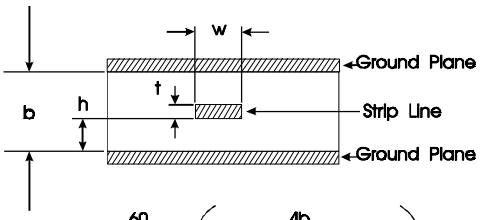
$$Z_o = \frac{87}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98h}{0.8w+t}\right)$$

Dimensions in inches

Microstrip Line

Essentially, the microstrip is a copper trace on a PCB over a ground plane. Typically, the dielectric is G10 glass epoxy. It differs from a standard PCB trace in that its width is calculated to have a characteristic impedance. To calculate the characteristic impedance of a microstrip line one must know the width and thickness of the trace, and the thickness and dielectric constant of the dielectric. For G10 glass epoxy, the dielectric constant (e_r) is about 5. Propagation delay is strictly a function of dielectric constant. For G10 propagation, delay is calculated to be 1.77 ns/ft.

Stripline is the other form a PCB transmission line can take. A buried trace between ground planes (or between a power plane and a ground plane) is common in multi-layer boards. Attempting to create a workstation design without the use of multi-layer boards would be adventurous to say the least, the issue would more likely be whether to place the interconnect on the surface or between layers. The between layer approach would work better from an EMI standpoint, but would be more difficult to lay out. A stripline is shown below:



$$Z_o = \frac{60}{\sqrt{e_r}} \ln\left(\frac{4b}{0.067\,\pi\, w\left(0.8 + \frac{t}{w}\right)}\right)$$

Dimensions in inches

Stripline

Using 1oz. copper (0.0015" thick) and 0.040" thickness G10, a 0.010" trace will exhibit a characteristic impedance of 75Ω in a stripline configuration.

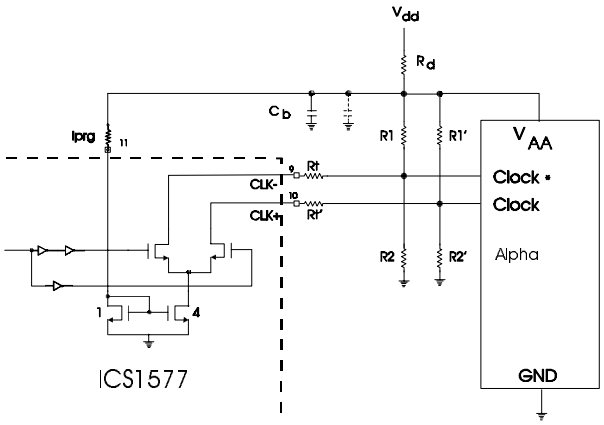
Output circuitry for the **ICS1577** is shown in the following diagram. It consists of a 4/1 current mirror, and two open drain output FETs along with inverting buffers to alternately enable each current-sinking driver. Both CLK and CLK- outputs are connected to the respective CLOCK and CLOCK* inputs of the termination with transmission lines and terminated in their equivalent impedances by the Thevenin equivalent impedances of R1 and R2 or R1' and R2'.

The **ICS1577** is incapable of sourcing current, so V_{ih} must be set by the ratios of these resistors for each of these lines. R1 and R2 are electrically in parallel from an AC standpoint because V_{dd} is bypassed to ground through bypass-capacitor network C_b. If we picked a target impedance of 75Ω for our transmission line impedance, a value of 91Ω for R1 and R1' and a value of 430Ω for R2 and R2' would yield a Thevinin equivalent characteristic impedance of 75.1W and a V_{ih} value of V_{AA}-.873 Volts, a margin of 0.127 Volts. This may be adequate; however, at higher frequencies one must contend with the input capacitance of the termination. Values of 82Ω for R1 and R1' and 820Ω for R2 and R2' would give us a characteristic impedance of 74.5Ω and a V_{ih} value of V_{AA}-.45. With a .55 Volt margin on Vih, this voltage level might be safer.

To set a value for V_{il}, we must determine a value for I_{prg} that will cause the output FET's to sink an appropriate current. We desire V_{il} to be V_{AA}-1.6 or greater. VAA-2 would seem to be a safe value. Setting up a sink current of 25 milliamperes would guarantee this through our 82Ω pull-up resistors. As this is controlled by a 4/1 current mirror, 7 mA into I_{prg} should set this current properly. A 510Ω resistor from V_{dd} to I_{prg} should work fine.

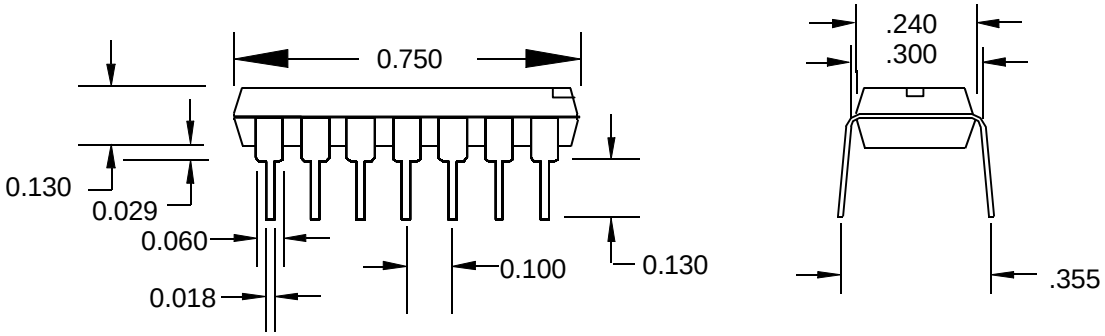
Resistors Rt and Rt' are shown as series terminating resistors at the **ICS1577** end of the transmission lines. These are not required for operation, but may be useful for meeting EMI requirements. Their intent is to interact with the input capacitance of the termination and the distributed capacitance of the transmission line to soften up rise and fall times and consequently cut some of the high-order harmonic content that is more likely to radiate RF energy. In actual usage they would most likely be 10 to 20Ω resistors or possibly ferrite beads.

Cb is shown as multiple capacitors. Typically, a 22 µF tantalum should be used with separate .1 µF and 220pF capacitors placed as close to the pins as possible. This provides low series inductance capacitors right at the source of high frequency energy. R_d is used to isolate the circuitry from external sources of noise. Five to ten ohms should be adequate.



ICS1577 Output Circuitry

Great care must be used when evaluating high frequency circuits to achieve meaningful results. The 10 pF input capacitance and long ground lead of an ordinary scope probe will make any measurements made with it meaningless. A low capacitance FET probe with a ground connection directly connected to the shield at the tip will be required. A 1 GHz bandwidth scope will be barely adequate, try to find a faster unit.



14-Pin DIP Package

Ordering Information

ICS1577N

Example:

ICS XXXX M

Package Type
N=DIP (Plastic)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

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