Output Considerations for the ICS1572

1 Introduction

The output considerations discussed in this application note apply to both the ICS1562A and the ICS1572. This application note includes a formula for calculating the trace width (w) that is needed to achieve the desired termination impedance (Z_0) for a circuit that uses either the ICS1562A or ICS1572.

Both the ICS1562A and ICS1572 use the same die. However, they have different pinouts and packages:

- The ICS1562A has a 0.15-inch 16-pin small-outline integrated circuit (SOIC) package.
- The ICS1572 has a 0.30-inch 20-pin SOIC package.

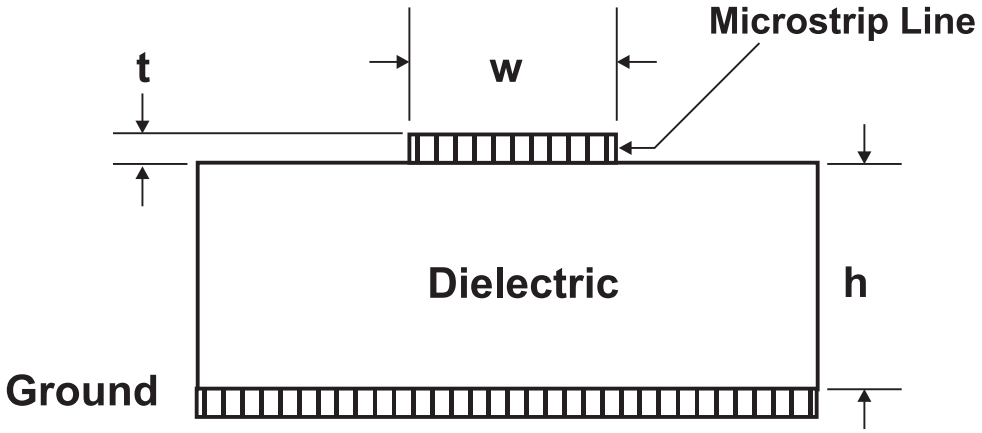
For a computer system, typically the ICS1562A / ICS1572 dot clock signals CLK+ and CLK– are the highest-frequency signals present. To minimize problems with electro-magnetic interference (EMI), crosstalk, and capacitive loading, use the following precautions when laying out the paths for these signals on a printed circuit board (PCB).

1. Place the ICS1562A / ICS1572 as close as possible to the destination device. That is, minimize the length of PCB traces that connect from the ICS1562A / ICS1572 CLK+ and CLK– pins to the corresponding destination device.[Signals from the CLK+ and CLK– pins run at very high frequencies (VHF). By minimizing the length of PCB traces that connect to these pins, these signals are less likely to radiate radio-frequency (RF) energy.]
2. Treat PCB traces for CLK+ and CLK– as if they are transmission lines and not just interconnecting wires. There are two possible types of traces to use:
   a. Microstrip line (discussed in Section 1.1, “PCB Transmission Line #1: Microstrip Line”)
   b. Stripline (discussed in Section 1.2, “PCB Transmission Line #2: Stripline”)

1.1 PCB Transmission Line #1: Microstrip Line

Figure 1 is a cross-section of a microstrip line, which is one of the forms of a PCB transmission line. A microstrip line is a PCB metal trace of width w, over a ground plane.

Figure 1. Microstrip Line



To calculate the required trace width, w, use the following equation:

$$w = \frac{7.463h}{\exp\left(\frac{Z_o \sqrt{0.475\,\varepsilon_r + 0.67}}{60}\right)} - 1.25t$$

To calculate the intrinsic propagation delay, T_d, use the following equation:

$$T_d = 33.36 \sqrt{0.475\,\varepsilon_r + 0.67} \quad \text{ps/cm}$$

Where:

- ε_r is the relative dielectric constant.
- h is the thickness of the dielectric layer.
- t is the thickness of the trace.
- Z_o is the required characteristic impedance of the microstrip line, in ohms.

Note:

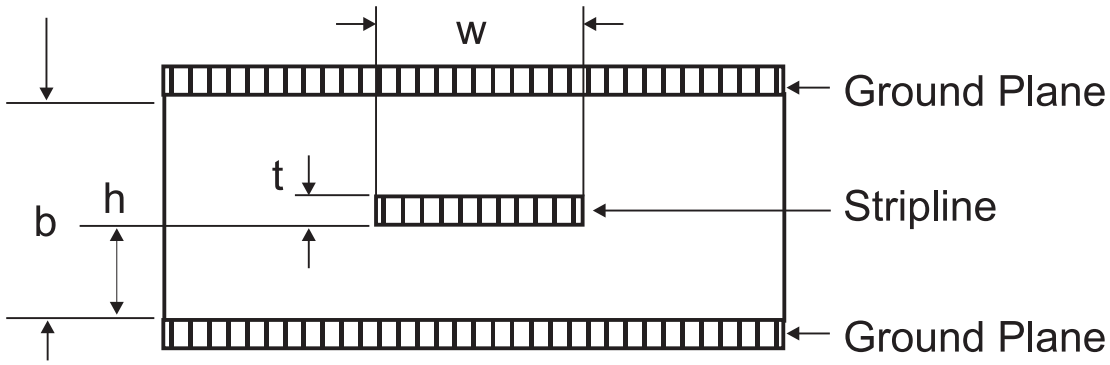
1. Dimensions w, h, and t must have the same units.
2. For FR4 glass epoxy, ε_r is 4.6.
3. If $w \leq 2h$, the maximum error is <3%.
4. Two commonly used copper plating standards are 1-ounce and 5-ounce. Their trace thickness (t) is as follows:
   a. For ‘1-ounce’ copper plating, t is 0.0036 cm.
   b. For ‘0.5-ounce’ copper plating, t is 0.0018 cm.

1.2 PCB Transmission Line #2: Stripline

A stripline, another form of PCB transmission line, is commonly used in multi-layer PCBs. A stripline is a trace that is buried either (1) between ground planes or (2) between a power plane and a ground plane. Given the choice of using standard PCB traces (that is, placing traces on the surface of a PCB) or using striplines to place traces in between layers, striplines work better from the standpoint of EMI, but are more difficult to lay out.

Figure 2 shows the type of stripline that is buried between ground planes.

Figure 2. Stripline (Buried between Ground Planes)



To calculate the required trace width, w, use the following equation:

$$w = \frac{2.375b}{\exp\left(\frac{Z_o\sqrt{\varepsilon_r}}{60}\right)} - 1.25t$$

To calculate the intrinsic propagation delay, T_d, use the following equation:

$$T_d = 33.36\sqrt{\varepsilon_r} \text{ ps/cm}$$

Where:

- b is the thickness of the dielectric layer between the ground planes.
- ε_r is the relative dielectric constant.
- t is the thickness of the trace.
- Z_o is the required characteristic impedance of the stripline, in ohms.

Note:

1. Dimensions w, h, and t must have the same units.
2. For FR4 glass epoxy, ε_r is 4.6.
3. If $w \leq 2h$, the maximum error is <3%.
4. Two commonly used copper plating standards are 1-ounce and 5-ounce. Their trace thickness (t) is as follows:
   a. For ‘1-ounce’ copper plating, t is 0.0036 cm.
   b. For ‘0.5-ounce’ copper plating, t is 0.0018 cm.

2 Output Circuitry

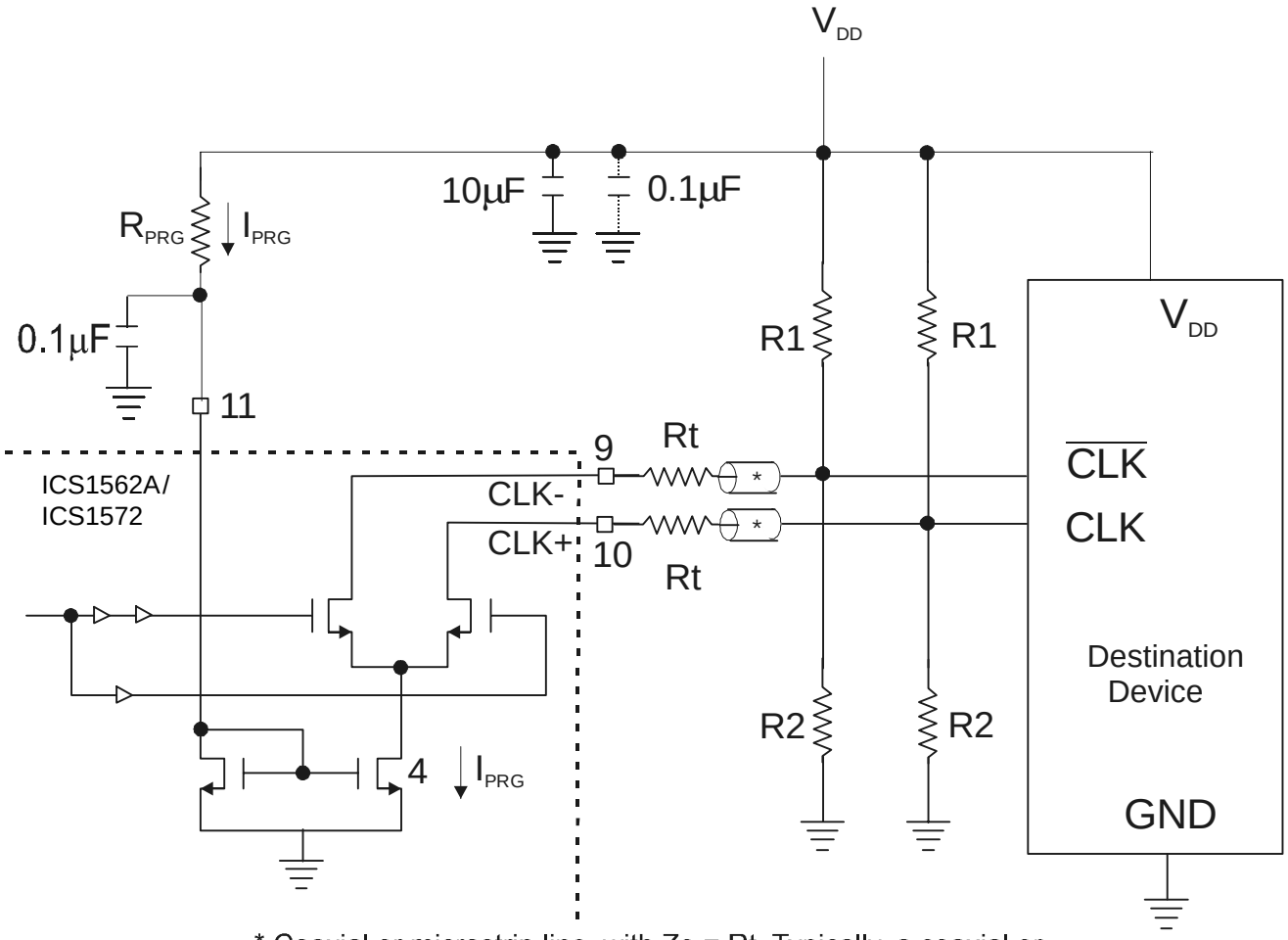
Figure 3 shows the output circuitry for the ICS1562A / ICS1572, both of which can drive a destination device. Both the ICS1562A / ICS1572 include the following:

- A 4/1 current mirror
- Two open-drain output field-effect transistors (FETs)
- Inverting buffers to alternately enable each current-sinking driver

In Figure 3, both the ICS1562A / ICS1572 CLK+ and CLK– outputs drive the corresponding CLK and $\overline{CLK}$ inputs of a destination device. Termination resistors R1 and R2 are placed as close as possible to the destination device. Ideally, the clock traces are close to each other and are routed directly to the ADC.

If the length of the clock traces exceeds 3 cm, use either microstrip (Section 1.1, “PCB Transmission Line #1: Microstrip Line”) or stripline (Section 1.2, “PCB Transmission Line #2: Stripline”). For a microstrip or stripline, Z_o, the characteristic impedance, equals the value of R1 and R2 in parallel.

Figure 3. ICS1562A / ICS1572 Output Circuitry



3 Selecting Component Values

To select component values for a circuit that uses either the ICS1562A or the ICS1572, refer to Figure 3 and use the following steps.

1. If desired, select Rt snubber resistors. A typical value for Rt is 10Ω.

   Snubber resistors are not essential. However, in combination with circuit stray capacitance, snubber resistors can partially attenuate higher harmonic components of the CLK+ and CLK– signals, thereby improving EMI performance.

2. Select Z_o, the termination impedance. A typical value for Z_o is between 50 and 100 Ω.

   If stripline or microstrip is to be used between the CLK+ and CLK– outputs and the termination, then Z_o is also the value of the characteristic impedance of the stripline or microstrip. For video applications, a typical value for Z_o is 75 Ω.

3. Select V_H and V_L, the high and low values of the input voltage to the destination device, as follows:
   a. See the data sheet for the destination device. The data sheet can provide the following values:
      (1) V_{IH}, the minimum value of the 'high' state input voltage
      (2) V_{IL}, the maximum value of the 'low' state input voltage
   b. For the V_{DD} value for the ICS1562A / ICS1572, select $V_{DD} > V_H > V_L$ and $V_{IL} > V_L > 0$. That is, select a high state voltage that is greater than V_{IH} and a low state voltage that is less than V_{IL}.

4. Calculate R1 as follows:

$$R1 = \frac{V_{DD}}{V_H} \times Z_o$$

5. Calculate R2 as follows:

$$R2 = \frac{(R1 \times Z_o)}{(R1 - Z_o)}$$

6. Calculate I_{PRG} as follows:

$$I_{PRG} \approx \frac{(V_H - V_L)}{4 \times Z_o}$$

7. Calculate R_{PRG} as follows:

$$R_{prg} \approx \frac{(V_{DD} - 1.4)}{I_{PRG}}$$