# Using SSTL-3 Outputs with CMOS or LVTTL Inputs

The ICS1523 has the following SSTL-3 outputs:

- LOCK/REF (pin 14)
- FUNC (pin 15)
- CLK/2 (pin 16)
- CLK (pin 17)

Per EIA/JESD8-8, SSTL-3 outputs are intended to provide a moderate voltage swing across a low-impedance load at the end of a transmission line. However, if an SSTL-3 output is connected directly to a destination LVTTL-compatible input, it can provide nearly rail-to-rail swings (that is, from 0 to 3.3 V). The equivalent source impedance of these outputs is typically 30 to 50Ω.

The FUNC and LOCK/REF signals are both at the input HSYNC frequency rate. As a result, if these signals are directly connected to a destination LVTTL-compatible input, typically this direct connection does not result in signal degradation.

The CLK and CLK/2 signals, in contrast to FUNC and LOCK/REF, are at much higher frequency rate. Due to internal design limitations, if the CLK and CLK/2 signals are directly connected to a destination LVTTL-compatible input, they exhibit frequency effects. For example, their waveforms can appear as though some shunt capacitance is present across the output load. For some applications (depending upon system requirements with respect to waveforms and delay), this equivalent RC effect can limit the highest frequency at which the SSTL-3 outputs can be used. For those applications, the designer can use the corresponding PECL outputs.

In general, for all high-frequency traces, ICS recommends traces less than 3 cm. (If there are long traces between CLK and CLK/2 outputs and their destination, there is additional shunt capacitance that can increase the total roundoff and delay. Long traces also increase the RF radiation at both the clock frequency and its harmonics.)