Line-Locked Applications Design Supplement

Line-Locked Applications

The term "Line-Locked" refers to **ICS1522** applications where one of the outputs of the **ICS1522** will be locked to some multiple of a reference frequency provided to it. A typical application of the **ICS1522** is generation of a sampling clock for an A/D converter that is digitizing the video output of a PC. Normally, this sampling clock should be of the same frequency as the clock which generated the video for best performance (fewest artifacts in the reproduction). Such a clock can be generated by the **ICS1522** by using the PC's HSYNC signal as the reference for the **ICS1522** and programming it to multiply that frequency.

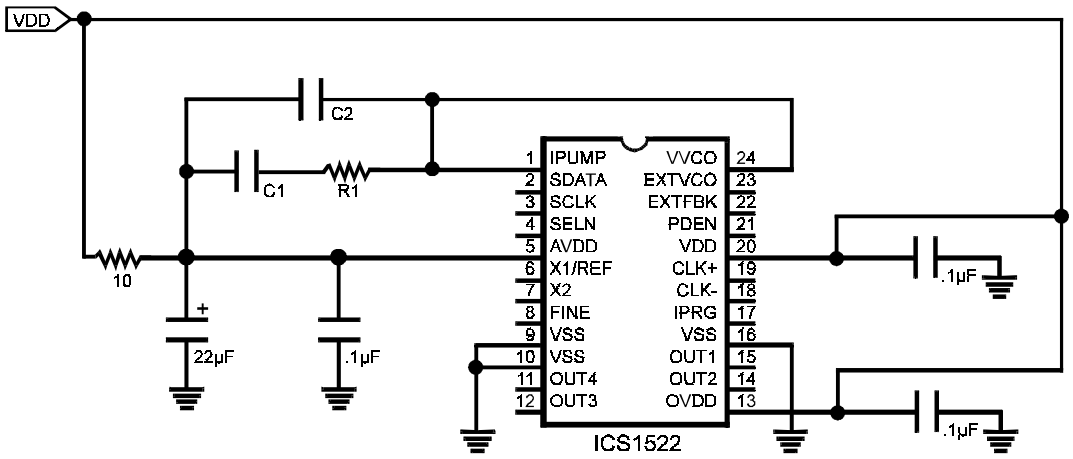
A step-by-step procedure for determining loop filter values and other programmable parameters follows.

Selection of External Components for Line-Locked Applications

ICS generally recommends use of an external loop filter with the **ICS1522** for line-locked applications. The fixed internal loop filter cannot achieve a good compromise over the full range of line-locked applications that the **ICS1522** can handle. Hence, the tuning of the filter values was skewed for normal clock synthesis (similar to ICS1562 "loop tuning"). Much better phase margin and loop damping will be achieved with an external loop filter. This document should help designers quickly arrive at the correct component values for the external loop filter and the correct programming of the device itself. Calculation for Section I is normally done once for a given application, calculation of Sections II & III should be done for all expected cases (or the calculation should be imbedded within the application firmware).

ICS1522 External Loop Filter

Recommended Power Distribution and Filter Configuration



Possible External Component Values:	Approx. Internal Component Values:
R1=51k	R1=120k
C1=.01µF	C1=110pF
C2=.001µF	C2=11pF
(Reg. 4, Bit 7=0)	(Reg. 4, Bit 7=1)

PFD & VCO Gains, In addition to the External Loop Filter values, might require adjustment to achieve the desired PLL performance.

I. Calculation of External Loop Filter Component Values

Enter the **lowest** reference frequency that will be used in the application (usually 15 kHz for TV, 31.5 kHz for VGA):

$F_{reference}$ =15 kHz

We next set the modulus of the Reference Divider. This should always be set to one for a line-locked application:

$N_{reference}$ =1

Select the phase detector gain to be used. We recommend that the higher gain settings be used to minimize the resulting impedances of the loop filter components. Normally, set:

PFD_Gain_Setting=6

From the data sheet, we enter the actual value at a setting of 6 into a variable:

$$Gain_{PFD} = \frac{30\mu A}{2\pi rad}$$

We next calculate the value of the resistor in the loop filter as a function of that gain. A good compromise is obtained when:

$$R = \frac{0.33\ volt}{Gain_{PFD}} \qquad R = 69.115k\Omega$$

... we substitute the nearest 5% value:

R=68KΩ

The value of the capacitor in series with the resistor sets the damping of the loop. Again, a good compromise will be achieved when:

$$C_1 = \frac{50}{2\pi F_{reference} R} \qquad C_1 = 7.802nF$$

... we substitute the nearest 10% value.

C_1=8.2nF

Next, we calculate the value of the capacitor connected in parallel with the series R & C_1 combination:

$$C_2 = \frac{C_1}{100} \qquad C_2 = 82pF$$

This capacitor gives improved high-frequency noise rejection, but is not necessary for loop stability.

II. Calculation of Divider Parameters within the ICS1522

As stated above, the Reference Divider modulus will be set to divided-by-1 in a line-locked application. The Feedback Divider Post-Scaler is also normally set to divide-by-1. The selection of the input source for the Feedback Divider will normally also be set to OUT1. When these options have been set, the phase of one of the OUT1 edges will be aligned with the reference clock. This is normally what is desired. This allows for correct alignment of the pixel boundaries in multiple-byte-per-pixel applications, such as true-color. It also allows for proper alignment of multi-byte interface RAMDAC™s in line-locked applications, (i.e., the RAMDAC LOAD clock will be consistently aligned with the reference clock).

Next, the Feedback Divider Modulus, LOAD Counter/Divider Modulus (or the modulus of the Divide-by-4, if used instead), Output Post Scaler, and VCO Gain must be selected. First, determine if the line-locked clock frequency is to be taken from the differential CLK outputs of the **ICS1522**, or the OUT1 pin of the **ICS1522**.

II(a). Line-Locked Output Taken from CLK Outputs

If the output is to be taken from the differential CLK outputs, the product of the LOAD Divider Modulus, Feedback Divider Modulus, and Feedback Post-Scaler (=1) must be set equal to the desired number of cycles of the CLK output per reference period. For this example, we assume that 1000 CLK cycles per reference clock is desired, and the RAMDAC used requires the LOAD Counter/Divider Modulus to be 8.

First, we set the modulus of the feedback divider post scaler:

$N_{feedback\_post\_scaler}$ =1

Then, we set the number of clocks desired per reference period

$N_{clocks\_per\_reference}$ =1000

Next, we set the modulus of the LOAD Counter/Divider (or the modulus of the separate multi-phase divide-by-4, if used):

N_{LOAD} =8

We calculate the required modulus of the feedback divider as:

$$N_{feedback} = \frac{N_{clocks\_per\_reference}}{N_{LOAD} N_{feedback\_post\_scaler}} \qquad N_{feedback} = 125$$

The frequency of the CLK output will then be the product of those dividers times the reference frequency:

$$F_{CLK} = F_{reference} N_{feedback} N_{feedback\_post\_scaler} N_{LOAD}$$

$$F_{CLK} = 15 \text{ MHz}$$

That frequency is relatively low for the VCO. We recommend that the VCO be operated at the highest frequency within its range. Therefore, we will set the Output Post-Scaler to divide-by-8.

$$N_{output\_post\_scaler} = 8$$

The VCO frequency can then be calculated:

$$F_{vco} = F_{CLK} N_{output\_post\_scaler} \qquad F_{vco} = 120 \text{ MHz}$$

... which is within the VCO maximum frequency limit.

II(b). Line-Locked Output Taken from OUT1 output.

Once again:

$$N_{feedback\_post\_scaler} = 1$$

If the pixel clock is to be taken from the OUT1 output, the product of the Feedback Divider and Feedback Post-Scaler (=1) must be equal to the desired number of OUT1 clocks per line. Suppose that we want 800 OUT1 cycles per reference clock. We simply then set the Feedback Divider Modulus to be:

$$N_{feedback} = 800$$

Perhaps we would like the frequency of the CLK outputs to be three times the OUT1 frequency (as in a true-color, three-bytes per pixel, application). We would set the LOAD Counter/ Divider Modulus:

$$N_{LOAD} = 3$$

and then the frequency of the CLK outputs will be ...

$$F_{CLK} = F_{reference} N_{feedback} N_{feedback\_post\_scaler} N_{LOAD}$$

$$F_{CLK} = 36 \text{ MHz}$$

Once again, that frequency is relatively low for the VCO. Therefore, we will set the Output Post-Scaler to divide-by-4.

$$N_{output\_post\_scaler} = 4$$

The VCO frequency (for this case) will be:

$$F_{vco} = F_{CLK} N_{output\_post\_scaler} \qquad F_{vco} = 144 \text{ MHz}$$

III. Calculation of VCO Gain Required:

We establish the minimum VCO gain needed as the following function of the VCO frequency (using the Fvco calculation of II(b). above):

$$gain_{vco\_minimum} = \frac{F_{vco}}{3.5 \text{ volt}} \qquad gain_{vco\_minimum} = 41.143 \frac{\text{MHz}}{\text{volt}}$$

From the data sheet we see that a VCO gain of 4 is the lowest setting that will meet the requirement, and we set the programming value:

VCO_Gain_Setting=4

We also make a variable that contains that VCO gain value:

$$Gain_{vco} = \frac{45 \text{ MHz}}{\text{volt}}$$

IV. Programming Summary

We now have all of the information that we need to program the **ICS1522**. Summarizing all of the above calculations and using the example shown in IIb above:

$N_{feedback}$=800

$N_{reference}$=1

VCO_Gain_Setting=4

PFD_Gain_Setting=6

We convert the modulus of the Output Post-Scaler, Feedback Post-Scaler, and LOAD Divider/Counter to programming of the PDA, PDB, and L bits respectively by looking it up from the data sheet:

$N_{output\_post\_scaler}$ =4	--- >	PDA =1
$N_{feedback\_post\_scaler}$ =1	--- >	PDB =8
N_{LOAD} =3	--- >	L =0

Other parameters that must be set are (some of these will vary depending on the specifics of the application):

LO =0	< --- sets phase of auxiliary (LO) feedback divider output
HI =0	< --- sets phase of auxiliary (HI) feedback divider output
REF_POL =1	< --- “O” for positive edge locking, “1” for negative edge
PDEN =1	< --- “0” to disable PLL locking, “1” to enable it
INT_FLT =0	< --- selects external loop filter
INT_VCO =1	< --- “0” to substitute external VCO, “1” for internal VCO
CLK_SEL =1	< --- “0” for locking CLK to reference, “1” for locking OUT1 to reference
FBK_SEL =1	< --- “0” for external feedback, “1” for internal feedback
FBK_POL =0	< --- “0” for locking to reference positive edge; “1” for internal feedback
ADD =0	< --- toggle “0” to “1” to “0” to add increment
SWLW =0	< --- “0” for external feedback, “1” for internal feedback
LD_LG =0	< --- “0” causes reference to lag feedback, “1” causes reference to lead feedback when Fine Phase Adjust is enabled
F_EN =0	< --- “0” disables, “1” enables Fine Phase Adjust
OMUX1 =0	< --- “0” for LOAD Divider/ Counter, “1” for multi-phase divide-by-four (0° phase)
OMUX2 =0	< --- “0” for output of internal feedback divider chain, “1” for multi-phase divide-by-four (90° phase)
OMUX3 =0	< --- “0” for feedback sync pulse LO, “1” for multi-phase divide-by-four (180° phase)
OMUX4 =0	< --- “0” for feedback sync pulse HI, “1” for multi-phase divide-by-four (270° phase)
DACRST =0	< --- “0” for normal operation, “1” to reset pipeline delay of Brooktree RAMDACs
AUXEN =0	< --- “0” for normal operation, “1” for output test mode
AUXCLK =0	< --- selects level on CLK outputs when AUXEN =“1”
EXTREF =1	< --- “0” for crystal oscillator, “1” for external reference
RESERVED =1	

V. Calculate Register Values

$R_0 = N_{feedback} - 1$

$R_1 = LO$

$R_2 = HI$

$R_3 = (N_{reference} - 1) + REF\_POL\ 2^{10}$

$R_4 = (VCO\_Gain\_Setting\ 2^{0}) + (PFD\_Gain\_Setting\ 2^{3}) + (PDEN\ 2^{6}) \ldots$
$+ (INT\_FLT\ 2^{7}) + (INT\_VCO\ 2^{8}) + (CLK\_SEL\ 2^{9}) \ldots$
$+ (RESERVED\ 2^{10})$

$R_5 = FBK\_SEL + (FBK\_POL\ 2^{1}) + (ADD\ 2^{2}) + (SWLW\ 2^{3}) + (PDA\ 2^{4}) \ldots$
$+ (PDB\ 2^{6}) + (LD\_LG\ 2^{8}) + (F\_EN\ 2^{9}) + (RESERVED\ 2^{10})$

$R_6 = (L\ 2^{0}) + (OMUX1\ 2^{3}) + (OMUX2\ 2^{4}) + (OMUX3\ 2^{5}) + (OMUX4\ 2^{6}) \ldots$
$+ (DACRST\ 2^{7}) + (AUXEN\ 2^{8}) + (AUXCLK\ 2^{9}) + (EXTREF\ 2^{10})$

With the above values:

$R_0 = 799$	or:	$R_0 = 31fh$
$R_1 = 0$	or:	$R_1 = 1$
$R_2 = 0$	or:	$R_2 = 0$
$R_3 = 1024$	or:	$R_3 = 400h$
$R_4 = 1908$	or:	$R_4 = 774h$
$R_5 = 1553$	or:	$R_5 = 611h$
$R_6 = 1024$	or:	$R_6 = 400h$