Integrated Circuit Systems, Inc.

# ICS8705I
## ZERO DELAY DIFFERENTIAL-TO-LVCMOS CLOCK GENERATOR

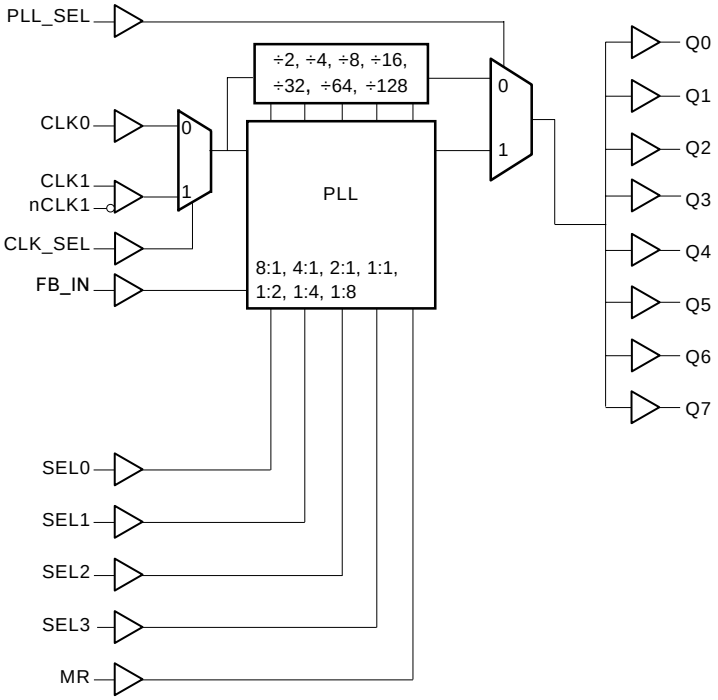
## GENERAL DESCRIPTION

The ICS8705I is a highly versatile 1:8 Differential-to-LVCMOS clock generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8705I has two selectable clock inputs. The CLK1, nCLK1 pair can accept most standard differential input levels. The single ended CLK0 input accepts LVCMOS or LVTTL input levels.The ICS8705I has a fully integrated PLL and can be configured as zero delay buffer, multiplier or divider and has an input and output frequency range of 15.625MHz to 275MHz. The reference divider, feedback divider and output divider are each programmable, thereby allowing for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8. The external feedback allows the device to achieve "zero delay" between the input clock and the output clocks. The PLL_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output dividers.

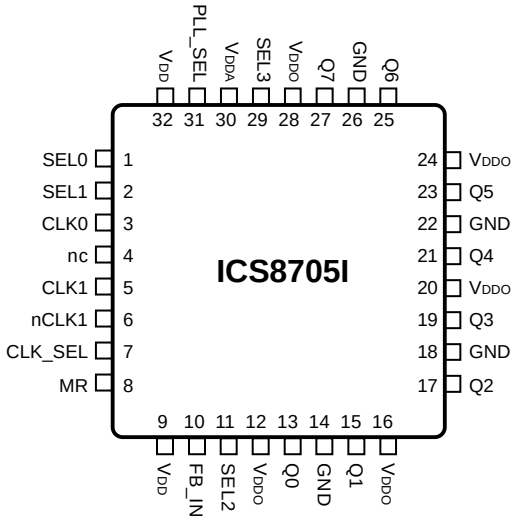
## FEATURES

- 8 LVCMOS outputs, 7Ω typical output impedance
- Selectable CLK1, nCLK1 or LVCMOS clock inputs
- CLK1, nCLK1 pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- CLK0 input accepts LVCMOS or LVTTL input levels
- Output frequency range: 15.625MHz - 275MHz
- Input frequency range: 15.625MHz - 275MHz
- VCO range: 250MHz - 550MHz
- External feedback for "zero delay" clock regeneration with configurable frequencies
- Programmable dividers allow for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8
- Fully integrated PLL
- Cycle-to-cycle jitter: 45ps (maximum)
- Output skew: CLK0, 65ps (maximum)
  CLK1, nCLK1, 55ps (maximum)
- Static Phase Offset: 25 ±125ps (maximum), CLK0
- Full 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature

## BLOCK DIAGRAM




## PIN ASSIGNMENT




**32-Lead LQFP**
7mm x 7mm x 1.4 mm
**Y Package**
Top View

**TABLE 1. PIN DESCRIPTIONS**

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1, 2 | SEL0, SEL1 | Input | Pulldown | Determines output divider values in Table 3. LVCMOS interface levels. |
| 3 | CLK0 | Input | Pulldown | Non-inverting LVCMOS clock input. |
| 4 | nc | | | No connect. |
| 5 | CLK1 | Input | Pulldown | Non-inverting differential clock input. |
| 6 | nCLK1 | Input | Pullup | Inverting differential clock input. |
| 7 | CLK_SEL | Input | Pulldown | Clock select input. When HIGH, selects differential CLK1, nCLK1. When LOW, selects LVCMOS CLK0. LVCMOS / LVTTL interface levels. |
| 8 | MR | Input | Pulldown | Master reset. Resets the output dividers. LVCMOS interface levels. |
| 9, 32 | $V_{DD}$ | Power | | Positive supply pins. Connect to 3.3V or 2.5V |
| 10 | FB_IN | Input | Pulldown | LVCMOS feedback input to phase detector for regenerating clocks with "zero delay". LVCMOS interface levels. |
| 11 | SEL2 | Input | Pulldown | Determines output divider values in Table 3. LVCMOS interface levels |
| 12, 16, 20, 24, 28 | $V_{DDO}$ | Power | | Output supply pins. Connect to 3.3V or 2.5V. |
| 13, 15, 17, 19, 21, 23, 25, 27 | Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7 | Output | | Clock output. 7Ω typical output impedance. LVCMOS interface levels. |
| 14, 18, 22, 26 | GND | Power | | Power supply ground. |
| 29 | SEL3 | Input | Pulldown | Determines output divider values in Table 3. LVCMOS interface levels |
| 30 | $V_{DDA}$ | Power | | Analog supply pin. Connect to 3.3V or 2.5V. |
| 31 | PLL_SEL | Input | Pullup | Selects between the PLL and reference clock as input to the dividers. When LOW, selects the reference clock (PLL Bypass). When HIGH, selects PLL (PLL Enabled). LVCMOS interface levels. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | | 4 | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | KΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | KΩ |
| $C_{PD}$ | Power Dissipation Capacitance (per output) | $V_{DD}$, $V_{DDO}$, $V_{DDA}$ = 3.465V | | | | pF |
| $R_{OUT}$ | Output Impedance | | | 7 | | Ω |

**TABLE 3A. PLL ENABLE FUNCTION TABLE**

| Inputs | | | | | Outputs PLL_SEL = 1 PLL Enable Mode |
|---|---|---|---|---|---|
| SEL3 | SEL2 | SEL1 | SEL0 | Reference Frequency Range (MHz) | Q0:Q7 |
| 0 | 0 | 0 | 0 | 125 - 275 | ÷ 1 |
| 0 | 0 | 0 | 1 | 62.5 - 137.5 | ÷ 1 |
| 0 | 0 | 1 | 0 | 31.25 - 68.75 | ÷ 1 |
| 0 | 0 | 1 | 1 | 15.625 - 34.375 | ÷ 1 |
| 0 | 1 | 0 | 0 | 125 - 275 | ÷ 2 |
| 0 | 1 | 0 | 1 | 62.5 - 137.5 | ÷ 2 |
| 0 | 1 | 1 | 0 | 31.25 - 68.75 | ÷ 2 |
| 0 | 1 | 1 | 1 | 125 - 275 | ÷ 4 |
| 1 | 0 | 0 | 0 | 62.5 - 137.5 | ÷ 4 |
| 1 | 0 | 0 | 1 | 125 - 275 | ÷ 8 |
| 1 | 0 | 1 | 0 | 62.5 - 137.5 | x 2 |
| 1 | 0 | 1 | 1 | 31.25 - 68.75 | x 2 |
| 1 | 1 | 0 | 0 | 15.625 - 34.375 | x 2 |
| 1 | 1 | 0 | 1 | 31.25 - 68.75 | x 4 |
| 1 | 1 | 1 | 0 | 15.625 - 34.375 | x 4 |
| 1 | 1 | 1 | 1 | 15.625 - 34.375 | x 8 |

**TABLE 3B. PLL BYPASS FUNCTION TABLE**

| Inputs | | | | Outputs PLL_SEL = 0 PLL Bypass Mode |
|---|---|---|---|---|
| SEL3 | SEL2 | SEL1 | SEL0 | Q0:Q7 |
| 0 | 0 | 0 | 0 | ÷ 8 |
| 0 | 0 | 0 | 1 | ÷ 8 |
| 0 | 0 | 1 | 0 | ÷ 8 |
| 0 | 0 | 1 | 1 | ÷ 16 |
| 0 | 1 | 0 | 0 | ÷ 16 |
| 0 | 1 | 0 | 1 | ÷ 16 |
| 0 | 1 | 1 | 0 | ÷ 32 |
| 0 | 1 | 1 | 1 | ÷ 32 |
| 1 | 0 | 0 | 0 | ÷ 64 |
| 1 | 0 | 0 | 1 | ÷ 128 |
| 1 | 0 | 1 | 0 | ÷ 4 |
| 1 | 0 | 1 | 1 | ÷ 4 |
| 1 | 1 | 0 | 0 | ÷ 8 |
| 1 | 1 | 0 | 1 | ÷ 2 |
| 1 | 1 | 1 | 0 | ÷ 4 |
| 1 | 1 | 1 | 1 | ÷ 2 |

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, $V_{DDx}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{DD}$+0.5 V |
| Outputs, $V_O$ | -0.5V to $V_{DDO}$+0.5V |
| Package Thermal Impedance, $\theta_{JA}$ | 47.9°C/W (0 lfpm) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,** $V_{DD} = V_{DDA} = V_{DDO}$ = 3.3V±5%, TA = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Input Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDA}$ | Analog Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDO}$ | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{DD}$ | Input Supply Current | | | | 90 | mA |
| $I_{DDA}$ | Analog Supply Current | | | | 15 | mA |
| $I_{DDO}$ | Output Supply Current | | | | 20 | mA |

**TABLE 4B. LVCMOS / LVTTLE DC CHARACTERISTICS,** $V_{DD} = V_{DDA} = V_{DDO}$ = 3.3V±5%, TA = -40°C TO 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | PLL_SEL, CLK_SEL, SEL0, SEL1, SEL2, SEL3, FB_IN, MR | | 2 | | $V_{DD}$ + 0.3 | V |
| | | CLK0 | | 2 | | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | PLL_SEL, CLK_SEL, SEL0, SEL1, SEL2, SEL3, FB_IN, MR | | -0.3 | | 0.8 | V |
| | | CLK0 | | -0.3 | | 1.3 | V |
| $I_{IH}$ | Input High Current | CLK0, CLK_SEL MR, FB_IN, SEL0, SEL1, SEL2, SEL3 | $V_{DD} = V_{IN}$ = 3.465V | | | 150 | µA |
| | | PLL_SEL | $V_{DD} = V_{IN}$ = 3.465V | | | 5 | µA |
| $I_{IL}$ | Input Low Current | CLK0, CLK_SEL MR, FB_IN, SEL0, SEL1, SEL2, SEL3 | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -5 | | | µA |
| | | PLL_SEL | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |
| $V_{OH}$ | Output High Voltage; NOTE 1 | | | 2.6 | | | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | | | | 0.5 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}$/2. In the Parameter Measurement Information section, see 3.3V Output Load Test Circuit figure.

**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,** $V_{DD} = V_{DDA} = V_{DDO}$ = 3.3V±5%, TA = -40°C TO 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | CLK1 | $V_{DD} = V_{IN}$ = 3.465V | | | 150 | µA |
| | | nCLK1 | $V_{DD} = V_{IN}$ = 3.465V | | | 5 | µA |
| $I_{IL}$ | Input Low Current | CLK1 | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -5 | | | µA |
| | | nCLK1 | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |
| $V_{PP}$ | Peak-to-Peak Input Voltage | | | 0.15 | | 1.3 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 | | | GND + 0.5 | | $V_{DD}$ - 0.85 | V |

NOTE 1: Common mode voltage is defined as $V_{IH}$.
NOTE 2: For single ended applications, the maximum input voltage for CLK1, nCLK1 is $V_{DD}$ + 0.3V.

**TABLE 5A. AC CHARACTERISTICS,** $V_{DD} = V_{DDA} = V_{DDO}$ = 3.3V±5%, TA = -40°C TO 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | | | 15.625 | | 275 | MHz |
| $tp_{LH}$ | Propagation Delay, Low-to-High; NOTE 1 | CLK0 | PLL_SEL = 0V, f ≤ 350MHz, Qx ÷ 2 | 5 | | 7 | ns |
| | | CLK1, nCLK1 | PLL_SEL = 0V, f ≤ 350MHz, Qx ÷ 2 | 5 | | 7.3 | ns |
| t(Ø) | Static Phase Offset; NOTE 2, 4 | CLK0 | PLL_SEL = 3.3V, fREF ≤ 200MHz, Qx ÷ 1 | -100 | 25 | 150 | ps |
| | | CLK1, nCLK1 | PLL_SEL = 3.3V, fREF ≤ 167MHz, Qx ÷ 1 | -15 | +135 | 285 | ps |
| | | | PLL_SEL = 3.3V, fREF = 200MHz, Qx ÷ 1 | -250 | -100 | 50 | ps |
| *t*sk(o) | Output Skew; NOTE 3, 4 | CLK0 | PLL_SEL = 0V | | | 65 | ps |
| | | CLK1, nCLK1 | PLL_SEL = 0V | | | 55 | ps |
| *t*jit(cc) | Cycle-to-Cycle Jitter; NOTE 4 | | $f_{OUT}$ > 40MHz | | | 45 | ps |
| $t_L$ | PLL Lock Time | | | | | 1 | mS |
| $t_R$ | Output Rise Time | | | 400 | | 950 | ps |
| $t_F$ | Output Fall Time | | | 400 | | 950 | ps |
| odc | Output Duty Cycle | | | 43 | | 57 | % |

All parameters measured at $f_{MAX}$ unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at $V_{DDO}$/2.
NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 3: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}$/2.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

**TABLE 4D. POWER SUPPLY DC CHARACTERISTICS,** $V_{DD} = V_{DDA} = V_{DDO}$ = 2.5V±5%, TA = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Input Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $V_{DDA}$ | Analog Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $V_{DDO}$ | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $I_{DD}$ | Input Supply Current | | | | 90 | mA |
| $I_{DDA}$ | Analog Supply Current | | | | 15 | mA |
| $I_{DDO}$ | Output Supply Current | | | | 20 | mA |

**TABLE 4E. LVCMOS / LVTTLE DC CHARACTERISTICS,** $V_{DD} = V_{DDA} = V_{DDO}$ = 2.5V±5%, TA = -40°C TO 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | PLL_SEL, CLK_SEL, SEL0, SEL1, SEL2, SEL3, FB_IN, MR | | 2 | | $V_{DD}$ + 0.3 | V |
| | | CLK0 | | 2 | | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | PLL_SEL, CLK_SEL, SEL0, SEL1, SEL2, SEL3, FB_IN, MR | | -0.3 | | 0.8 | V |
| | | CLK0 | | -0.3 | | 1.3 | V |
| $I_{IH}$ | Input High Current | CLK0, CLK_SEL MR, FB_IN, SEL0, SEL1, SEL2, SEL3 | $V_{DD} = V_{IN}$ = 2.625V | | | 150 | µA |
| | | PLL_SEL | $V_{DD} = V_{IN}$ = 2.625V | | | 5 | µA |
| $I_{IL}$ | Input Low Current | CLK0, CLK_SEL MR, FB_IN, SEL0, SEL1, SEL2, SEL3 | $V_{DD}$ = 2.625V, $V_{IN}$ = 0V | -5 | | | µA |
| | | PLL_SEL | $V_{DD}$ = 2.625V, $V_{IN}$ = 0V | -150 | | | µA |
| $V_{OH}$ | Output High Voltage; NOTE 1 | | | 1.8 | | | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | | | | 0.5 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}$/2. In the Parameter Measurement Information section, see 2.5V Output Load Test Circuit figure.

**TABLE 4F. DIFFERENTIAL DC CHARACTERISTICS,** $V_{DD} = V_{DDA} = V_{DDO}$ = 2.5V±5%, TA = -40°C TO 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | CLK1 | $V_{DD} = V_{IN}$ = 2.625V | | | 150 | µA |
| | | nCLK1 | $V_{DD} = V_{IN}$ = 2.625V | | | 5 | µA |
| $I_{IL}$ | Input Low Current | CLK1 | $V_{DD}$ = 2.625V, $V_{IN}$ = 0V | -5 | | | µA |
| | | nCLK1 | $V_{DD}$ = 2.625V, $V_{IN}$ = 0V | -150 | | | µA |
| $V_{PP}$ | Peak-to-Peak Input Voltage | | | 0.15 | | 1.3 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 | | | GND + 0.5 | | $V_{DD}$ - 0.85 | V |

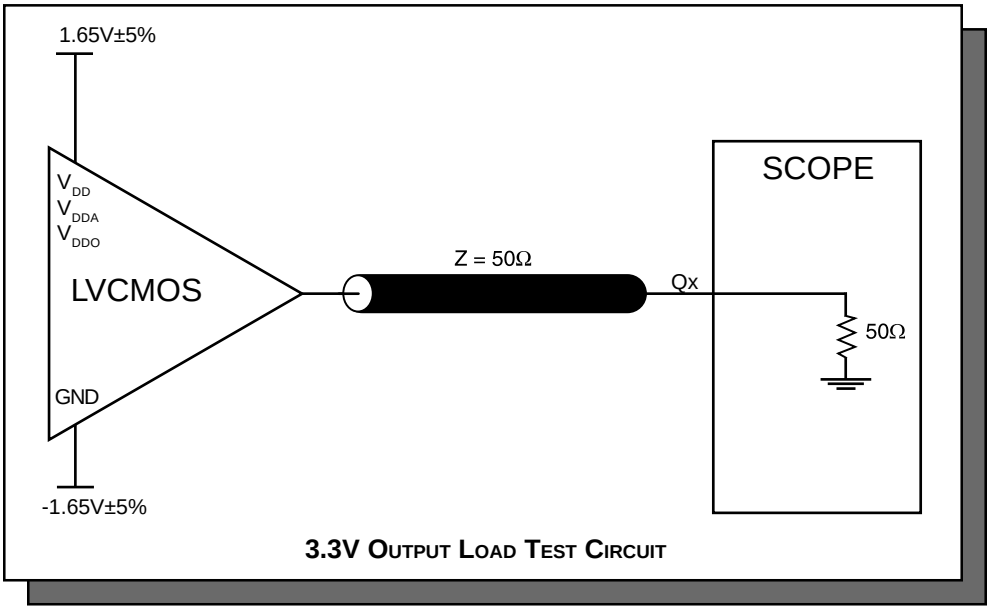
NOTE 1: Common mode voltage is defined as $V_{IH}$.
NOTE 2: For single ended applications, the maximum input voltage for CLK1, nCLK1 is $V_{DD}$ + 0.3V.

**TABLE 5B. AC CHARACTERISTICS,** $V_{DD} = V_{DDA} = V_{DDO}$ = 2.5V±5%, TA = -40°C TO 85°C

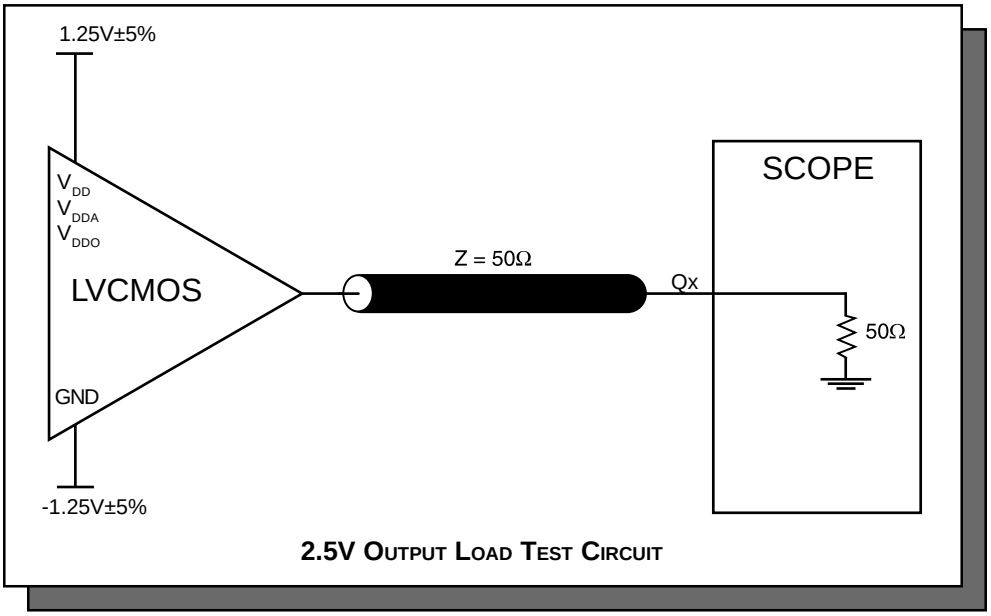
| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | | | 15.625 | | 275 | MHz |
| $tp_{LH}$ | Propagation Delay, Low-to-High; NOTE 1 | CLK0 | PLL_SEL = 0V, f ≤ 350MHz, Qx ÷ 2 | 5 | | 7 | ns |
| | | CLK1, nCLK1 | PLL_SEL = 0V, f ≤ 350MHz, Qx ÷ 2 | 5 | | 7.3 | ns |
| t(Ø) | Static Phase Offset; NOTE 2, 4 | CLK0 | PLL_SEL = 2.5V, fREF ≤ 200MHz, Qx ÷ 1 | -250 | 25 | 200 | ps |
| | | CLK1, nCLK1 | PLL_SEL = 2.5V, fREF = 133MHz, Qx ÷ 1 | -50 | 100 | 250 | ps |
| | | | PLL_SEL = 2.5V, fREF = 200MHz, Qx ÷ 1 | -300 | -100 | 100 | ps |
| *t*sk(o) | Output Skew; NOTE 3, 4 | CLK0 | PLL_SEL = 0V | | | 65 | ps |
| | | CLK1, nCLK1 | PLL_SEL = 0V | | | 55 | ps |
| *t*jit(cc) | Cycle-to-Cycle Jitter; NOTE 4 | | $f_{OUT}$ > 40MHz | | | 45 | ps |
| $t_L$ | PLL Lock Time | | | | | 1 | mS |
| $t_R$ | Output Rise Time | | | 400 | | 950 | ps |
| $t_F$ | Output Fall Time | | | 400 | | 950 | ps |
| odc | Output Duty Cycle | | | 43 | | 57 | % |

All parameters measured at $f_{MAX}$ unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at $V_{DDO}/2$.
NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 3: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

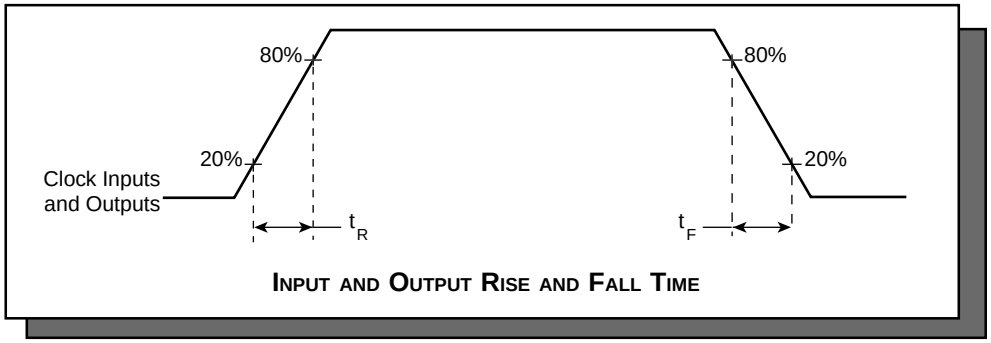
# PARAMETER MEASUREMENT INFORMATION



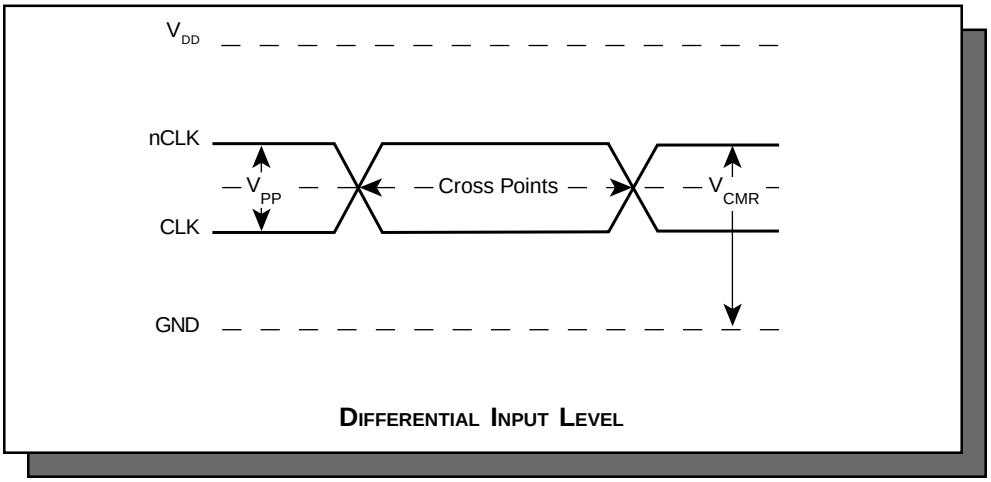

**3.3V OUTPUT LOAD TEST CIRCUIT**



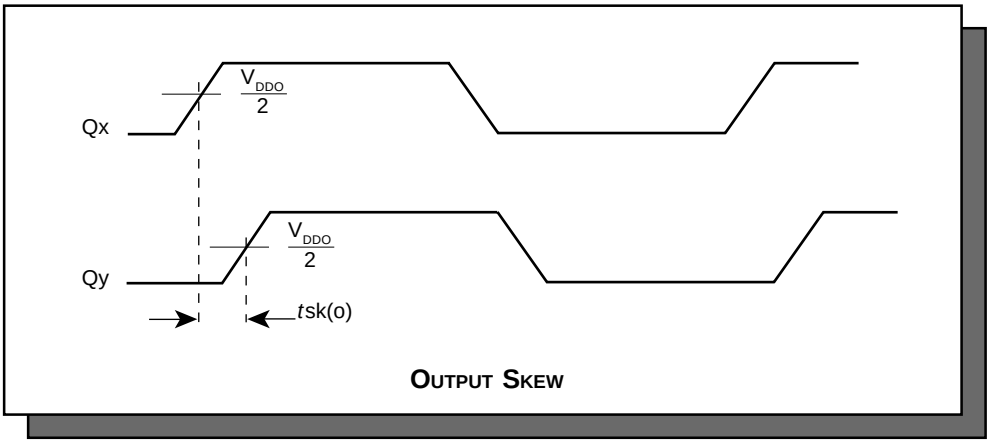

**2.5V OUTPUT LOAD TEST CIRCUIT**



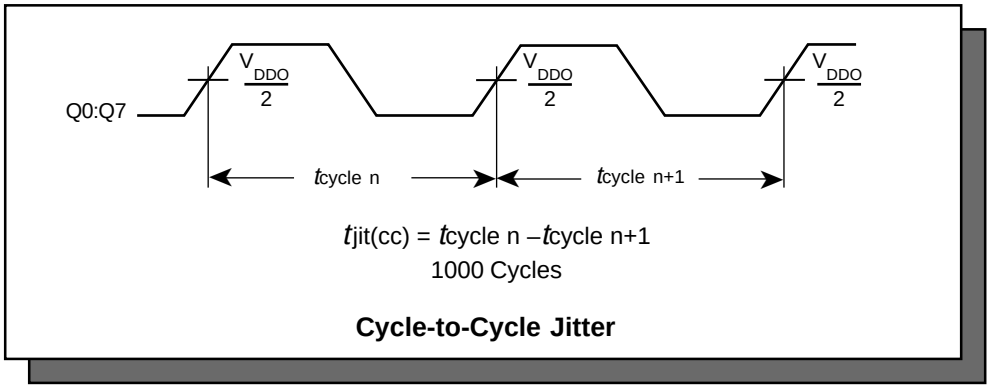

**INPUT AND OUTPUT RISE AND FALL TIME**




**DIFFERENTIAL INPUT LEVEL**

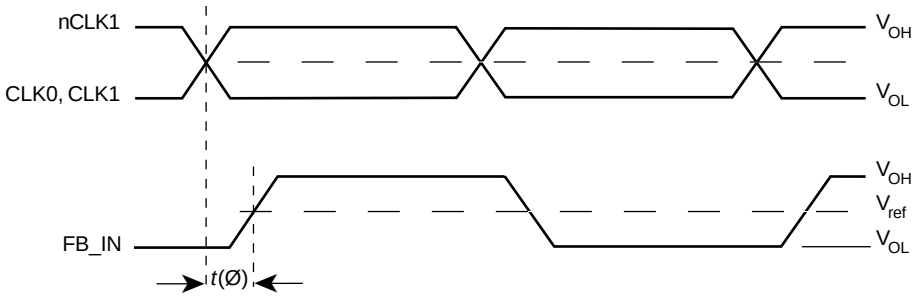



**OUTPUT SKEW**



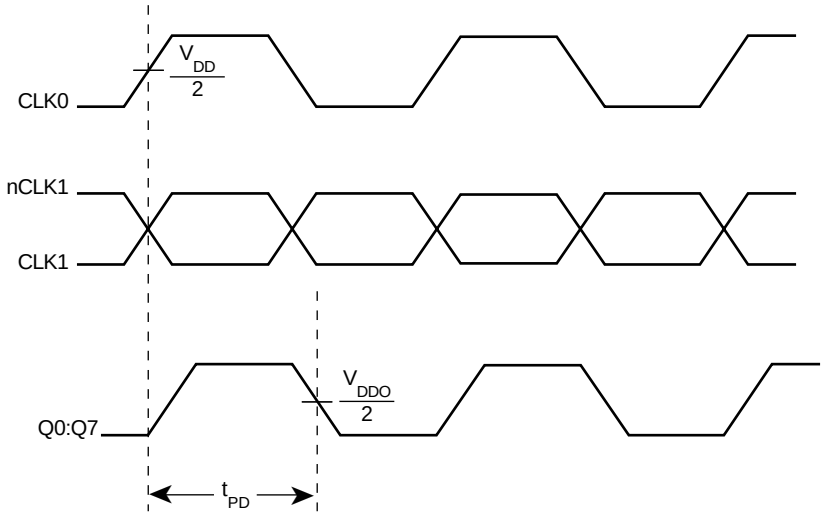

$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$
1000 Cycles

**Cycle-to-Cycle Jitter**

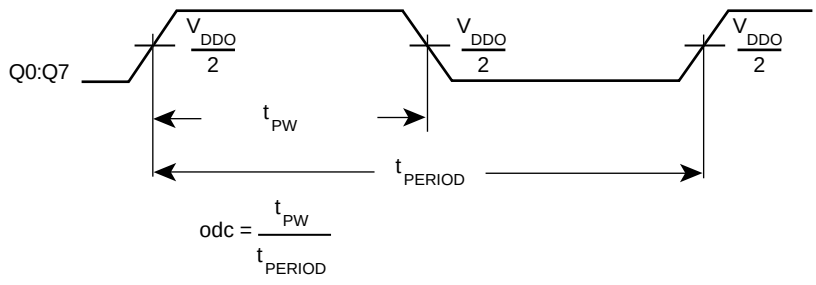



$t(Ø)_{mean}$ = Static Phase Offset
(where $t(Ø)$ is any random sample, and $t(Ø)_{mean}$ is the average of the sampled cycles measured on controlled edges)

**STATIC PHASE OFFSET**




**PROPAGATION DELAY**




**$t_{PW}$, odc AND $t_{PERIOD}$**

# APPLICATION INFORMATION

## POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8705I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. $V_{DD}$, $V_{DDA}$, and $V_{DDO}$ should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each $V_{DDA}$.

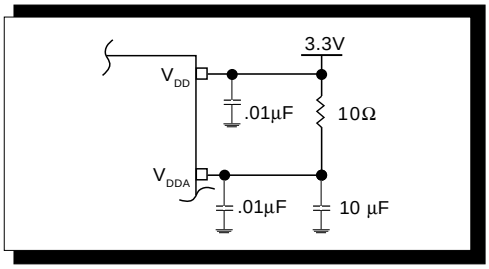



**FIGURE 1 - POWER SUPPLY FILTERING**

## WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

*Figure 2* shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{DD}$/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{DD}$ = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

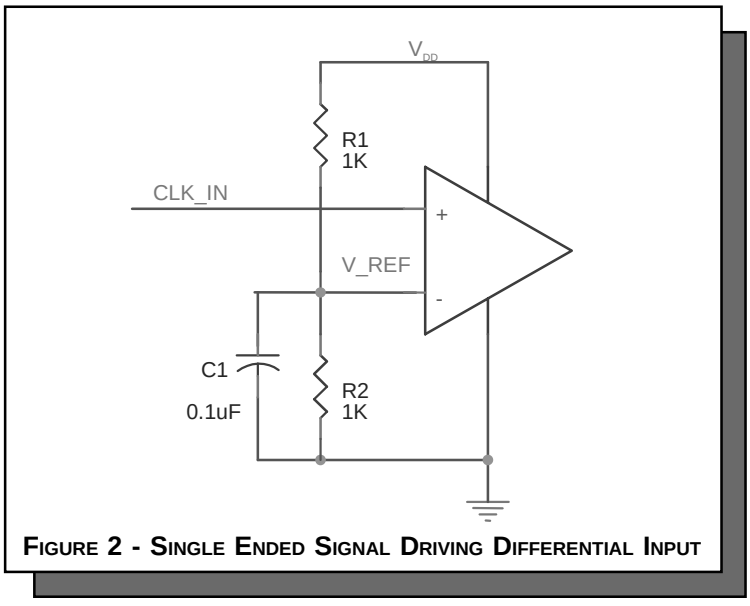



**FIGURE 2 - SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT**

# RELIABILITY INFORMATION

**TABLE 6. $\theta_{JA}$ VS. AIR FLOW TABLE**

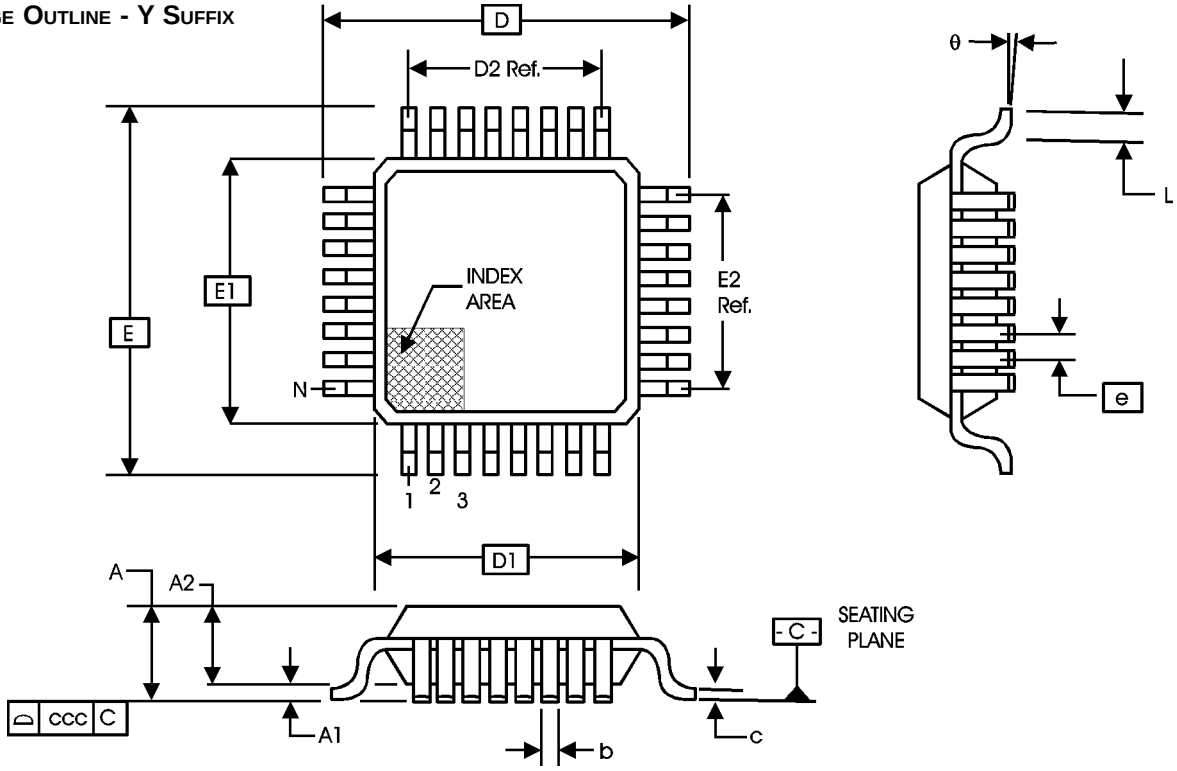
| $\theta_{JA}$ by Velocity (Linear Feet per Minute) | | | |
|---|---|---|---|
| | **0** | **200** | **500** |
| Single-Layer PCB, JEDEC Standard Test Boards | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 47.9°C/W | 42.1°C/W | 39.4°C/W |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS8705I is: 3126

## PACKAGE OUTLINE - Y SUFFIX




### TABLE 7. PACKAGE DIMENSIONS

| JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS | | | |
|---|---|---|---|
| SYMBOL | BBA | | |
| | MINIMUM | NOMINAL | MAXIMUM |
| N | | 32 | |
| A | -- | -- | 1.60 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.30 | 0.37 | 0.45 |
| c | 0.09 | -- | 0.20 |
| D | | 9.00 BASIC | |
| D1 | | 7.00 BASIC | |
| D2 | | 5.60 Ref. | |
| E | | 9.00 BASIC | |
| E1 | | 7.00 BASIC | |
| E2 | | 5.60 Ref. | |
| e | | 0.80 BASIC | |
| L | 0.45 | 0.60 | 0.75 |
| θ | 0° | -- | 7° |
| ccc | -- | -- | 0.10 |

Reference Document: JEDEC Publication 95, MS-026

**TABLE 8. ORDERING INFORMATION**

| Part/Order Number | Marking | Package | Count | Temperature |
|---|---|---|---|---|
| ICS8705BYI | ICS8705BYI | 32 Lead LQFP | 250 per tray | -40°C to 85°C |
| ICS8705BYIT | ICS8705BYI | 32 Lead LQFP on Tape and Reel | 1000 | -40°C to 85°C |