ICS84329-01

700MHz, Low Jitter, Crystal-to-3.3V Differential LVPECL Frequency Synthesizer

General Description

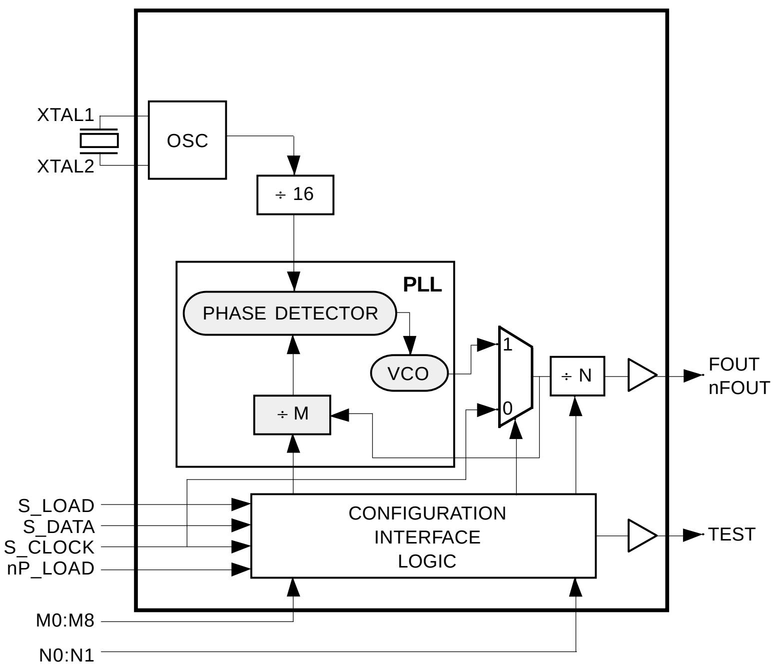
HiPerClockS™

The ICS84329-01 is a general purpose, single output high frequency synthesizer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The VCO operates at a frequency range of 200MHz to 700MHz. The VCO frequency is programmed in steps equal to the value of the crystal frequency divided by 16. The VCO and output frequency can be programmed using the serial or parallel interfaces to the configuration logic. The output can be configured to divide the VCO frequency by 1, 2, 4, and 8. Output frequency steps as small as 125KHz to 1MHz can be achieved using a 16MHz crystal depending on the output dividers.

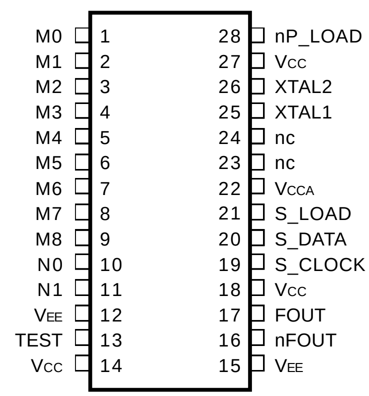
Features

- Fully integrated PLL, no external loop filter requirements
- 1 differential 3.3V LVPECL output
- Crystal oscillator interface
- 25MHz to 700MHz output frequency
- VCO range: 200MHz to 700MHz
- Parallel interface for programming counter and output dividers during power-up
- Serial 3 wire interface
- RMS Period jitter: 5.5ps (maximum)
- Cycle-to-cycle jitter: 35ps (maximum)
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature
- Pin compatible with the SY89429

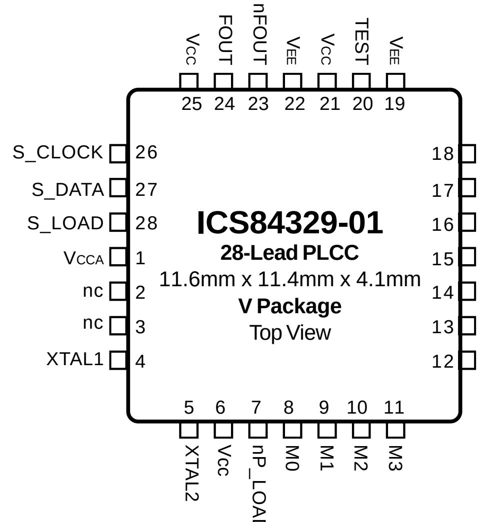
Block Diagram



Pin Assignment



ICS84329-01
28-Lead SOIC
7.5mm x 18.05mm x 2.25mm package body
M Package
Top View



Functional Description

NOTE: The functional description that follows describes operation using a 16MHz crystal. Valid PLL loop divider values for different crystal or input frequencies are defined in the Input Frequency Characteristics, Table 6, NOTE 1.

The ICS84329-01 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A series-resonant, fundamental crystal is used as the input to the on-chip oscillator. The output of the oscillator is divided by 16 prior to the phase detector. With a 16MHz crystal this provides a 1MHz reference frequency. The VCO of the PLL operates over a range of 200MHz to 700MHz. The output of the M divider is also applied to the phase detector.

The phase detector and the M divider force the VCO output frequency to be M times the reference frequency ÷ 16 by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVPECL output buffers. The divider provides a 50% output duty cycle.

The programmable features of the ICS84329-01 support two input modes and programmable M divider and N output divider. The two input operational modes are parallel and serial. *Figure 1* shows the timing diagram for each mode. In parallel mode the nP_LOAD input is LOW. The data on inputs M0 through M8 and N0 through N1 is passed directly to the M divider and N output divider. On the LOW-to-HIGH transition of the nP_LOAD input, the data is latched and the M divider remains loaded until the next LOW transition on nP_LOAD or until a serial event occurs. The TEST output is Mode 000 (shift register out) when operating in the parallel input mode. The relationship between the VCO frequency, the crystal frequency and the M divider is defined as follows:

$$fVCO = \frac{fxtal}{16} \times M$$

The M value and the required values of M0 through M8 are shown in Table 3B, Programmable VCO Frequency Function Table. Valid M values for which the PLL will achieve lock are defined as $200 \le M \le 511$. The frequency out is defined as follows:

$$fout = \frac{fVCO}{N} = \frac{fxtal}{16} \times \frac{M}{N}$$

Serial operation occurs when nP_LOAD is HIGH and S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the M divider when S_LOAD transitions from LOW-to-HIGH. The M divide and N output divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH, data at the S_DATA input is passed directly to the M divider on each rising edge of S_CLOCK. The serial mode can be used to program the M and N bits and test bits T2:T0. The internal registers T2:T0 determine the state of the TEST output as follows:

T2	T1	T0	TEST Output	fOUT
0	0	0	Shift Register Out	fOUT
0	0	1	High	fOUT
0	1	0	PLL Reference Xtal ÷ 16	fOUT
0	1	1	VCO ÷ M (non 50% Duty M divider)	fOUT
1	0	0	fOUT LVCMOS Output Frequency < 200MHz	fOUT
1	0	1	Low	fOUT
1	1	0	S_CLOCK ÷ M (non 50% Duty Cycle M divider)	S_CLOCK ÷ N divider
1	1	1	fOUT ÷ 4	fOUT

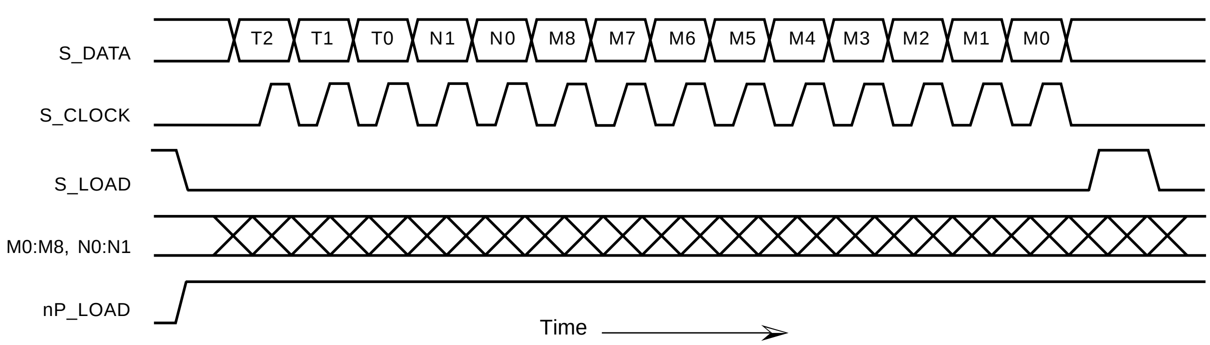


Figure 1 - Parallel & Serial Load Operations

Table 1. Pin Descriptions

Name	Type		Description
M0, M1, M2 M3, M4, M5 M6, M7, M8	Input	Pullup	M divider inputs. Data latched on LOW-to-HIGH transistion of nP_LOAD input. LVCMOS / LVTTL interface levels.
N0, N1	Input	Pullup	Determines N output divider value as defined in Table 3C Function Table. LVCMOS / LVTTL interface levels.
V_{EE}	Power		Negative supply pins.
TEST	Output		Test output which is used in the serial mode of operation. LVCMOS interface levels.
V_{CC}	Power		Positive supply pins.
nFOUT, FOUT	Output		Differential output for the synthesizer. 3.3V LVPECL interface levels.
S_CLOCK	Input	Pulldown	Clocks the serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK.
S_DATA	Input	Pulldown	Shift register serial input. Data sampled on the rising edge of S_CLOCK.
S_LOAD	Input	Pulldown	Controls transition of data from shift register into the M divider. LVCMOS / LVTTL interface levels.
V_{CCA}	Power		Analog supply pin.
nc	Unused		No connect.
XTAL1, XTAL2	Input		Crystal oscillator inputs.
nP_LOAD	Input	Pullup	Parallel load input. Determines when data present at M8:M0 is loaded into M divider, and when data present at N1:N0 sets the N output divider value. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

Table 3A. Parallel and Serial Modes Function Table

Inputs						Conditions
nP_LOAD	M	N	S_LOAD	S_CLOCK	S_DATA	
X	X	X	X	X	X	Reset. M and N bits are all set HIGH.
L	Data	Data	X	X	X	Data on M and N inputs passed directly to M divider and N output divider. TEST mode 000.
↑	Data	Data	X	X	X	Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs.
H	X	X	L	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
H	X	X	↑	L	Data	Contents of the shift register are passed to the M divider and N output divider.
H	X	X	↓	L	Data	M divide and N output divide values are latched.
H	X	X	L	X	X	Parallel or serial input do not affect shift registers.

NOTE: L = LOW
H = HIGH
X = Don't care
↑ = Rising edge transition
↓= Falling edge transition

Table 3B. Programmable VCO Frequency Function Table

VCO Frequency (MHz)	M Divider	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
200	200	0	1	1	0	0	1	0	0	0
201	201	0	1	1	0	0	1	0	0	1
202	202	0	1	1	0	0	1	0	1	0
203	203	0	1	1	0	0	1	0	1	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
509	509	1	1	1	1	1	1	1	0	1
510	510	1	1	1	1	1	1	1	1	0
511	511	1	1	1	1	1	1	1	1	1

NOTE 1: These M divide values and the resulting frequencies correspond to a crystal frequency of 16MHz.

Table 3C. Programmable Output Divider Function Table

Inputs		N Divider Value	Output Frequency (MHz)	
N1	N0		Minimum	Maximum
0	0	1	200	700
0	1	2	100	350
1	0	4	50	175
1	1	8	25	87.5

Absolute Maximum Ratings

Supply Voltage, V_{CCx}	4.6V
Inputs, V_I	-0.5V to V_{CCx} + 0.5V
Outputs, V_O	-0.5V to V_{CC} + 0.5V
Package Thermal Impedance, θ_{JA}	46.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. DC Power Supply Characteristics, $V_{CC} = V_{CCA}$ = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				110	mA
I_{CCA}	Analog Supply Current				15	mA

Table 4B. LVCMOS / LVTTL DC Characteristics, $V_{CC} = V_{CCA}$ = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	S_LOAD, nP_LOAD, S_DATA, S_CLOCK, M0:M8, N0:N1		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	S_LOAD, nP_LOAD, S_DATA, S_CLOCK, M0:M8, N0:N1		-0.3		0.8	V
I_{IH}	Input High Current	M0-M8, N0, N1, nP_LOAD	$V_{CC} = V_{IN}$ = 3.465V			5	µA
		S_LOAD, S_DATA, S_CLOCK	$V_{CC} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	M0-M8, N0, N1, nP_LOAD	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
		S_LOAD, S_DATA, S_CLOCK	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1			2.6			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{CC}/2. See figure "3.3V Output Load Test Circuit" in the "Parameter Measurement Information" section.

Table 4C. LVPECL DC Characteristics, $V_{CC} = V_{CCA}$ = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 1.0	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		0.95	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		10		25	MHz
Equivalent Series Resistance (ESR)				70	Ω
Shunt Capacitance				7	pF

Table 6. Input Frequency Characteristics, $V_{CC} = V_{CCA} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	XTAL; NOTE 1		10		20	MHz
		XTAL; NOTE 1, 2		20		25	MHz
		S_CLOCK				50	MHz

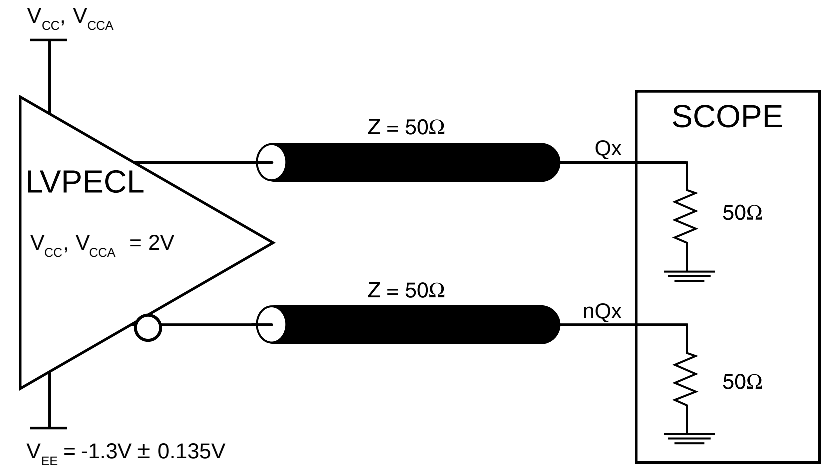
NOTE 1: For the crystal frequency range the M value must be set to achieve the minimum or maximum VCO frequency range of 200MHz or 700MHz. Using the minimum frequency of 10MHz valid values of M are $320 \le M \le 511$.
Using the maximum frequency of 25MHz valid values of M are $128 \le M \le 448$.
NOTE 2: For input frequency greater than 20MHz, XTAL1 requires series capacitance.
Refer to "Crystal Tuning and Oscillator Interface Guide".

Table 7. AC Characteristics, $V_{CC} = V_{CCA} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

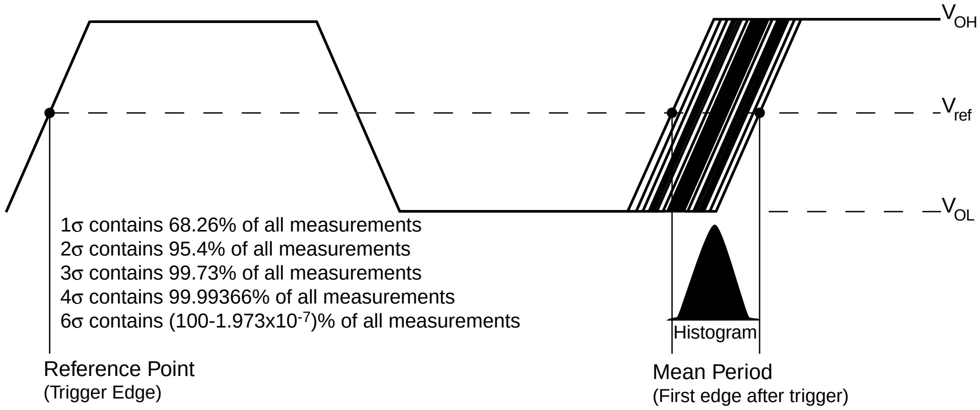
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency				700	MHz
*t*jit(per)	Period Jitter, RMS; NOTE 1, 2	fOUT ≥ 65MHz			5.5	ps
		fOUT < 65MHz			12	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1, 2	fOUT ≥ 50MHz			35	ps
		fOUT < 50MHz			50	ps
t_R	Output Rise Time	20% to 80%	300		800	ps
t_F	Output Fall Time	20% to 80%	300		800	ps
t_S	Setup Time		5			ns
t_H	Hold Time		5			ns
t_L	PLL Lock Time				10	ms
odc	Output Duty Cycle		45	50	55	%

See Parameter Measurement Information section.
Characterized using a 16MHz XTAL.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: See Applications section.

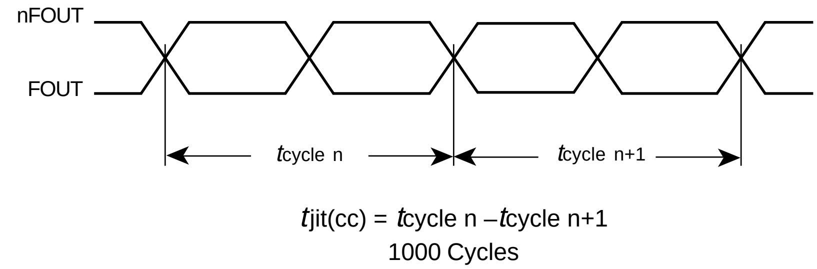
Parameter Measurement Information



3.3V Output Load Test Circuit

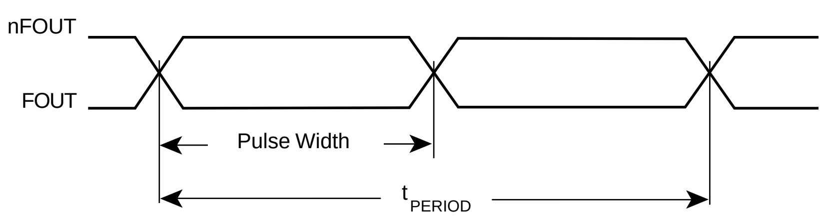


Period Jitter



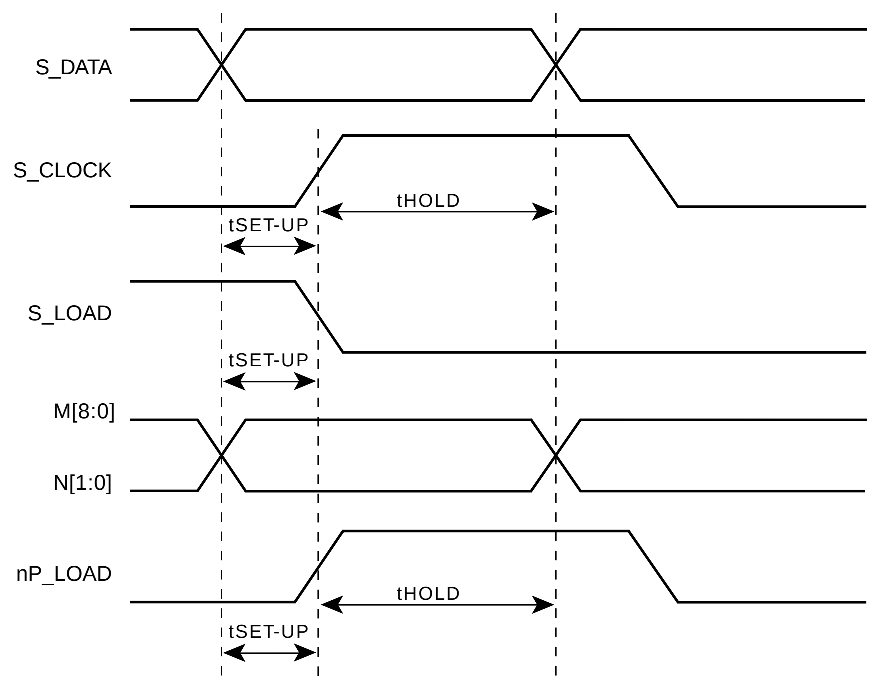
CYCLE-TO-CYLE JITTER

INPUT AND OUTPUT RISE AND FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

odc & t_{PERIOD}



Setup and Hold

Applications

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS84329-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} and V_{CCA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA} pin.

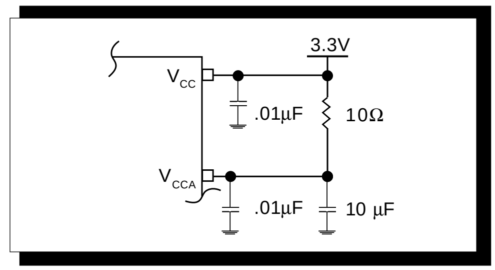


Figure 2 - Power Supply Filtering

Termination for LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. There are a few simple termination schemes. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

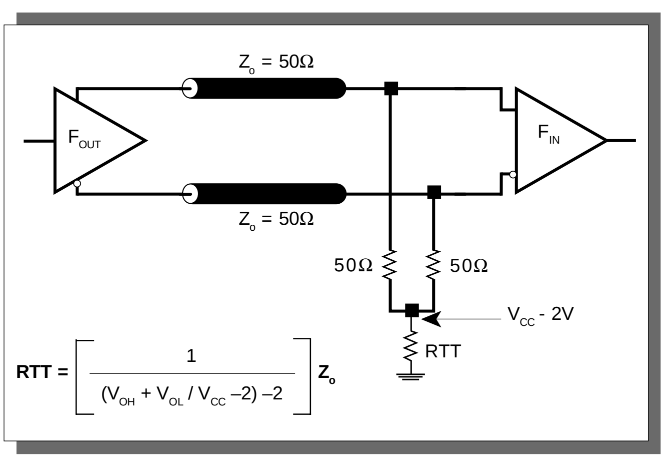


Figure 3A - LVPECL Output Termination

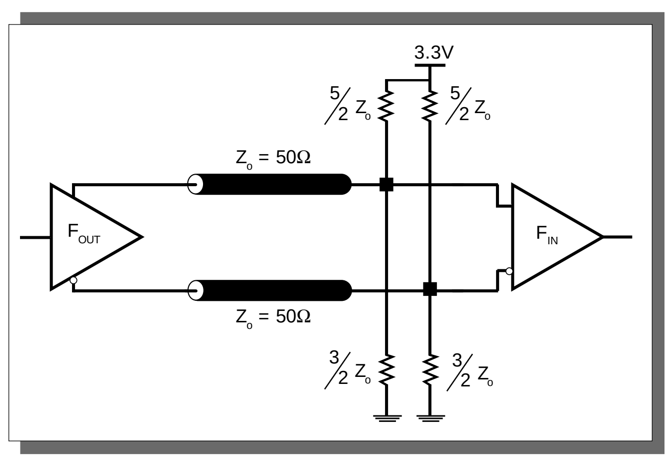


Figure 3B - LVPECL Output Termination

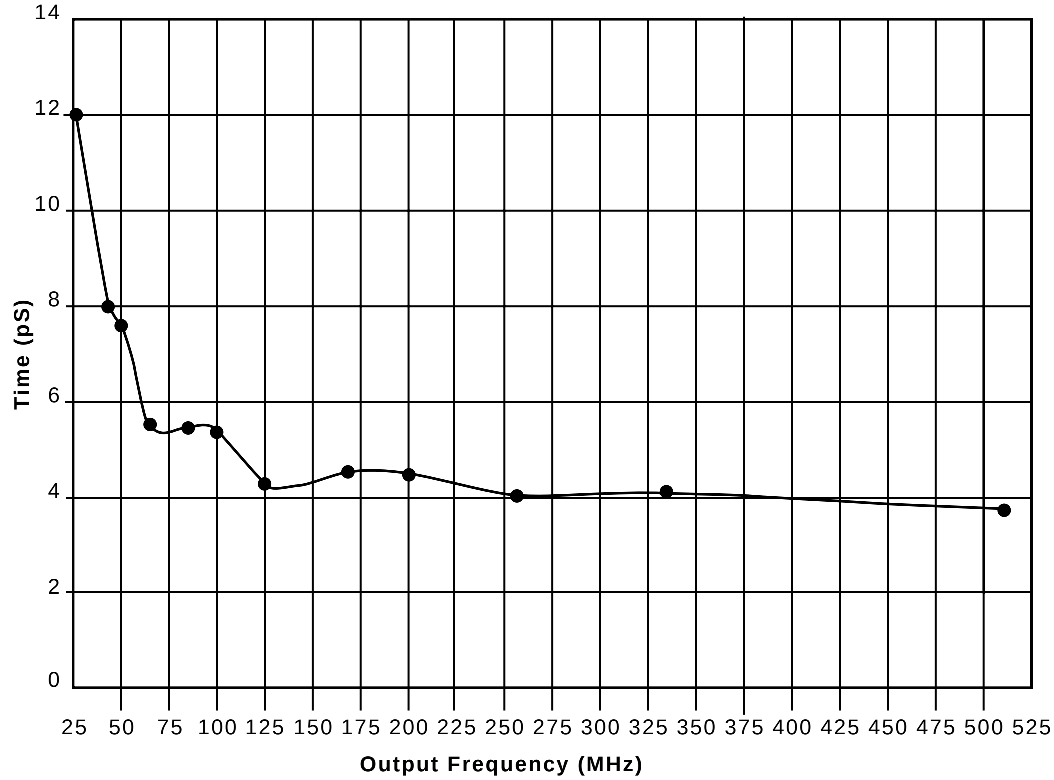


Figure 4A - RMS Jitter vs. fOUT (using a 16MHz XTAL)

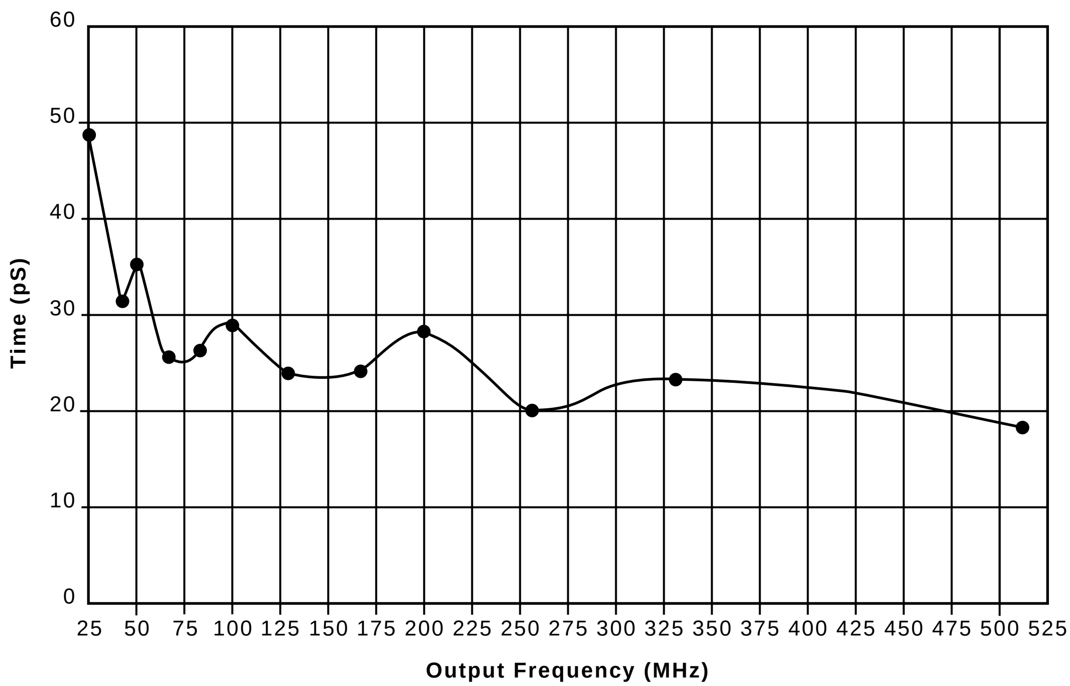


Figure 4B - Cycle-to-Cycle Jitter vs. fOUT (using a 16MHz XTAL)

Crystal Input and Oscillator Interface

The ICS84329-01 features an internal oscillator that uses an external quartz crystal as the source of its reference frequency. The oscillator is a series resonant, multi-vibrator type design. This design provides better stability and eliminates the need for large on chip capacitors. Though a series resonant crystal is preferred, a parallel resonant crystal can be used. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified. A few hundred ppm translates to KHz inaccuracy. In general computing applications, this level of inaccuracy is irrelevant. If better ppm accuracy is required, an external capacitor can be added to a quartz crystal in series to XTAL1. *Figure 5A* shows how to interface with a crystal.

Figures 5A and 5B show various crystal parameters which are recommended only as guidelines. *Figure 5A* shows how to interface a capacitor with a parallel resonant crystal. *Figure 5B* shows the capacitor value needed for the optimum ppm performance over various series resonant crystal frequencies. For IA64/32 platforms which required a Raltron Parallel Resonant Quartz crystal part #AS-16.66-18-SMD-T-M1, a 7pF series capacitor can be used to better the ppm accuracy.

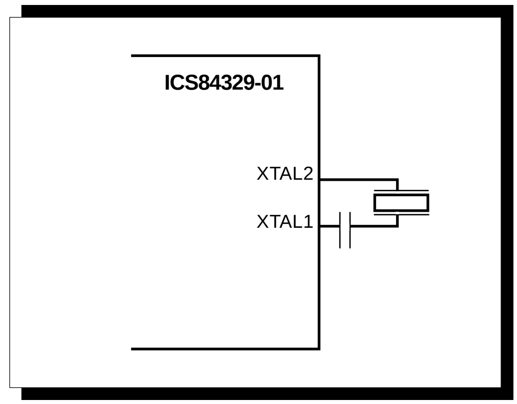
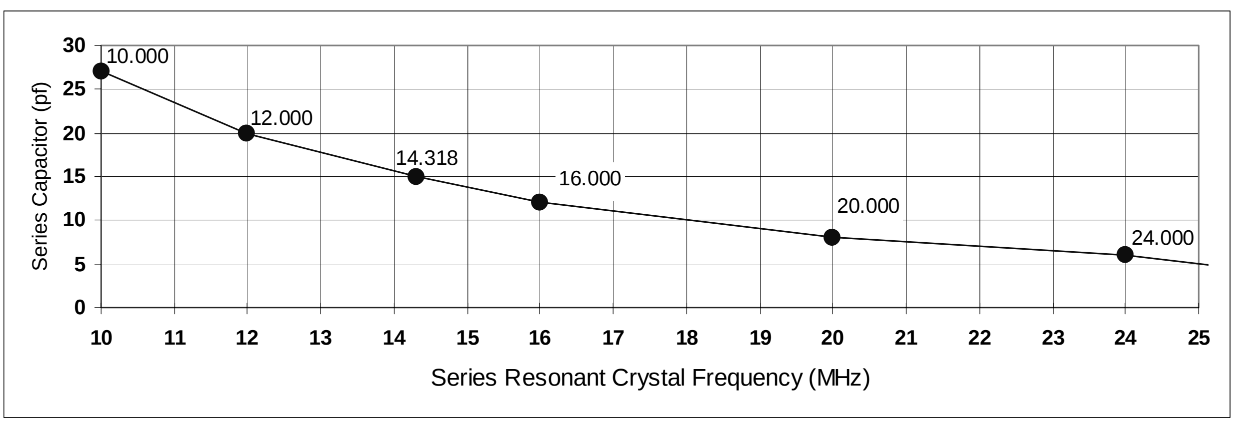


Figure 5A - Crystal Interface

Figure 5B. Recommended tuning capacitance for various series resonant crystals.



Layout Guideline

The schematic of the ICS84329-01 layout example used in this layout guideline is shown in *Figure 6A.* The ICS84329-01 recommended PCB board layout for this example is shown in *Figure 6B.* This layout example is used as a general guideline. The layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stacking of the P.C. board.

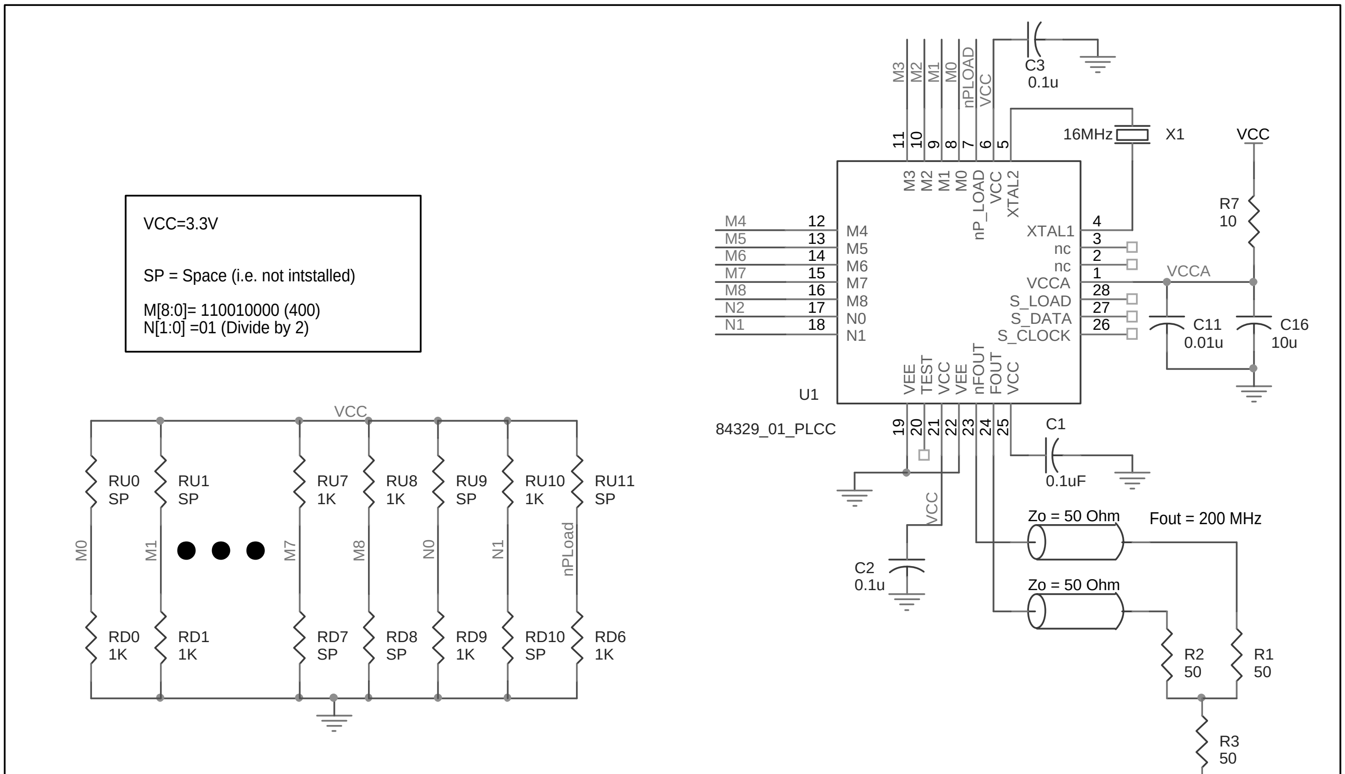


Figure 6A - Schematic of Recommended Layout

The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.

Power and Grounding

Place the decoupling capacitors C1, C2 and C3, as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the V_{CCA} pin as possible.

Clock Traces and Termination

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have the same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The matching termination resistors should be located as close to the receiver input pins as possible.

Crystal

The crystal X1 should be located as close as possible to the pins 24 (XTAL1) and 25 (XTAL2). The trace length between the X1 and U1 should be kept to a minimum to avoid unwanted parasitic inductance and capacitance. Other signal traces should not be routed near the crystal traces.

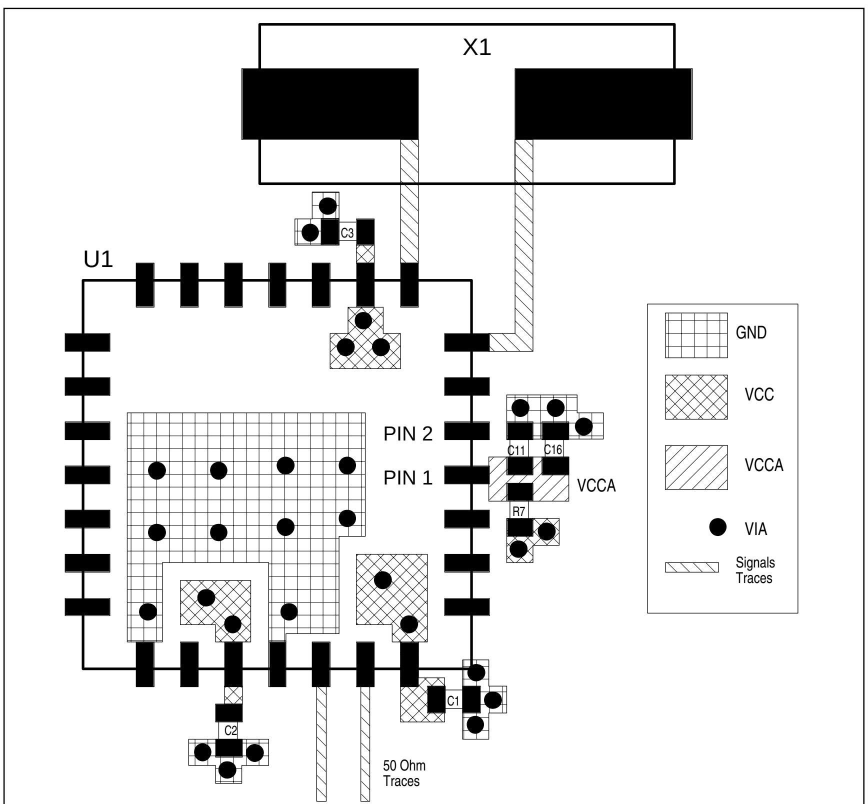


Figure 6B - PCB Board Layout for ICS84329-01

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS84329-01. Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS84329-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 110mA = **381.2mW**
- Power (outputs)$_{MAX}$ = **30.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 1 * 30.2mW = **30.2mW**

Total Power $_{\_MAX}$ (3.465V, with all outputs switching) = 381.2mW + 30.2mW = **411.4mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A
Tj = Junction Temperature
θ_{JA} = Junction-to-Ambient Thermal Resistance
Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 39.7°C/W per Table 8A below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.411W * 39.7°C/W = 86.3°C. This is well below the limit of 125°C

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 8A. Thermal Resistance θ_{JA} for 28-pin SOIC, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	76.2°C/W	60.8°C/W	53.2°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Table 8B. Thermal Resistance θ_{JA} for 28-pin PLCC, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	37.8°C/W	31.1°C/W	28.3°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in the *Figure 7.*

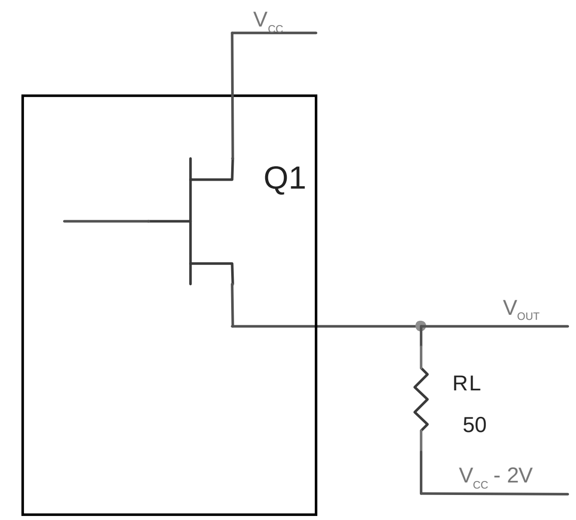


Figure 7 - LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 1.0V}$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{1.0V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 1V)/50\Omega] * 1V = 20.0mW$

$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.2mW**

Reliability Information

Table 9A. θ_{JA} vs. Air Flow SOIC Table

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	76.2°C/W	60.8°C/W	53.2°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Table 9B. θ_{JA} vs. Air Flow PLCC Table

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	37.8°C/W	31.1°C/W	28.3°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for ICS84329-01 is: 4408

Package Outline - M Suffix

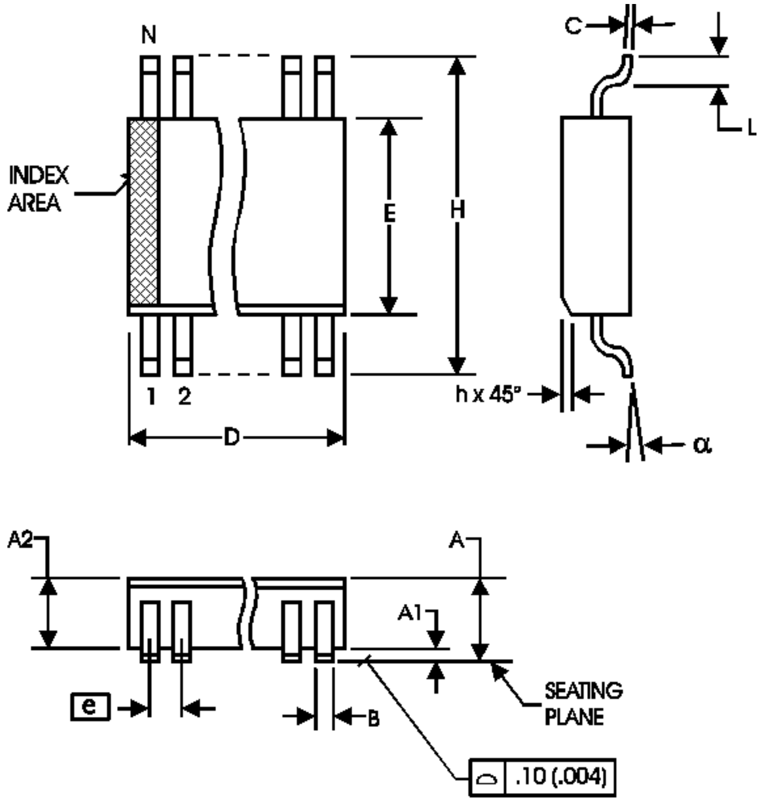


Table 10A. Package Dimensions

SYMBOL	Millimeters	
	MINIMUM	MAXIMUM
N	28	
A	--	2.65
A1	0.10	--
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	17.70	18.40
E	7.40	7.60
e	1.27 BASIC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-013, MO-119

Package Outline - V Suffix

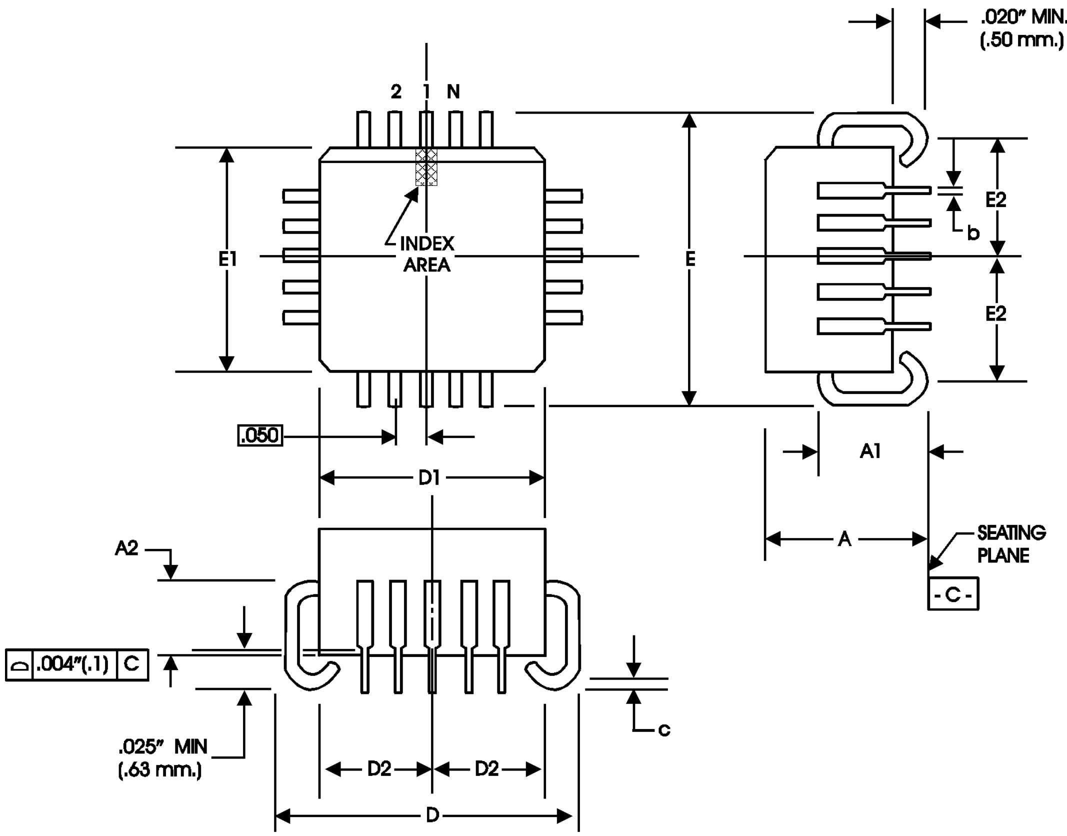


Table 10B. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	28	
A	4.19	4.57
A1	2.29	3.05
A2	1.57	2.11
b	0.33	0.53
c	0.19	0.32
D	12.32	12.57
D1	11.43	11.58
D2	4.85	5.56
E	12.32	12.57
E1	11.43	11.58
E2	4.85	5.56

Reference Document: JEDEC Publication 95, MS-018

Table 11. Ordering Information

Part/Order Number	Marking	Package	Count	Temperature
ICS84329AM-01	ICS84329AM-01	28 Lead SOIC	26 per Tube	0°C to 70°C
ICS84329AM-01T	ICS84329AM-01	28 Lead SOIC on Tape and Reel	1000	0°C to 70°C
ICS84329AV-01	ICS84329AV-01	28 Lead PLCC	38 per Tube	0°C to 70°C
ICS84329AV-01T	ICS84329AV-01	28 Lead PLCC on Tape and Reel	500	0°C to 70°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T6	6 12	Input Frequency Characteristics Table - • updated XTAL from 25MHz Max. to 20MHz Max. • added another XTAL row to include Notes 1 and 2 Added Crystal Input and Oscillator Interface section.	02/14/02