

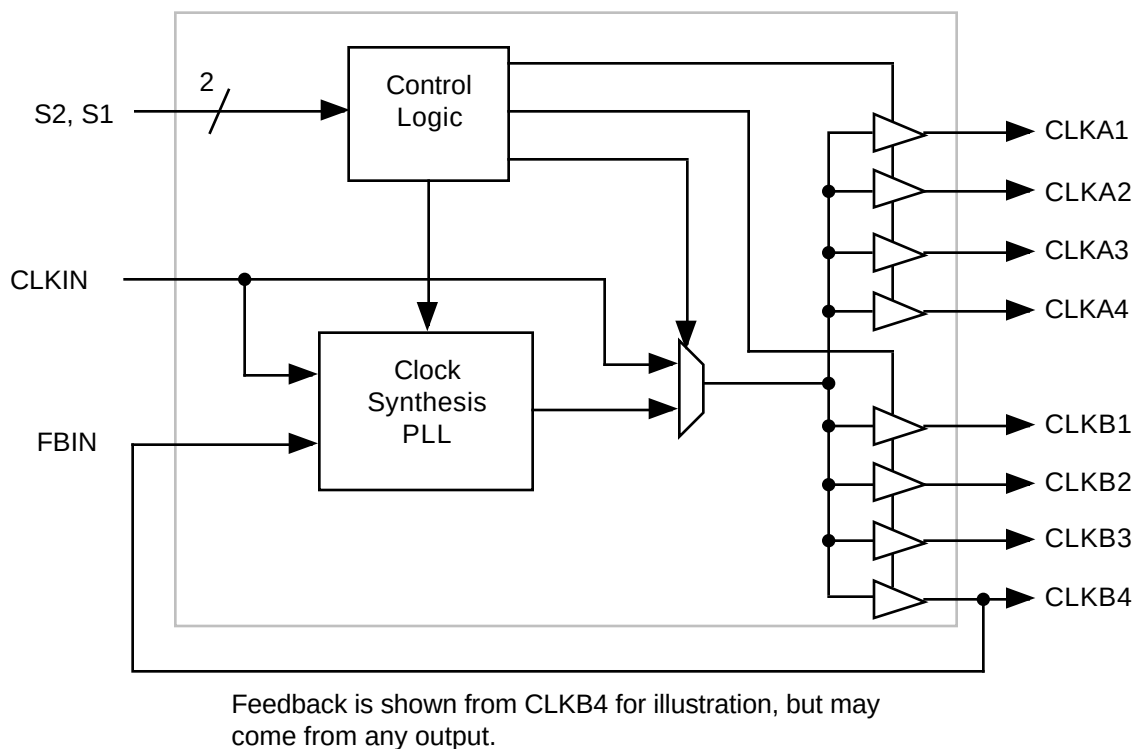
**Description**

The ICS671-03 is a low phase noise, high speed PLL based, 8 output, low skew zero delay buffer. Based on ICS's proprietary low jitter Phase Locked Loop (PLL) techniques, the device provides eight low skew outputs at speeds up to 133 MHz at 3.3 V. The outputs can be generated from the PLL (for zero delay), or directly from the input (for testing), and can be set to tri-state mode or to stop at a low level. For normal operation as a zero delay buffer, any output clock is tied to the FBIN pin.

ICS manufactures the largest variety of clock generators and buffers, and is the largest clock supplier in the world.

**Features**

- Packaged in 16 pin narrow (150 mil) SOIC
- Clock outputs from 10 to 133 MHz
- Zero input-output delay
- Eight low-skew (<200 ps) outputs
- Device-to-device skew <700 ps
- Low jitter (<200 ps)
- Full CMOS outputs with 25 mA output drive capability at TTL levels
- 5 V tolerant FBIN and CLKIN pins
- Tri-state mode for board-level testing
- Advanced, low power, sub-micron CMOS process
- 3.3 V operating voltage
- Industrial temperature range of -40 to 85 °C

**Block Diagram**



## Pin Assignment

|       |   |    |       |
|-------|---|----|-------|
| CLKIN | 1 | 16 | FBIN  |
| CLKA1 | 2 | 15 | CLKA4 |
| CLKA2 | 3 | 14 | CLKA3 |
| VDD   | 4 | 13 | VDD   |
| GND   | 5 | 12 | GND   |
| CLKB1 | 6 | 11 | CLKB4 |
| CLKB2 | 7 | 10 | CLKB3 |
| S2    | 8 | 9  | S1    |

16 pin narrow (150 mil) SOIC

## Output Clock Mode Select Table

| S2 | S1 | CLKA1:A4           | CLKB1:B4           | A & B Source   | PLL Status |
|----|----|--------------------|--------------------|----------------|------------|
| 0  | 0  | Tri-state (Note 1) | Tri-state (Note 1) | PLL            | ON         |
| 0  | 1  | Stopped Low        | Stopped Low        | none           | OFF        |
| 1  | 0  | Running            | Running            | CLKIN (Note 2) | OFF        |
| 1  | 1  | Running            | Running            | PLL            | ON         |

Notes: 1. Outputs are in high impedance state with weak pulldowns.

2. Buffer mode only; not zero delay between input and output.

## Pin Descriptions

| Number       | Name     | Type | Description                                                                  |
|--------------|----------|------|------------------------------------------------------------------------------|
| 1            | CLKIN    | I    | Clock Input. (5 V tolerant)                                                  |
| 2, 3, 14, 15 | CLKA1:A4 | O    | Clock Outputs A1:A4. See above table. Outputs have weak pulldown resistors.  |
| 4, 13        | VDD      | P    | Power supply. Connect both pins to 3.3 V.                                    |
| 5, 12        | GND      | P    | Connect to ground.                                                           |
| 6, 7, 10, 11 | CLKB1:B4 | O    | Clock Outputs B1:B4. See above table. Outputs have weak pulldown resistors.  |
| 8            | S2       | I    | Select input 2. See table above. Internal pull-up.                           |
| 9            | S1       | I    | Select input 1. See table above. Internal pull-up.                           |
| 16           | FBIN     | I    | Feedback Input. Connect to any output under normal operation. (5 V tolerant) |

Key: I = Input; O = output; P = power supply connection. Outputs have a weak internal pull-down when in tri-state mode.

## External Components

The ICS671-03 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01 $\mu$ F should be connected between VDD and GND on pins 4 and 5, and VDD and GND on pins 13 and 12, as close to the device as possible. A series termination resistor of 33  $\Omega$  may be used close to each clock output pin to reduce reflections.



## PRELIMINARY INFORMATION

ICS671-03

## 3.3 Volt Zero Delay, Low Skew Buffer

## Electrical Specifications

| Parameter                                                          | Conditions            | Minimum | Typical | Maximum | Units |
|--------------------------------------------------------------------|-----------------------|---------|---------|---------|-------|
| <b>ABSOLUTE MAXIMUM RATINGS (note 1)</b>                           |                       |         |         |         |       |
| Supply voltage, VDD                                                | Referenced to GND     | -0.5    |         | 7       | V     |
| Inputs and Clock Outputs                                           | Referenced to GND     | -0.5    |         | VDD+0.5 | V     |
| CLKIN and FBIN Inputs                                              |                       | -0.5    |         | 5.5     |       |
| Electrostatic Discharge                                            | MIL-STD-883           | 2000    |         |         | V     |
| Ambient Operating Temperature                                      |                       | -40     |         | 85      | °C    |
| Soldering Temperature                                              | Max of 10 seconds     |         |         | 260     | °C    |
| Junction temperature                                               |                       |         |         | 150     | °C    |
| Storage temperature                                                |                       | -65     |         | 150     | °C    |
| <b>DC CHARACTERISTICS (VDD = 3.3 V unless specified otherwise)</b> |                       |         |         |         |       |
| Operating Voltage, VDD                                             |                       | 3.00    |         | 3.60    | V     |
| Input High Voltage, VIH                                            |                       | 2       |         |         | V     |
| Input Low Voltage, VIL                                             |                       |         |         | 0.8     | V     |
| Output High Voltage, VOH                                           | IOH=-12 mA            | 2.4     |         |         | V     |
| Output Low Voltage, VOL                                            | IOL=12 mA             |         |         | 0.4     | V     |
| Output High Voltage, VOH, CMOS level                               | IOH=-8mA              | VDD-0.4 |         |         | V     |
| Operating Supply Current, IDD (Note 2)                             | No Load, S2=1, S1=1   |         |         | 70      | mA    |
| Power Down Supply Current, IDD                                     | CLKIN=0, S2=0, S1=1   |         | 1.3     |         | mA    |
|                                                                    | CLKIN=0 (Note 3)      |         | 1.3     |         | mA    |
| Short Circuit Current                                              | Each output           |         | ±50     |         | mA    |
| Input Capacitance                                                  | S2, S1, FBIN          |         | 5       |         | pF    |
| <b>AC CHARACTERISTICS (VDD = 3.3 V unless specified otherwise)</b> |                       |         |         |         |       |
| Input Clock Frequency                                              | See table on page 2   | 10      |         | 133     | MHz   |
| Output Clock Frequency                                             | See table on page 2   | 10      |         | 133     | MHz   |
| Output Clock Rise Time, CL=30pF                                    | 0.8 to 2.0V           |         |         | 1.5     | ns    |
| Output Clock Fall Time, CL=30pF                                    | 2.0 to 0.8V           |         |         | 1.25    | ns    |
| Output Clock Duty Cycle, VDD=3.3V                                  | At VDD/2              | 45      | 50      | 55      | %     |
| Device to Device Skew, equally loaded                              | rising edges at VDD/2 |         |         | 700     | ps    |
| Output to Output Skew, equally loaded                              | rising edges at VDD/2 |         |         | 200     | ps    |
| Input to Output Skew, FBIN to CLKA4, S1=1, S0 =1 (Note 2)          |                       |         |         |         |       |
|                                                                    | rising edges at VDD/2 |         |         | ±250    | ps    |
| Maximum Absolute Jitter                                            |                       |         | 130     |         | ps    |
| Cycle to Cycle Jitter, 30pF loads                                  |                       |         |         | 300     | ps    |
| PLL Lock Time (Note 4)                                             |                       |         |         | 1.0     | ms    |

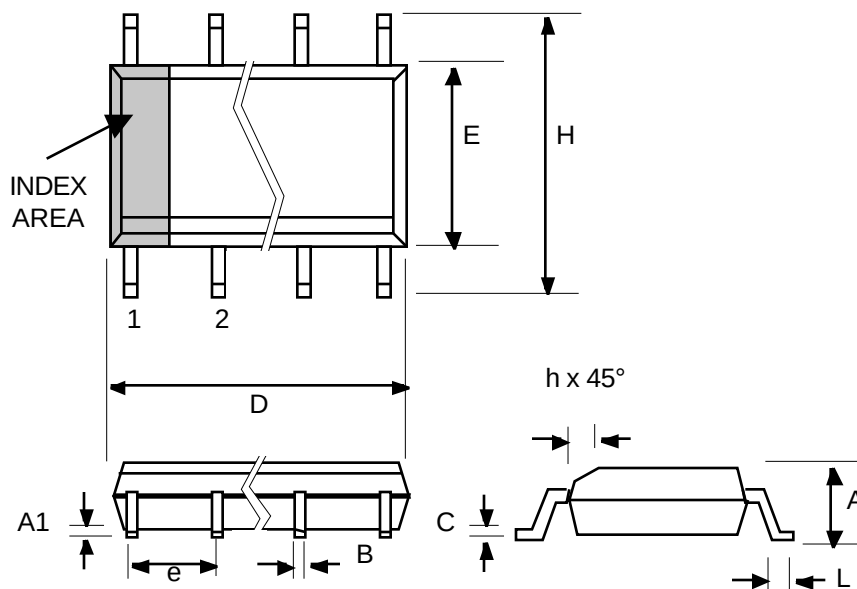
- Notes: 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
2. With CLKIN = 100 MHz, FBIN to CLKA4, all outputs at 100 MHz.
3. When there is no clock signal present at CLKIN, the ICS671-03 will enter a power down mode. The PLL is stopped and the outputs are tri-state.
4. With VDD at a steady state, and valid clocks at CLKIN and FBIN.



Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC Publication No. 95.)

16 pin SOIC narrow



| Symbol | Inches   |        | Millimeters |       |
|--------|----------|--------|-------------|-------|
|        | Min      | Max    | Min         | Max   |
| A      | 0.0532   | 0.0688 | 1.35        | 1.75  |
| A1     | 0.0040   | 0.0098 | 0.10        | 0.24  |
| B      | 0.0130   | 0.0200 | 0.33        | 0.51  |
| C      | 0.0075   | 0.0098 | 0.19        | 0.24  |
| D      | 0.3859   | 0.3937 | 9.80        | 10.00 |
| E      | 0.1497   | 0.1574 | 3.80        | 4.00  |
| e      | .050 BSC |        | 1.27 BSC    |       |
| H      | 0.2284   | 0.2440 | 5.80        | 6.20  |
| h      | 0.0099   | 0.0195 | 0.25        | 0.50  |
| L      | 0.0160   | 0.0500 | 0.41        | 1.27  |

Ordering Information

| Part/Order Number | Marking     | Shipping packaging | Package     | Temperature   |
|-------------------|-------------|--------------------|-------------|---------------|
| ICS671M-03I       | ICS671M-03I | tubes              | 16 pin SOIC | -40 to +85 °C |
| ICS671M-03IT      | ICS671M-03I | tape and reel      | 16 pin SOIC | -40 to +85 °C |

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