Integrated Circuit Systems, Inc.

ICS9250-51

Frequency Generator & Integrated Buffers for Celeron & PII/III™

Recommended Application:

815 B-Step type chipset.

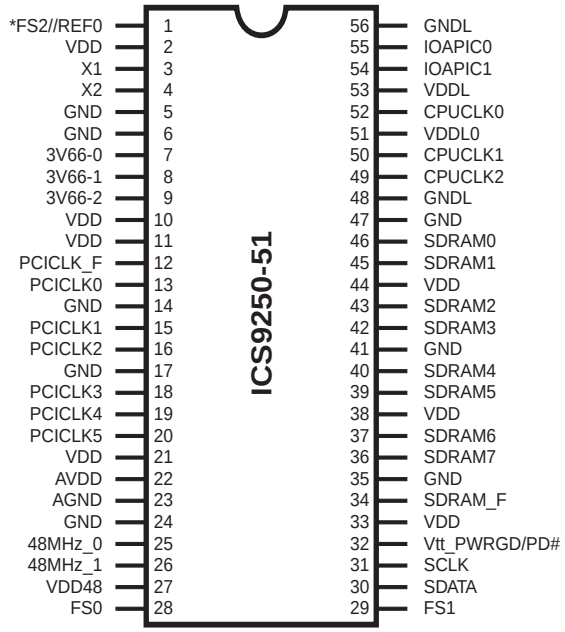
Output Features:

- 3 CPU (2.5V) (up to 133MHz achievable through I^2C)
- 9 SDRAM (3.3V) (up to 133MHz achievable through I^2C)
- 7 PCI (3.3 V) @33.3MHz
- 2 IOAPIC (2.5V) @ 33.3 MHz
- 3 Hublink clocks (3.3 V) @ 66.6 MHz
- 2 (3.3V) @ 48 MHz (Non spread spectrum)
- 1 REF (3.3V) @ 14.318 MHz

Features:

- Supports spread spectrum modulation, 0 to -0.5% down spread.
- I^2C support for power management
- Efficient power management scheme through PD#
- Uses external 14.138 MHz crystal
- Alternate frequency selections available through I^2C control.
- 815 B-Step compliant for frequency select latched inputs. Internal power-on-reset and latching, are delayed until Vtt_PWRGD signal is gated high onto the PD#.

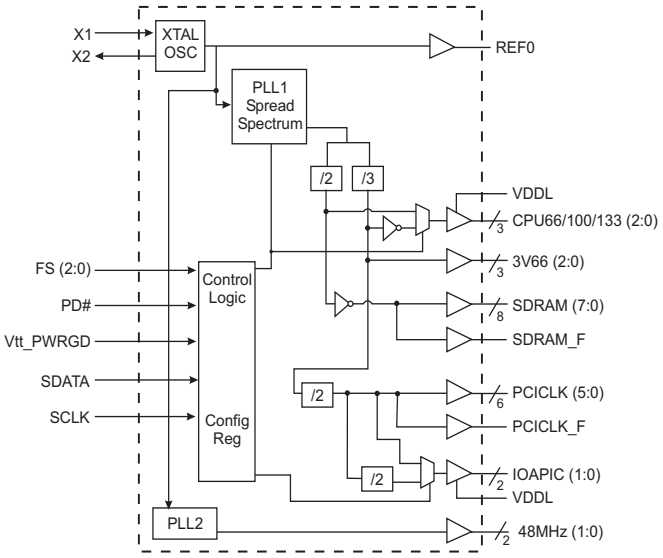
Pin Configuration



56-Pin 300mil SSOP

* This input has a 50KΩ pull-down to GND.

Block Diagram



Functionality

FS2	FS1	FS0	Function
X	0	0	Tristate
X	0	1	Test
0	1	0	Active CPU = 66MHz SDRAM = 100MHz
0	1	1	Active CPU = 100MHz SDRAM = 100MHz
1	1	0	Active CPU = 133MHz SDRAM = 133MHz
1	1	1	Active CPU = 133MHz SDRAM = 100MHz

Power Groups

AVDD = Pin 22 Analog power for PLL
AGND = Pin 23 Analog ground
VDD48 = Pin 27 Analog power for 48MHz PLL
GND48 = Pin 24 Analog ground for 48MHz PLL

General Description

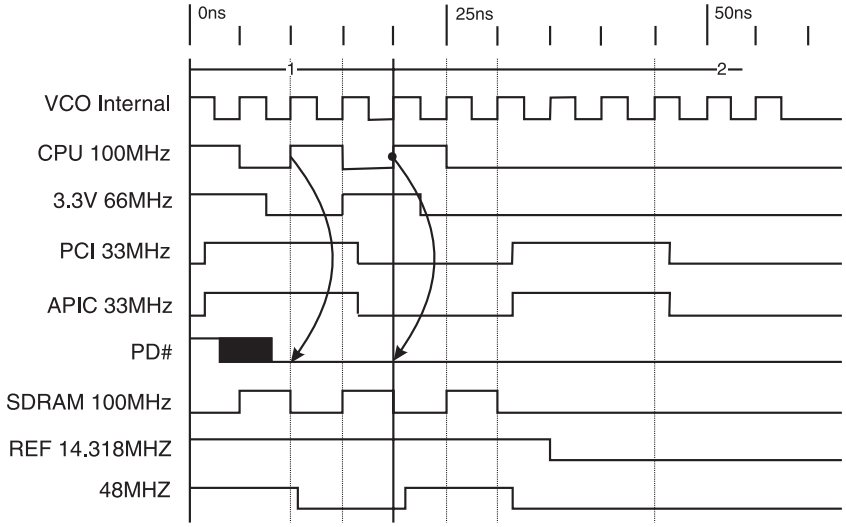
The **ICS9250-51** is a single chip clock solution for 815 B-Step type chipset. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I^2C programming. Spread spectrum typically reduces EMI by 8dB to 10 dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9250-51 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	FS2	IN	Function Select pin. Determines CPU frequency, all output functionality
	REF0	OUT	3.3V, 14.318MHz reference clock output.
3	X1	IN	Crystal input, has internal load cap (33pF) and feedback resistor from X2
4	X2	OUT	Crystal output, nominally 14.318MHz. Has internal load cap (33pF)
5, 6, 14, 17, 24, 35, 41, 47, 48, 56	GND	PWR	Ground pins for 3.3V supply
9, 8, 7	3V66 (2:0)	OUT	3.3V Fixed 66MHz clock outputs for HUB
2, 10, 11, 21, 33, 38, 44	VDD	PWR	3.3V power supply
12	PCICLK_F	OUT	Free running 3.3V PCI clock output
20, 19, 18, 16, 15, 13	PCICLK (5:0)	OUT	3.3V PCI clock outputs
25	48MHz_0	OUT	3.3V Fixed 48MHz clock outputs for USB
26	48MHz_1	OUT	3.3V fixed 48MHz clock output. Stronger output for graphics/video interface (minimum 1V/ns edge rate)
22	AVDD	PWR	Analog power supply for 3.3V CPU PLL
23	AGND	PWR	Analog ground for CPU PLL
27	VDD48	PWR	Analog power for 48MHz PLL
29, 28	FS (1:0)	IN	Function Select pins. Determines CPU frequency, all output functionality. Please refer to Functionality table on page 3.
30	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
31	SCLK	IN	Clock pin of I^2C circuitry 5V tolerant
32	Vtt_PWRGD	IN	This pin acts as a dual function input pin for Vtt_PWRGD and PD# signal. When Vtt_PWRGD goes high the frequency select will be latched at power on thereafter the pin is an asynchronous active low power down pin.
	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
36, 37, 39, 40, 42, 43, 45, 46	SDRAM (7:0)	OUT	3.3V output running 100MHz. All SDRAM outputs can be turned off through I^2C
34	SDRAM_F	OUT	3.3V free running 100MHz SDRAM, cannot be turned off through I^2C
49, 50, 52	CPUCLK (2:0)	OUT	2.5V Host bus clock output. 66MHz, 100MHz or 133MHz depending on FS pins.
51, 53	VDDL	PWR	2.5V power suypply for CPU & IOAPIC
54, 55	IOAPIC (1:0)	OUT	2.5V clock outputs running at 33.3MHz.

Power Down Waveform



Note

1. After PD# is sampled active (Low) for 2 consective rising edges of CPUCLKs, all the output clocks are driven Low on their next High to Low tranistiion.

2. Power-up latency <3ms.

3. Waveform shown for 100MHz

Maximum Allowed Current

815 Condition	Max 2.5V supply consumption Max discrete cap loads, Vddq2 = 2.625V All static inputs = Vddq3 or GND	Max 2.5V supply consumption Max discrete cap loads, Vddq2 = 3.465V All static inputs = Vddq3 or GND
Powerdown Mode (PWRDWN# = 0	10mA	10mA
Full Active 66MHz FS[2:0] = 010	70mA	280mA
Full Active 100MHz FS[2:0] = 011	100mA	280mA
Full Active 133MHz FS[2:0] = 111		

Clock Enable Configuration

PD#	CPUCLK	SDRAM	IOAPIC	66MHz	PCICLK	REF, 48MHz	Osc	VCOs
0	LOW	LOW	LOW	LOW	LOW	LOW	OFF	OFF
1	ON	ON	ON	ON	ON	ON	ON	ON

Truth Table

FS2	FS1	FS0	CPU	SDRAM	3V66	PCI	48MHz	REF	IOAPIC
X	0	0	Tristate	Tristate	Tristate	Tristate	Tristate	Tristate	Tristate
X	0	1	TCLK/2	TCLK/2	TCLK/3	TCLK/6	TCLK/2	TCLK	TCLK/6
0	1	0	66.6 MHz	100 MHz	66.6 MHz	33.3 MHz	48 MHz	14.318 MHz	33.3 MHz
0	1	1	100 MHz	100 MHz	66.6 MHz	33.3 MHz	48 MHz	14.318 MHz	33.3 MHz
1	1	0	133 MHz	133 MHz	66.6 MHz	33.3 MHz	48 MHz	14.318 MHz	33.3 MHz
1	1	1	133 MHz	100 MHz	66.6 MHz	33.3 MHz	48 MHz	14.318 MHz	33.3 MHz

Byte 0: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Description
Bit 7		Reserved ID	0	(Active/Inactive)
Bit 6		Reserved ID	0	(Active/Inactive)
Bit 5		Reserved ID	0	(Active/Inactive)
Bit 4		Reserved ID	0	(Active/Inactive)
Bit 3		SpreadSpectrum (1=On/0=Off)	1	(Active/Inactive)
Bit 2	26	48MHz 1	1	(Active/Inactive)
Bit 1	25	48MHz 0	1	(Active/Inactive)
Bit 0	49	CPUCLK2	1	(Active/Inactive)

Note: Reserved ID bits must be wirtten as "0".

Byte 1: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Description
Bit 7	36	SDRAM7	1	(Active/Inactive)
Bit 6	37	SDRAM6	1	(Active/Inactive)
Bit 5	39	SDRAM5	1	(Active/Inactive)
Bit 4	40	SDRAM4	1	(Active/Inactive)
Bit 3	42	SDRAM3	1	(Active/Inactive)
Bit 2	43	SDRAM2	1	(Active/Inactive)
Bit 1	45	SDRAM1	1	(Active/Inactive)
Bit 0	46	SDRAM0	1	(Active/Inactive)

Notes:

1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.
2. PWD = Power on Default

Byte 2: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Description
Bit 7	9	3V66-2 (AGP)	1	(Active/Inactive)
Bit 6	20	PCICLK5	1	(Active/Inactive)
Bit 5	19	PCICLK4	1	(Active/Inactive)
Bit 4	18	PCICLK3	1	(Active/Inactive)
Bit 3	16	PCICLK2	1	(Active/Inactive)
Bit 2	15	PCICLK1	1	(Active/Inactive)
Bit 1	13	PCICLK0	1	(Active/Inactive)
Bit 0	-	Undefined bit	X	(Active/Inactive)

Notes:

1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.
2. PWD = Power on Default
3. Undefined bit can be wirtten with either a "1" or "0".

Byte 3: ICS Reserved Functionality and frequency select register (Default as noted in PWD)

Bit	Desctiption								PWD
Bit7	ICS Reserved bit (Note 2)								0
Bit6	ICS Reserved bit (Note 2)								0
Bit5	ICS Reserved bit (Note 2)								0
Bit4	ICS Reserved bit (Note 2)								0
Bit3	ICS Reserved bit (Note 2)								0
Bit2	Undefined bit (Note 3)								X
Bit1	Undefined bit (Note 3)								X
Bit 0	Bit 0	FS0	FS1	CPUCLK MHz	SDRAM MHz	3V66 MHz	PCICLK MHz	IOAPIC MHz	0 Note 1
	0	0	0	66.66	100.0	66.66	33.33	33.33	
	0	1	0	100.0	100.0	66.66	33.33	33.33	
	0	0	1	133.32	133.32	66.66	33.33	33.33	
	0	1	1	133.32	100.0	66.66	33.33	33.33	
	1	0	0	66.66	100.0	66.66	33.33	33.33	
	1	1	0	100.0	100.0	66.66	33.33	33.33	
	1	0	1	133.32	133.32	66.66	33.33	33.33	
	1	1	1	133.32	133.32	66.66	33.33	33.33	

Note 1: For system operation, the BSEL lines of the CPU will program FS0, FS2 for the appropriate CPU speed, always with SDRAM = 100MHz. After BIOS verifies the SDRAM is PC133 speed, then bit 0 can be written from the default 0 to 1 to change the SDRAM output frequency from 100MHz to 133MHz. This will only change if the CPU is at the 133MHz FSB speed as shown in this table. The CPU, 3v66, PCI, and IOAPIC clocks will be glitch free during this transition, and only SDRAM will change.

Note 2: "ICS RESERVED BITS" must be writtern as "O".

Note3: Undefined bits can be written either as "1 or 0"

Byte 4: Reserved Register
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Description
Bit 7	-	Reserved	0	(Active/Inactive)
Bit 6	-	Reserved	0	(Active/Inactive)
Bit 5	-	Reserved	0	(Active/Inactive)
Bit 4	-	Reserved	0	(Active/Inactive)
Bit 3	-	Reserved	0	(Active/Inactive)
Bit 2	-	Reserved	0	(Active/Inactive)
Bit 1	-	Reserved	0	(Active/Inactive)
Bit 0	-	Reserved	0	(Active/Inactive)

Byte 5: Reserved Register
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Description
Bit 7	-	Reserved	0	(Active/Inactive)
Bit 6	-	Reserved	0	(Active/Inactive)
Bit 5	-	Reserved	0	(Active/Inactive)
Bit 4	-	Reserved	0	(Active/Inactive)
Bit 3	-	Reserved	0	(Active/Inactive)
Bit 2	-	Reserved	0	(Active/Inactive)
Bit 1	-	Reserved	0	(Active/Inactive)
Bit 0	-	Reserved	0	(Active/Inactive)

Notes:

1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.
2. PWD = Power on Default

Group Timing Relationship Table[1]

Group	CPU 66MHz SDRAM 100MHz		CPU 100MHz SDRAM 100MHz		CPU 133MHz SDRAM 100MHz		CPU 133MHz SDRAM 133MHz	
	Offset	Tolerance	Offset	Tolerance	Offset	Tolerance	Offset	Tolerance
CPU to SDRAM	2.5ns	500ps	5.0ns	500ps	0.0ns	500ps	3.75ns	500ps
CPU to 3V66	7.5ns	500ps	5.0ns	500ps	0.0ns	500ps	0.0ns	500ps
SDRAM to 3V66	0.0ns	500ps	0.0ns	500ps	0.0ns	500ps	3.75ns	500ps
3V66 to PCI	1.5-3.5ns	N/A	1.5-3.5ns	N/A	1.5-3.5ns	N/A	1.5 - 3.5ns	N/A
IOAPIC to PCI	0.0ns	1.0ns	0.0ns	1.0ns	0.0ns	1.0ns	0.0ns	1.0ns
USB & DOT	Asynch	N/A	Asynch	N/A	Asynch	N/A	Asynch	N/A

Absolute Maximum Ratings

Core Supply Voltage . . . . . 4.6 V
I/O Supply Voltage 3.6V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5	2		
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200	-100		mA
Operating Supply Current	$I_{DD3.3OP}$	C_L = 0 pF; 66 MHz		97	115	mA
		C_L = 0 pF; 100 MHz		91	110	
		C_L = 0 pF; 133 MHz		100	165	
		C_L = Max loads; 66 MHz		295	330	
		C_L = Max loads; 100 MHz		280	320	
		C_L = Max loads; 133 MHz		300	395	
	$I_{DD2.5OP}$	C_L = 0 pF; 66 MHz		16	19	
		C_L = 0 pF; 100 MHz		25	35	
		C_L = 0 pF; 133 MHz		26	40	
		C_L = Max loads; 66 MHz		19	30	
		C_L = Max loads; 100 MHz		34	50	
		C_L = Max loads; 133 MHz		40	70	
Powerdown Current	$I_{DD3.3PD}$	C_L = Max loads		220	400	mA
	$I_{DD.25PD}$	Input address V_{DD} or GND		<1	10	
Input Frequency	F_i	V_{DD} = 3.3 V	12	14.32	16	MHz
Pin Inductance	L_{pin}			7		nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{OUT}	Output pin capacitance		6		pF
	C_{INX}	X_1 & X_2 pins	27		45	pF
Transition time[1]	T_{trans}	To 1st crossing of target frequency			5	ms
Settling time[1]	T_s	From 1st crossing to 1% target frequency			5	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target frequency			5	ms
Delay[1]	t_{PZH},t_{PZL}	Output enable delay (all outputs)	1		10	ns
	t_{PHZ},t_{PLZ}	Output disable delay (all outputs)	1		10	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DDL} = 2.5V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}	$V_O = V_{DD}*(0.5)$	13.5		45	Ω
Output Impedance	R_{DSN2B}	$V_O = V_{DD}*(0.5)$	13.5		45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -3 mA	2.3			V
Output Low Voltage	V_{OL2B}	I_{OL} = 5 mA			0.2	V
Output High Current	I_{OH2B}	V_{OH} @ MIN = 1.0 V	-27			mA
		V_{OH} @ MAX = 2.375 V			-27	
Output Low Current	I_{OL2B}	V_{OL} @ MIN = 1.2 V	27			mA
		V_{OL} @ MAX = 0.3 V			30	
Rise Time[1]	t_{r2B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4	1.11	1.6	ns
Fall Time[1]	t_{f2B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4	1.13	1.6	ns
Duty Cycle[1]	d_{t2B}	V_T = 1.25 V, 66, 100 MHz	45	50	55	%
		V_T = 1.25 V, 133 MHz	45	49	55	
Skew window[1]	t_{sk2B}	V_T = 1.25 V		82	175	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	V_T = 1.25 V		122	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 3V66

T_A = 0 - 70C; V_{DD} = 3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP11}	$V_O = V_{DD}*(0.5)$	12		55	Ohms
Output Impedance	R_{DSN11}	$V_O = V_{DD}*(0.5)$	12		55	Ohms
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	V_{OH} @ MIN = 1.0 V	-33			
		V_{OH} @ MAX = 3.135 V			-33	mA
Output Low Current	I_{OL1}	V_{OL} @ MIN = 1.95 V	30			mA
		V_{OL} @ MAX = 0.4 V			38	
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4	1.47	1.8	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	1.5	1.8	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	48.9	55	%
Skew window[1]	t_{sk1}	V_T = 1.5 V		88	175	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc1}$	V_T = 1.5 V		139	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70C; V_{DDL} = 2.5V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP4B1}	$V_O = V_{DD}*(0.5)$	9		30	Ohms
Output Impedance	R_{DSN4B1}	$V_O = V_{DD}*(0.5)$	9		30	Ohms
Output High Voltage	V_{OH4B}	I_{OH} = -1 mA	2			V
Output Low Voltage	V_{OL4B}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH4B}	V_{OH} @ MIN = 1.0 V	-27			mA
		V_{OH} @ MAX = 2.375 V			-27	
Output Low Current	I_{OL4B}	V_{OL} @ MIN = 1.2 V	27			mA
		V_{OL} @ MAX = 0.3 V			30	
Rise Time[1]	t_{r4B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4	1.2	1.6	ns
Fall Time[1]	t_{f4B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4	1.26	1.6	ns
Duty Cycle[1]	d_{t4B}	V_T = 1.25 V	45	50.7	55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc4B}$	V_T = 1.25 V		92	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70C; V_{DD} = 3.3V +/-5%; C_L = 20-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP31}	$V_O = V_{DD}*(0.5)$	10		24	W
Output Impedance	R_{DSN31}	$V_O = V_{DD}*(0.5)$	10		24	W
Output High Voltage	V_{OH3}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL3}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH3}	V_{OH} @ MIN = 2.0 V	-54			mA
		V_{OH} @ MAX = 3.135 V			-46	mA
Output Low Current	I_{OL3}	V_{OL} @ MIN = 1.0 V	54			mA
		V_{OL} @ MAX = 0.4 V			53	mA
Rise Time[1]	t_{r3}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4	1.06	1.6	ns
Fall Time[1]	t_{f3}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	1.37	1.6	ns
Duty Cycle[1]	d_{t3}	V_T = 1.5 V	45	53.7	55	%
Skew window[1]	t_{sk3}	V_T = 1.5 V		69	250	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc3}$	V_T = 1.5 V, 66, 100 MHz		189	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCI

T_A = 0 - 70C; V_{DD} = 3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP11}	$V_O = V_{DD}*(0.5)$	12		55	Ohms
Output Impedance	R_{DSN11}	$V_O = V_{DD}*(0.5)$	12		55	Ohms
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	V_{OH} @ MIN = 1.0 V	-33			mA
		V_{OH} @ MAX = 3.135 V			-33	
Output Low Current	I_{OL1}	V_{OL} @ MIN = 1.95 V	30			mA
		V_{OL} @ MAX = 0.4 V			38	
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4	1.39	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	1.44	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	52.2	55	%
Skew window[1]	t_{sk1}	V_T = 1.5 V		290	500	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc1}$	V_T = 1.5 V		105	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF, 48MHz_0 (Pin 25)

T_A = 0 - 70C; V_{DD} = 3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP51}	$V_O = V_{DD}*(0.5)$	20		60	Ohms
Output Impedance	R_{DSN51}	$V_O = V_{DD}*(0.5)$	20		60	Ohms
Output High Voltage	V_{OH15}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH5}	V_{OH} @ MIN = 1.0 V	-29			mA
		V_{OH} @ MAX = 3.135 V			-23	
Output Low Current	I_{OL5}	V_{OL} @ MIN = 1.95 V	29			mA
		V_{OL} @ MAX = 0.4 V			27	
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4	1.5	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	1.93	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	52.9	55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc5}$	V_T = 1.5 V, Fixed clocks			500	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc5}$	V_T = 1.5 V, Ref clocks		882	1000	ps

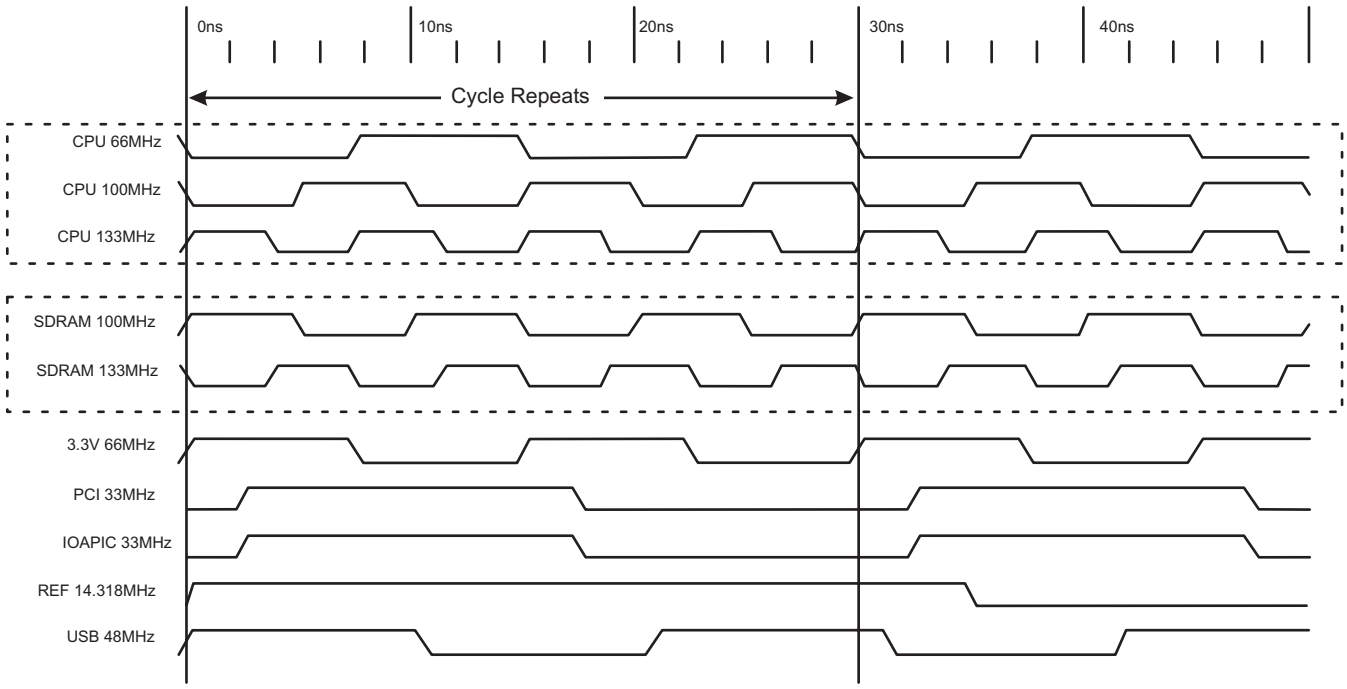
[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 48MHz_1 (Pin 26)

T_A = 0 - 70C; V_{DD} = 3.3V +/-5%; C_L = 10-15 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP31}	$V_O = V_{DD}*(0.5)$	10		24	Ohms
Output Impedance	R_{DSN31}	$V_O = V_{DD}*(0.5)$	10		24	Ohms
Output High Voltage	V_{OH3}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL3}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH3}	V_{OH} @ MIN = 2.0 V	-54			mA
		V_{OH} @ MAX = 3.135 V			-46	
Output Low Current	I_{OL3}	V_{OL} @ MIN = 1.0 V	54			mA
		V_{OL} @ MAX = 0.4 V			53	
Rise Time[1]	t_{r3}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4	1.24	1.6	ns
Fall Time[1]	t_{f3}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	1.28	1.6	ns
Duty Cycle[1]	d_{t3}	V_T = 1.5 V	45	51.7	55	%
Skew	t_{sk3}	V_T = 1.5 V		150	250	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc3B}$	V_T = 1.5 V		189	500	ps

[1]Guaranteed by design, not 100% tested in production.



Group Offset Waveforms

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D2(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

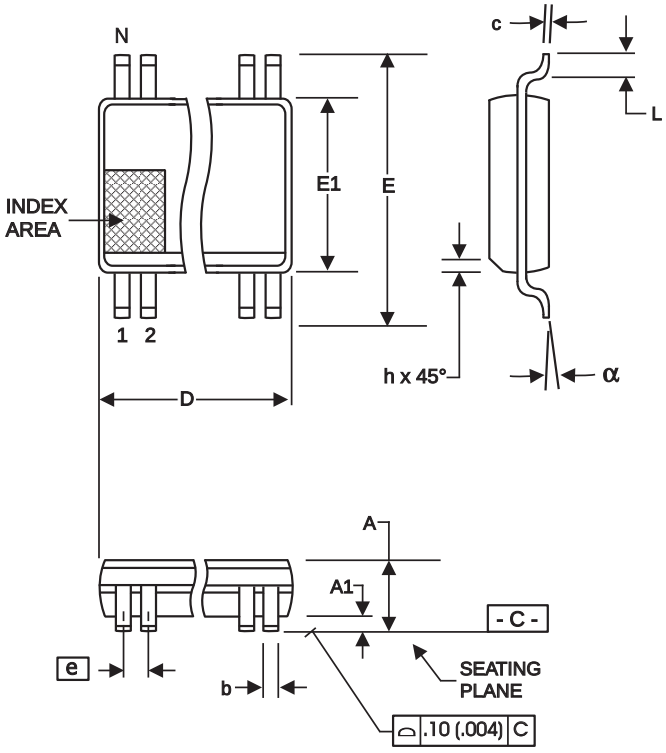
How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D3(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.



300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.413	2.794	.095	.110
A1	0.203	0.406	.008	.016
b	0.203	0.343	.008	.0135
c	0.127	0.254	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.033	10.668	.395	.420
E1	7.391	7.595	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.381	0.635	.015	.025
L	0.508	1.016	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.288	18.542	.720	.730

JEDEC MO-118 6/1/00
DOC# 10-0034 REV B

Ordering Information

ICS9250yF-51-T

Example:

ICS XXXX y F - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device