IS62WV25616ALL
IS62WV25616BLL

256K x 16 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

PRELIMINARY INFORMATION
MARCH 2002

FEATURES

- High-speed access time: 55ns, 70ns
- CMOS low power operation
  - 36 mW (typical) operating
  - 9 µW (typical) CMOS standby
- TTL compatible interface levels
- Single power supply
  - 1.65V--2.2V V_{CC} (62WV25616ALL)
  - 2.5V--3.6V V_{CC} (62WV25616BLL)
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available
- 2CS Option Available

DESCRIPTION

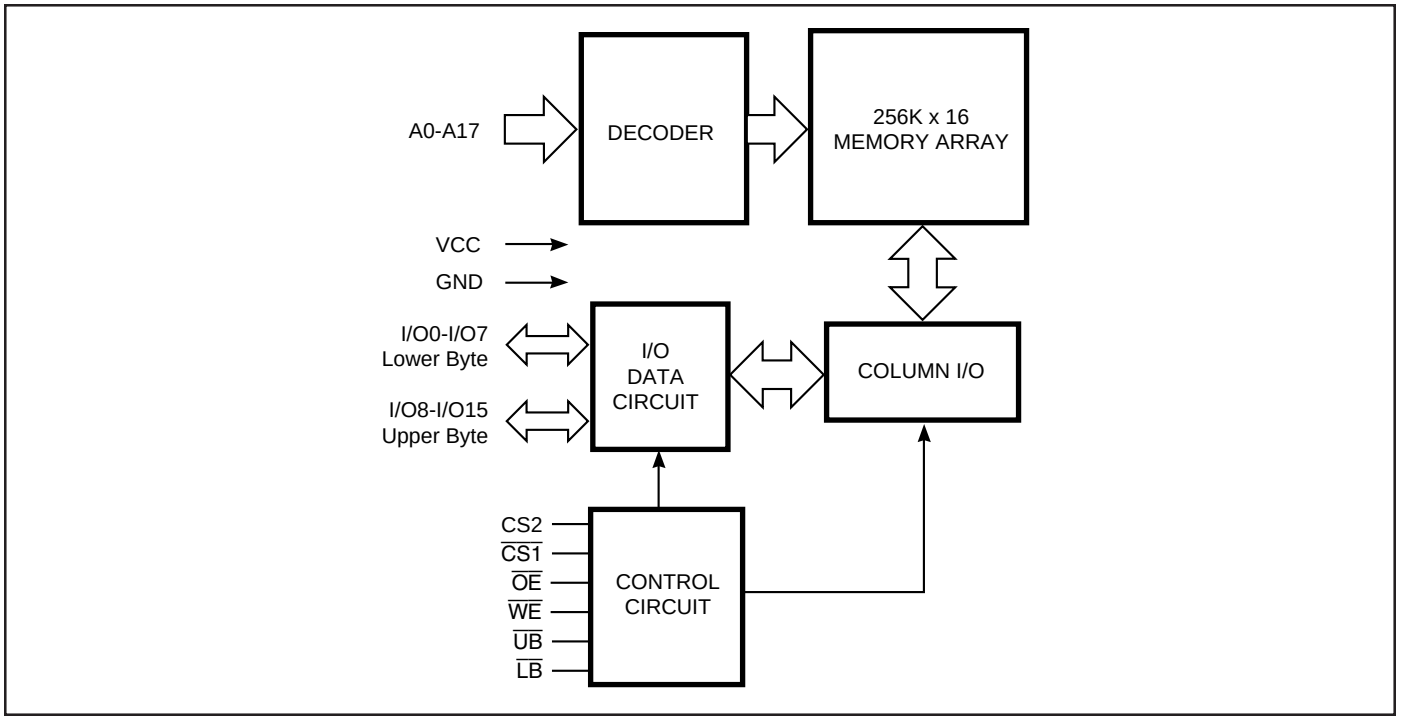
The *ISSI* IS62WV25616ALL / IS62WV25616BLL are high-speed, 4M bit static RAMs organized as 128K words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CS1}$ is HIGH (deselected) or when CS2 is LOW (deselected) or when $\overline{CS1}$ is LOW, CS2 is HIGH and both $\overline{LB}$ and $\overline{UB}$ are HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

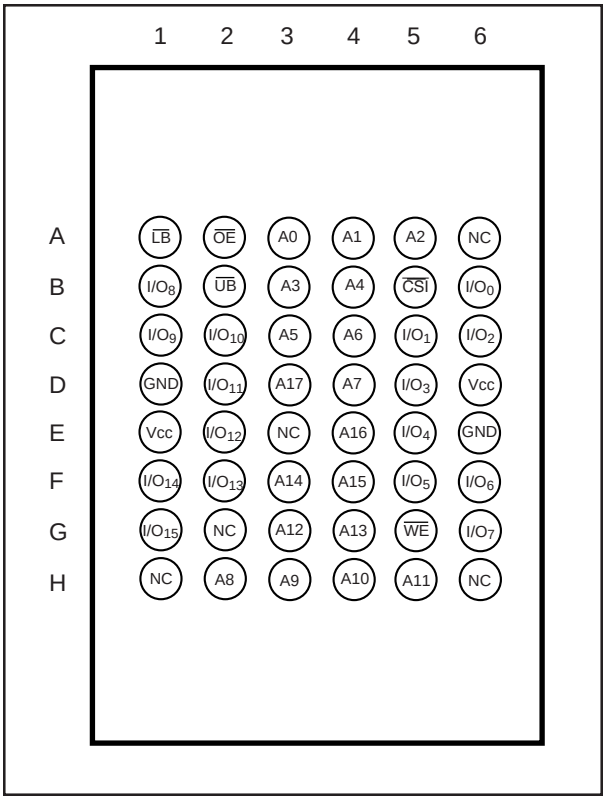
The IS62WV25616ALL and IS62WV25616BLL are packged in the JEDEC standard 48-pin mini BGA (6mm x 8mm) and 44-Pin TSOP (TYPE II). 48-pin mini BGA is available both in 1CS and 2CS options.

FUNCTIONAL BLOCK DIAGRAM

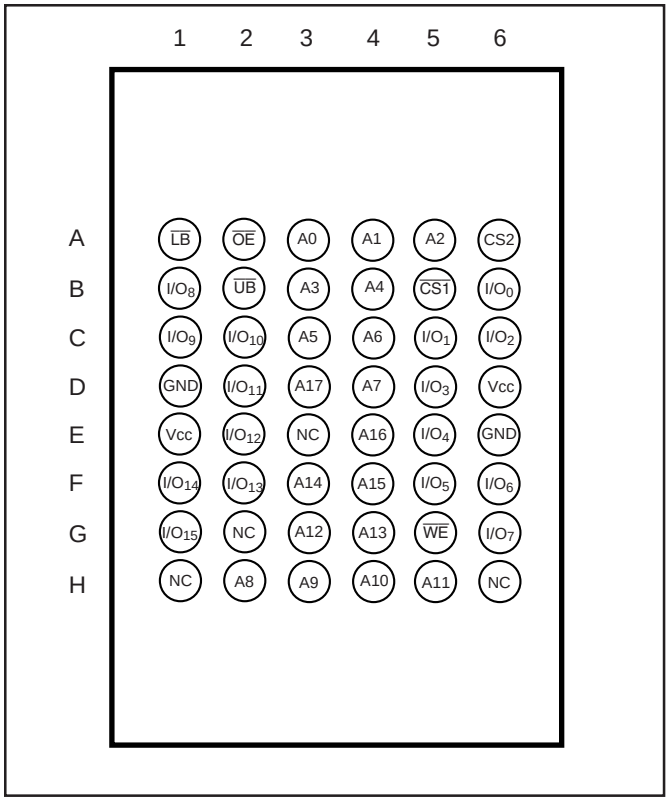


PIN CONFIGURATIONS

48-Pin mini BGA (6mm x 8mm) (Package Code B)



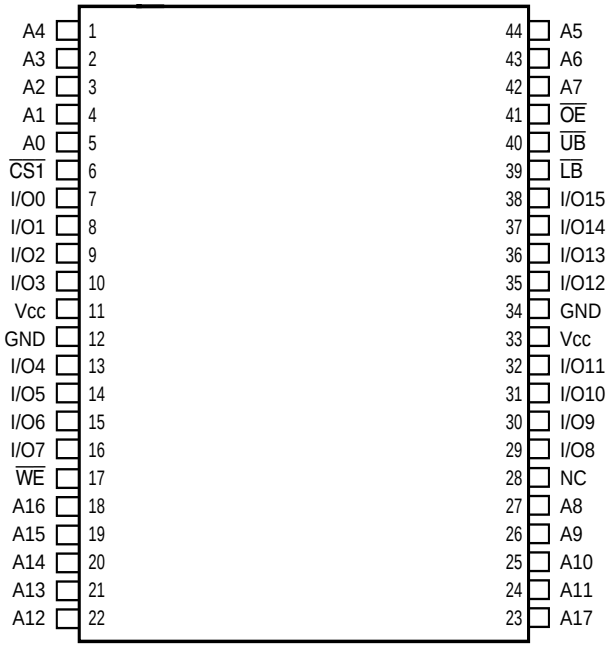
48-Pin mini BGA (6mm x 8mm) 2 CS Option (Package Code B2)



PIN DESCRIPTIONS

A0-A17	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CS1}$, CS2	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
Vcc	Power
GND	Ground

44-Pin mini TSOP (Type II) (Package Code T)



TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN I/O0-I/O7	I/O PIN I/O8-I/O15	Vcc Current
Not Selected	X	H	X	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
	X	X	L	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
	X	X	X	X	H	H	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	H	L	X	High-Z	High-Z	I_{CC}
	H	L	H	H	X	L	High-Z	High-Z	I_{CC}
Read	H	L	H	L	L	H	D_{OUT}	High-Z	I_{CC}
	H	L	H	L	H	L	High-Z	D_{OUT}	
	H	L	H	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	H	X	L	H	D_{IN}	High-Z	I_{CC}
	L	L	H	X	H	L	High-Z	D_{IN}	
	L	L	H	X	L	L	D_{IN}	D_{IN}	

OPERATING RANGE (Vcc)

Range	Ambient Temperature	IS62WV25616ALL	IS62WV25616BLL
Commercial	0°C to +70°C	1.65V - 2.2V	2.5V - 3.6V
Industrial	–40°C to +85°C	1.65V - 2.2V	2.5V - 3.6V

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.2 to Vcc+0.3	V
T_{BIAS}	Temperature Under Bias	–40 to +85	°C
V_{CC}	Vcc Related to GND	–0.2 to +3.8	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Vcc	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.65-2.2V	1.4	—	V
		I_{OH} = -1 mA	2.5-3.6V	2.2	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	1.65-2.2V	—	0.2	V
		I_{OL} = 2.1 mA	2.5-3.6V	—	0.4	V
V_{IH}	Input HIGH Voltage		1.65-2.2V	1.4	V_{CC} + 0.2	V
			2.5-3.6V	2.2	V_{CC} + 0.3	V
V_{IL}(1)	Input LOW Voltage		1.65-2.2V	–0.2	0.4	V
			2.5-3.6V	–0.2	0.6	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}		–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}, Outputs Disabled		–1	1	µA

Notes:
1. V_{IL} (min.) = –1.0V for pulse width less than 10 ns.

CAPACITANCE(1)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	10	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

IS62WV25616ALL, POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 55	Max. 70	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com.	30	25	mA
			Ind.	35	30	
I_{CC1}	Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = 0	Com.	5	5	mA
			Ind.	5	5	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IH}, CS2 = V_{IL}, f = 1 MHz	Com.	0.3	0.3	mA
			Ind.	0.3	0.3	
		OR				
	ULB Control	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IL}, f = 0, $\overline{UB}$ = V_{IH}, $\overline{LB}$ = V_{IH}				
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., $\overline{CS1} \geq V_{CC} - 0.2V$, CS2 $\leq$ 0.2V, $V_{IN} \geq V_{CC} - 0.2V$, or $V_{IN} \leq 0.2V$, f = 0	Com.	15	15	µA
			Ind.	15	15	
		OR				
	ULB Control	V_{CC} = Max., $\overline{CS1}$ = V_{IL}, CS2 = V_{IH} $V_{IN} \leq 0.2V$, f = 0; $\overline{UB}$/$\overline{LB}$ = $V_{CC} - 0.2V$				

IS62WV25616BLL, POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 55	Max. 70	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com.	45	40	mA
			Ind.	50	45	
I_{CC1}	Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = 0	Com.	5	5	mA
			Ind.	5	5	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IH}, CS2 = V_{IL}, f = 1 MHz	Com.	0.3	0.3	mA
			Ind.	0.3	0.3	
	OR					
	ULB Control	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IL}, f = 0, $\overline{UB}$ = V_{IH}, $\overline{LB}$ = V_{IH}				
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., $\overline{CS1} \geq V_{CC} - 0.2V$, CS2 $\leq$ 0.2V, $V_{IN} \geq V_{CC} - 0.2V$, or $V_{IN} \leq 0.2V$, f = 0	Com.	15	15	µA
			Ind.	15	15	
	OR					
	ULB Control	V_{CC} = Max., $\overline{CS1}$ = V_{IL}, CS2 = V_{IH} $V_{IN} \leq 0.2V$, f = 0; $\overline{UB}$/$\overline{LB}$ = $V_{CC} - 0.2V$				

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

AC TEST CONDITIONS

Parameter	62WV25616ALL (Unit)	62WV25616BLL (Unit)
Input Pulse Level	0.4V to Vcc-0.2	0.4 to 2.2V
Input Rise and Fall Times	5 ns	5ns
Input and Output Timing and Reference Level	V_{REF}	V_{REF}
Output Load	See Figures 1 and 2	See Figures 1 and 2

AC TEST LOADS

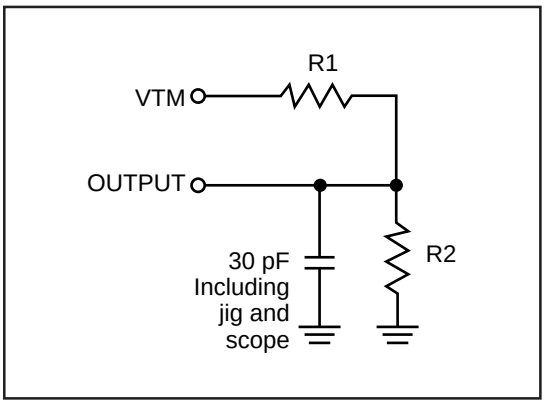


Figure 1

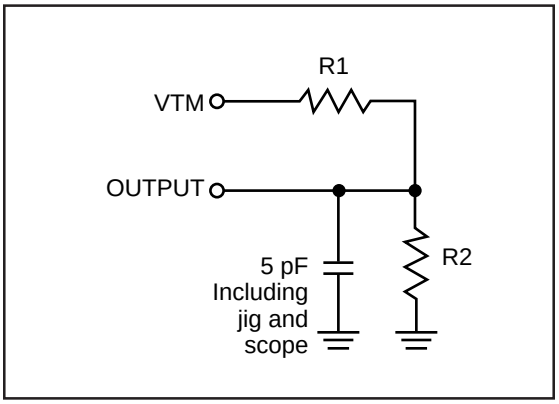


Figure 2

	1.65-2.2V	2.5V - 3.6V
R1(Ω)	3070	3070
R2(Ω)	3150	3150
V_{REF}	0.9V	1.5V
V_{TM}	1.8V	2.8V

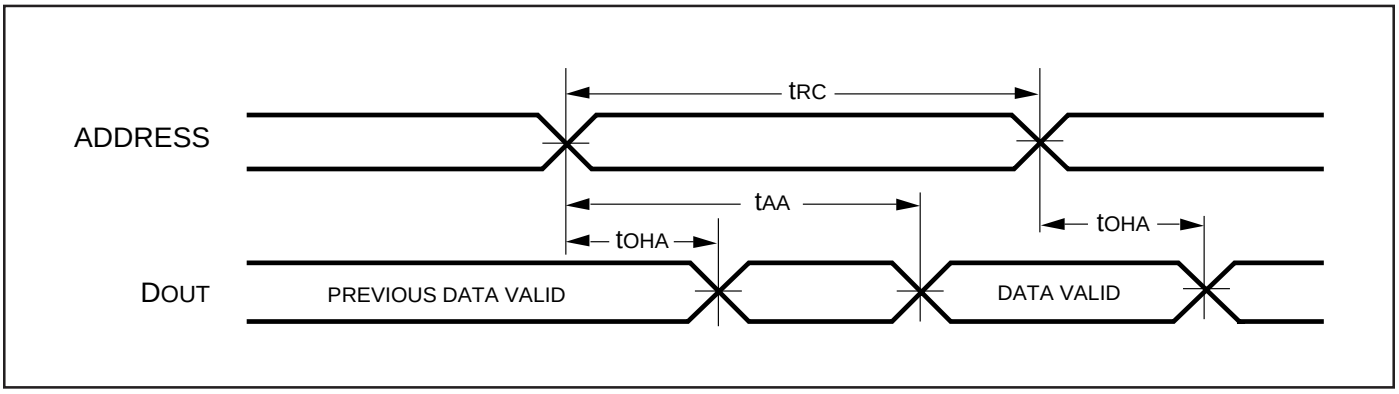
READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	55 ns Min.	55 ns Max.	70 ns Min.	70 ns Max.	Unit
t_{RC}	Read Cycle Time	55	—	70	—	ns
t_{AA}	Address Access Time	—	55	—	70	ns
t_{OHA}	Output Hold Time	10	—	10	—	ns
t_{ACS1}/t_{ACS2}	$\overline{CS1}$/CS2 Access Time	—	55	—	70	ns
t_{DOE}	$\overline{OE}$ Access Time	—	25	—	35	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	20	—	25	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	5	—	5	—	ns
t_{HZCS1}/t_{HZCS2}[2]	$\overline{CS1}$/CS2 to High-Z Output	0	20	0	25	ns
t_{LZCS1}/t_{LZCS2}[2]	$\overline{CS1}$/CS2 to Low-Z Output	10	—	10	—	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	55	—	70	ns
t_{HZB}	$\overline{LB}$, $\overline{UB}$ to High-Z Output	0	20	0	25	ns
t_{LZB}	$\overline{LB}$, $\overline{UB}$ to Low-Z Output	0	—	0	—	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V, input pulse levels of 0.4 to 1.4V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

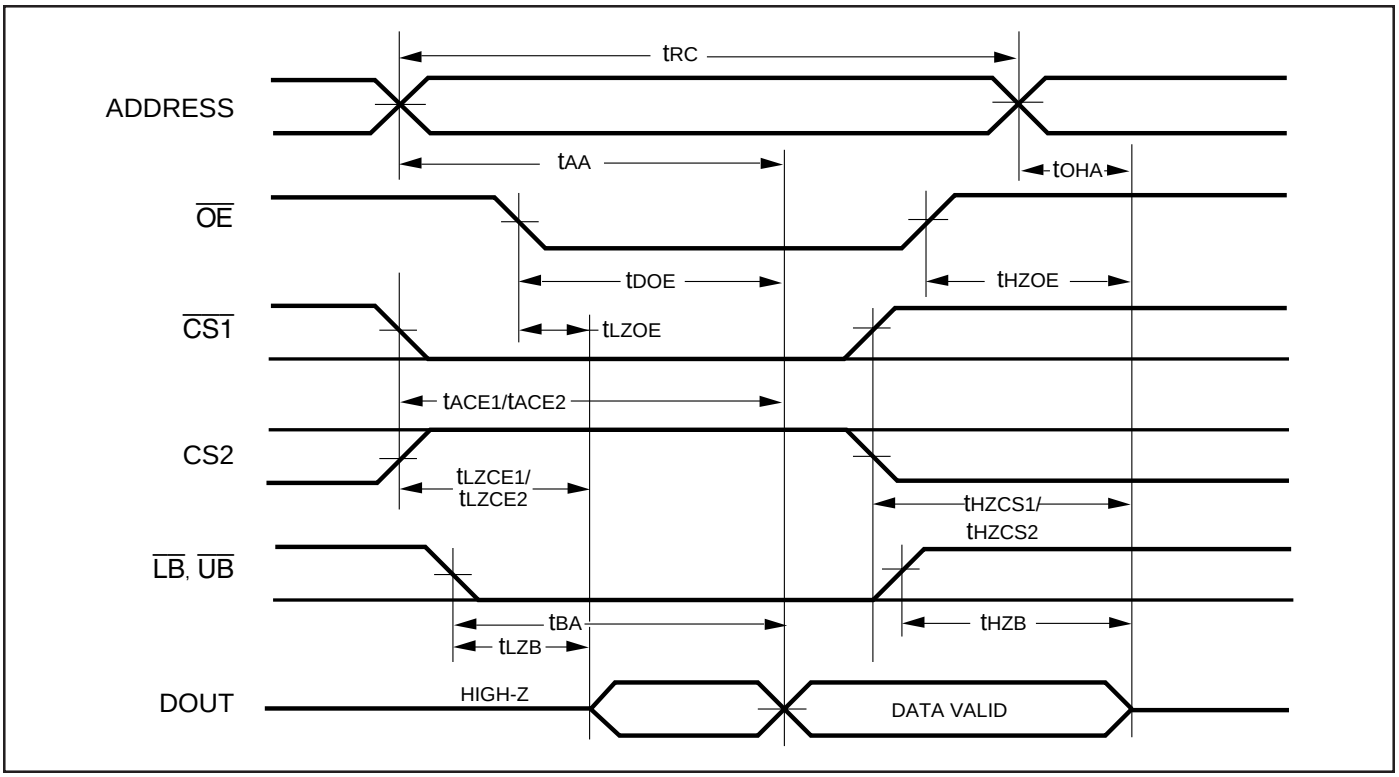
AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CS1}$ = $\overline{OE}$ = V_{IL}, $\overline{CS2}$ = $\overline{WE}$ = V_{IH}, $\overline{UB}$ or $\overline{LB}$ = V_{IL})



AC WAVEFORMS

READ CYCLE NO. 2[1,3] ($\overline{CS1}$, $\overline{CS2}$, $\overline{OE}$, AND $\overline{UB}$/$\overline{LB}$ Controlled)



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CS1}$, $\overline{UB}$, or $\overline{LB}$ = V_{IL}. CS2=$\overline{WE}$=V_{IH}.
3. Address is valid prior to or coincident with $\overline{CS1}$ LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

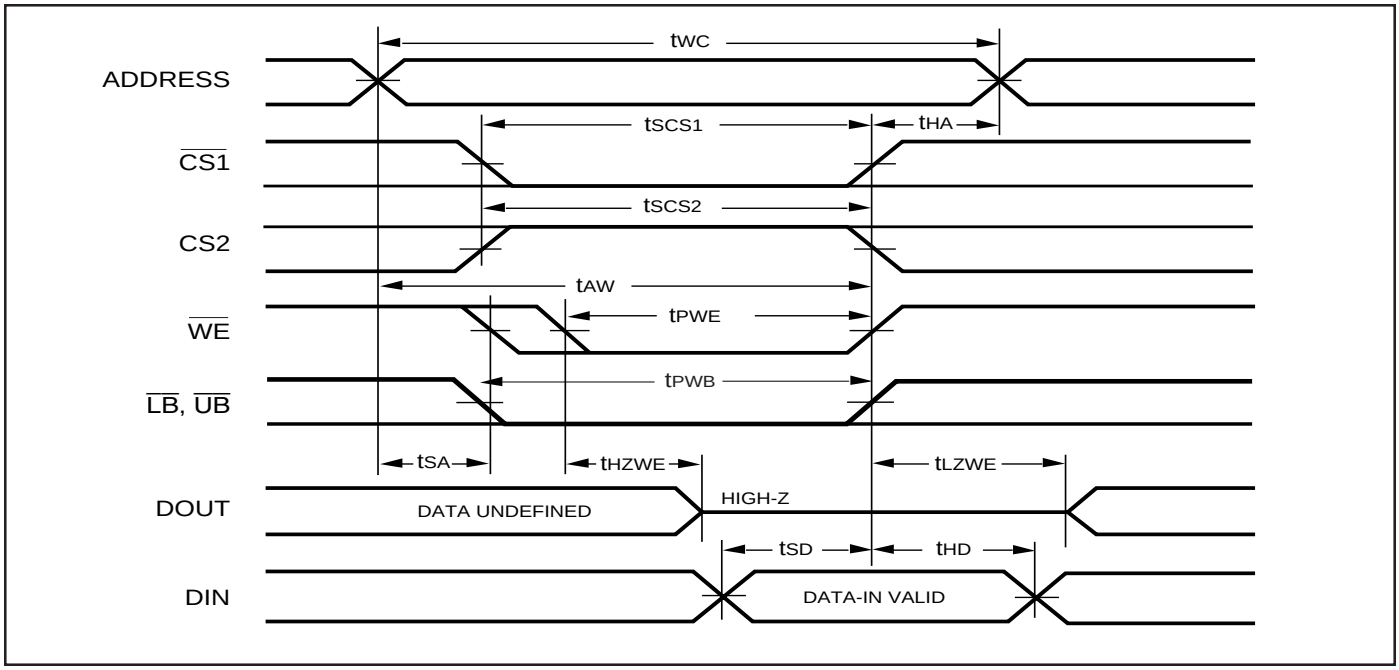
Symbol	Parameter	55 ns Min.	55 ns Max.	70 ns Min.	70 ns Max.	Unit
t_{WC}	Write Cycle Time	55	—	70	—	ns
t_{SCS1}/t_{SCS2}	$\overline{CS1}$/CS2 to Write End	45	—	60	—	ns
t_{AW}	Address Setup Time to Write End	45	—	60	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	45	—	60	—	ns
t_{PWE}	$\overline{WE}$ Pulse Width	40	—	50	—	ns
t_{SD}	Data Setup to Write End	25	—	30	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	20	—	20	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V, input pulse levels of 0.4V to 1.4V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CS1}$ LOW, CS2 HIGH and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

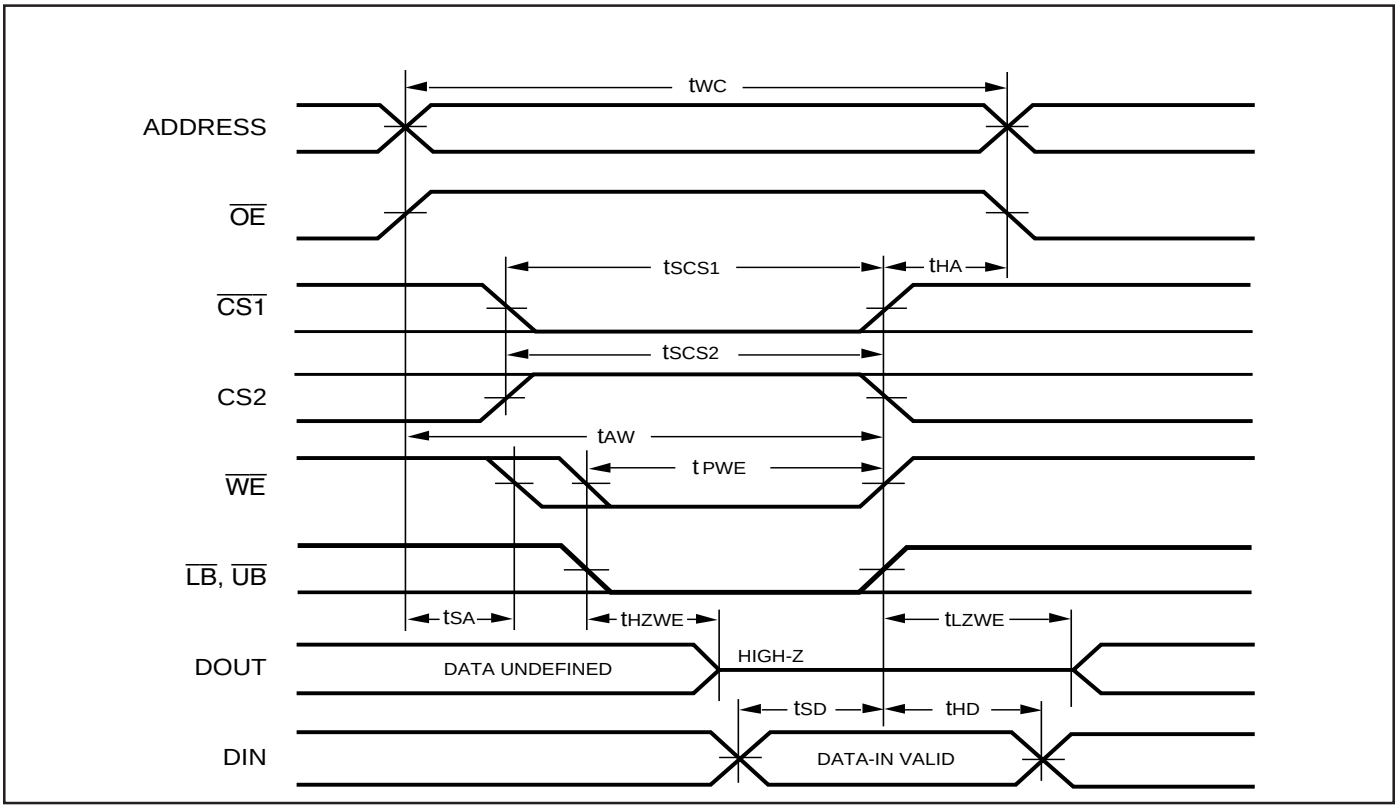
WRITE CYCLE NO. 1[1,2] ($\overline{CS1}$ Controlled, $\overline{OE}$ = HIGH or LOW)



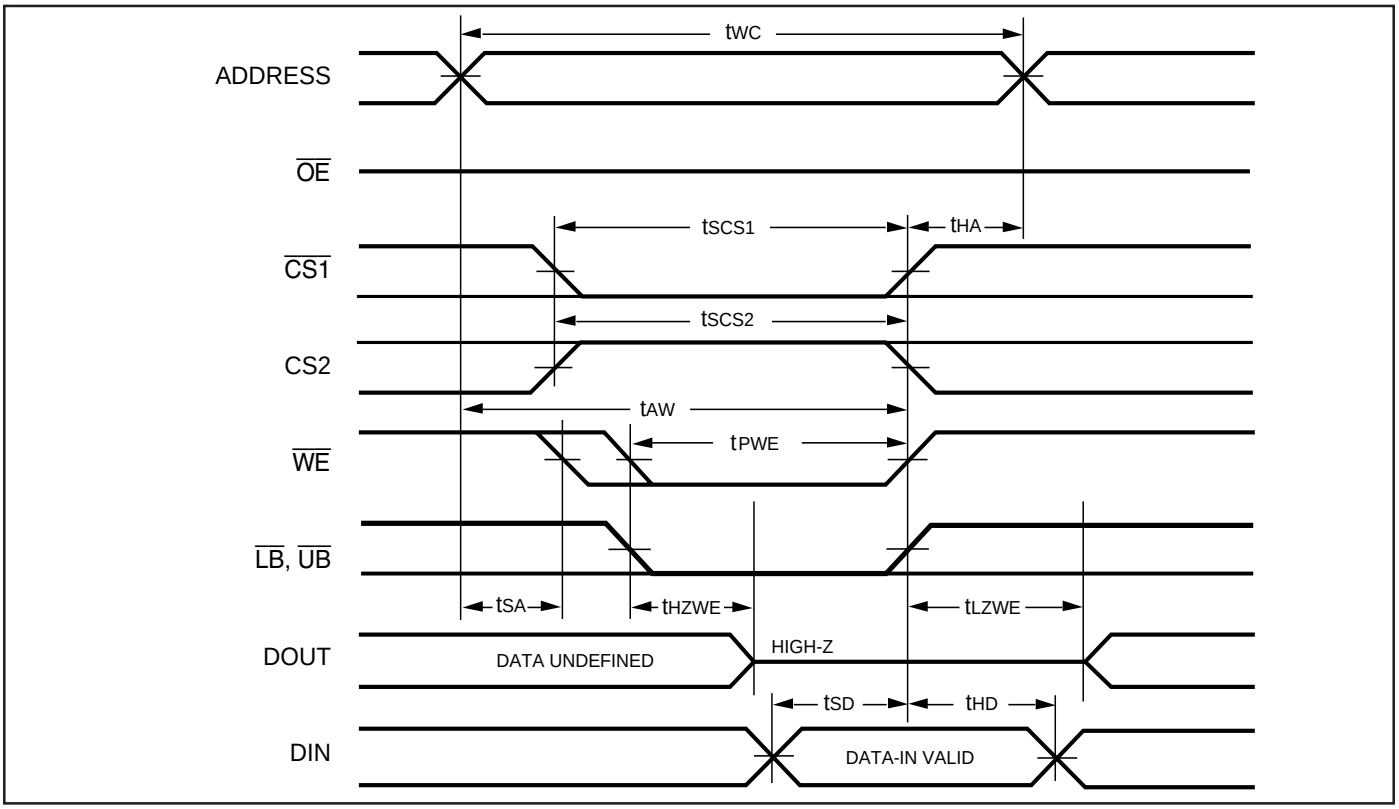
Notes:

1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CS1}$, CS2 and $\overline{WE}$ inputs and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.
2. WRITE = ($\overline{CS1}$) [($\overline{LB}$) = ($\overline{UB}$)] ($\overline{WE}$).

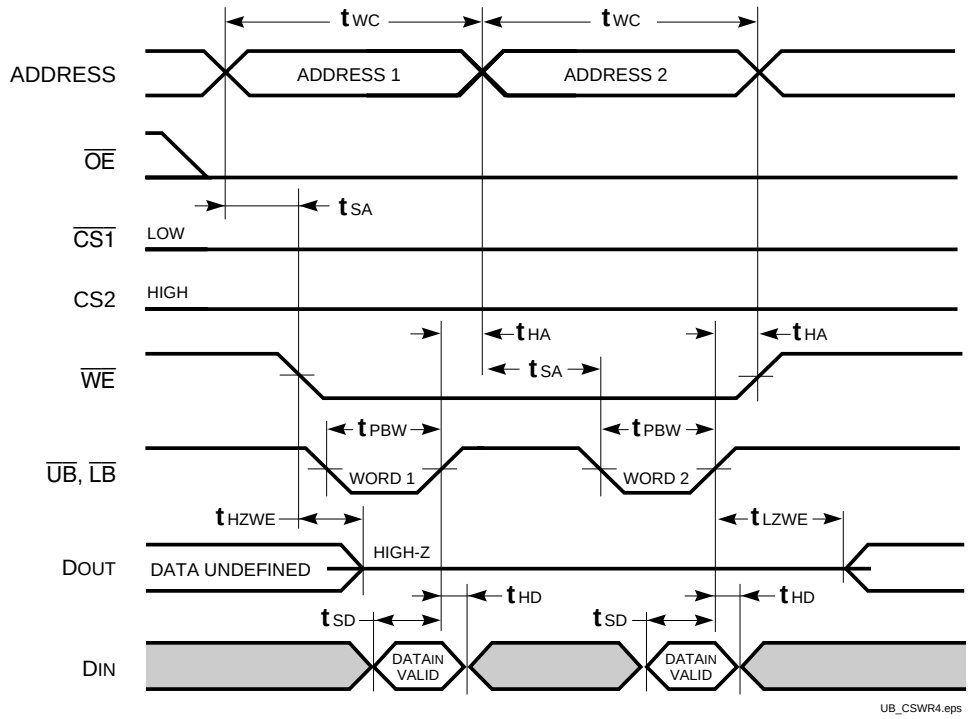
WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)



WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



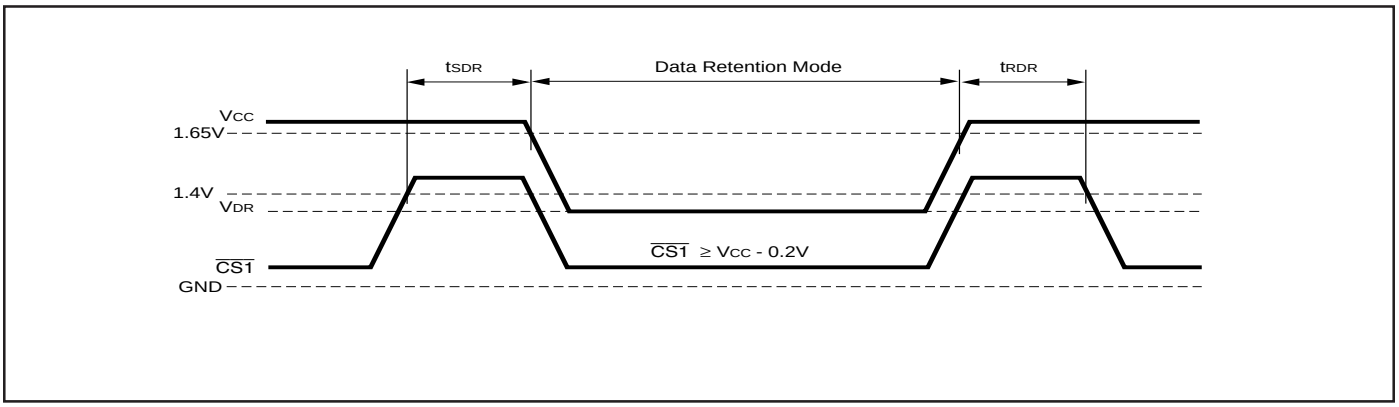
WRITE CYCLE NO. 4 ($\overline{UB}$/$\overline{LB}$ Controlled)



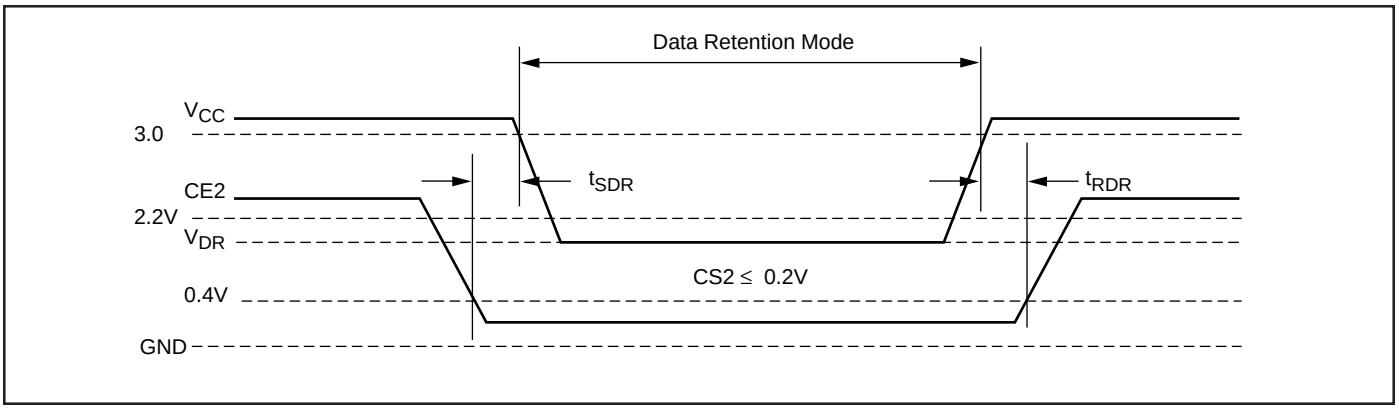
DATA RETENTION SWITCHING CHARACTERISTICS (LL)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V_{DR}	Vcc for Data Retention	See Data Retention Waveform	1.0	3.6	V
I_{DR}	Data Retention Current	Vcc = 1.0V, $\overline{CS1} \geq$ Vcc – 0.2V	—	15	µA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}	—	ns

DATA RETENTION WAVEFORM ($\overline{CS1}$ Controlled)



DATA RETENTION WAVEFORM (CS2 Controlled)



ORDERING INFORMATION

IS62WV25616ALL (1.65V - 2.2V)

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
70	IS62WV25616ALL-70T	TSOP
70	IS62WV25616ALL-70B	mini BGA (6mm x 8mm)
70	IS62WV25616ALL-70B2	mini BGA (6mm x 8mm), 2 CS Option

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
70	IS62WV25616ALL-70TI	TSOP
70	IS62WV25616ALL-70BI	mini BGA (6mm x 8mm)
70	IS62WV25616ALL-70B2I	mini BGA (6mm x 8mm), 2 CS Option

ORDERING INFORMATION

IS62WV25616BLL (2.5V - 3.6V)

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
55	IS62WV25616BLL-55T	TSOP
55	IS62WV25616BLL-55B	mini BGA (6mm x 8mm)
55	IS62WV25616BLL-55B2	mini BGA (6mm x 8mm), 2 CS Option
70	IS62WV25616BLL-70T	TSOP
70	IS62WV25616BLL-70B	mini BGA (6mm x 8mm)
70	IS62WV25616BLL-70B2	mini BGA (6mm x 8mm), 2 CS Option

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IS62WV25616BLL-55TI	TSOP
55	IS62WV25616BLL-55BI	mini BGA (6mm x 8mm)
55	IS62WV25616BLL-55B2I	mini BGA (6mm x 8mm), 2 CS Option
70	IS62WV25616BLL-70TI	TSOP
70	IS62WV25616BLL-70BI	mini BGA (6mm x 8mm)
70	IS62WV25616BLL-70B2I	mini BGA (6mm x 8mm), 2 CS Option

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