INTEGRATED TECHNOLOGY EXPRESS, INC.

IT7020C / IT7020H

Durable High-Voltage 240-Channel Common Driver for Dot-Matrix STN LCD

Preliminary Specification V0.4

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Revision History

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CONTENTS

FIGURES

TABLES

1. Features

- **Supports up to 1/240 display duty**
- **Supports 43V LCD drive voltage at maximum**
- **Supports 3.0 to 5.5V operating voltage**
- **Provides 240 LCD drive circuit**
- **Provides built-in power circuit for generating –21.5 V**
- **Provides the intermediate voltage interface**
- **Provides 3 selections of output modes:**
  - 240-output mode
  - 200-output mode
  - 160-output mode
- **Built-in alternating signal generation circuit (programmable through the MWS0 – MWS4 pins) is provided to restrain crosstalk**
- **Supports the display-off function**
- **Package**
  - Flex TCP
  - can also be shipped in bare chip

2. General Description

The IT7020 features a high-voltage common driver, which consists of 240 channels. The IT7020 can drive a dot matrix STN LCD panel, and has been designed specifically to meet the LCD requirement in PDA devices. It can be used in conjunction with the segment drivers: IT7010 or IT7012C.

In terms of power consumption, the device is able to reduce the required voltage level and power consumption considerably. Additionally, the built-in screen display off function supported in the device can also help to reduce the overall power consumption while the LCD panel is not actively in use. In logic portion, the IT7020 operates with a low 3V logic drive voltage to help reducing power consumption.

The device can generate a high voltage drive of +21.5V and –21.5V through a 43V high voltage CMOS process technology. By the built-in power circuit and external capacity, the generation of –21.5V will occur from +21.5V.

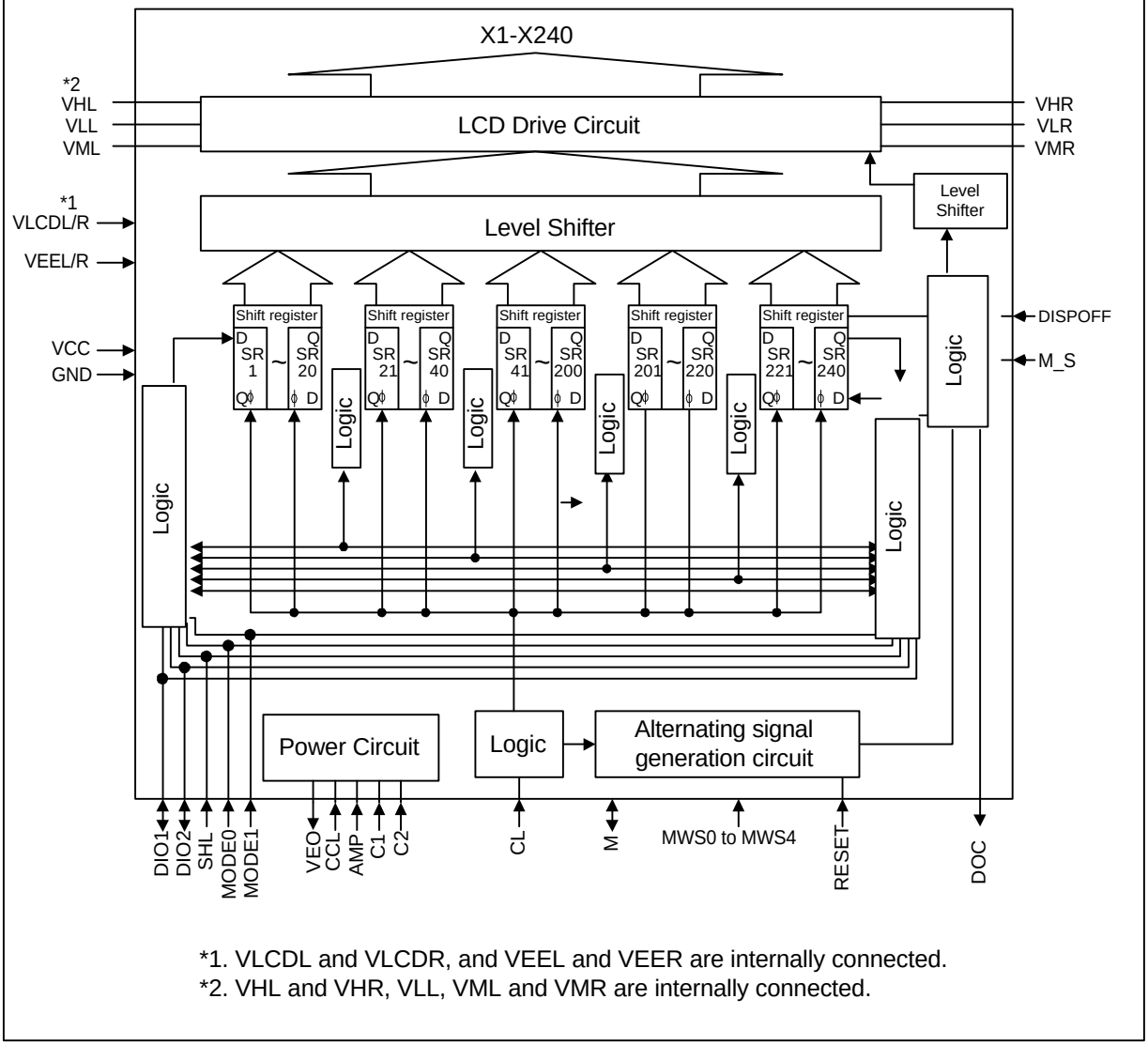
In addition, users are allowed the selection of 240-, 200- and 160-channel output mode by conveniently changing the mode according to what panel resolution they have.

In addition to the bare-chip package, the IT7020 is also available in 273-pin fine-pitch flex Tape-Carrier Package (TCP).

Moreover, ITE also provides users with complete local technical support. The company is dedicated to assisting customers in procuring multiple competitive edges, such as reducing development time, cost effectiveness and low power consumption for expanding the STN-LCD market share in a fast move.

ITE is committed to launching the LCD driver and controller series products, and will offer the most competitive solution through high integration and solid R&D expertise.

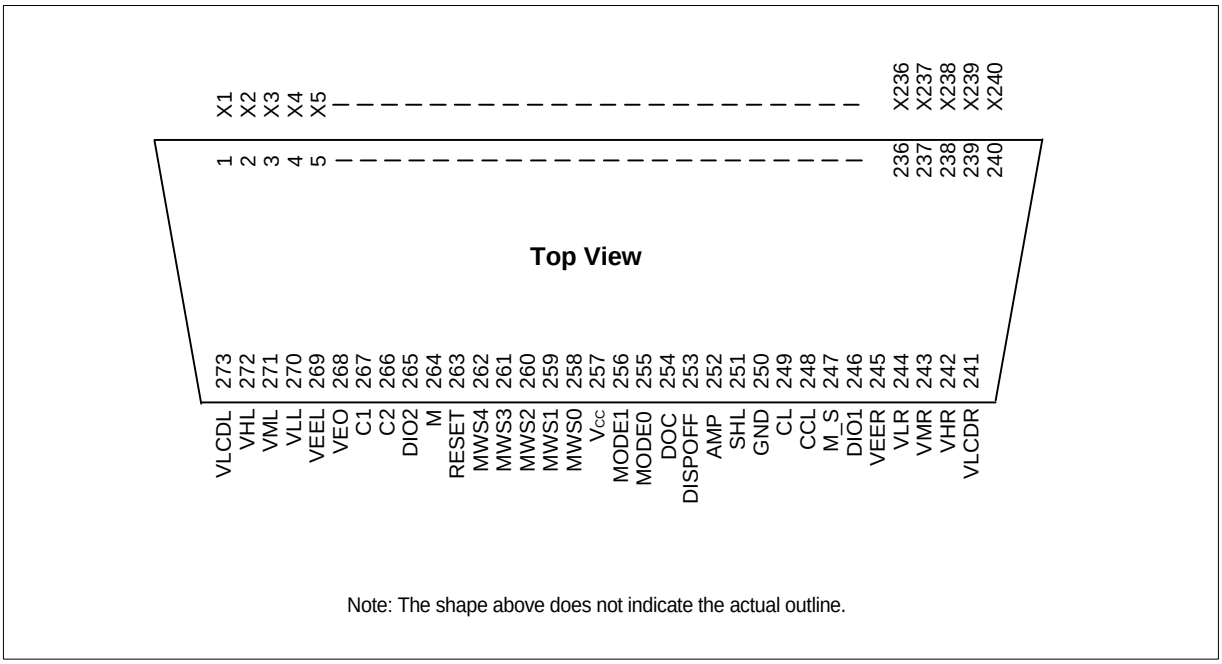
3. Block Diagram



*1. VLCDL and VLCDR, and VEEL and VEER are internally connected.
*2. VHL and VHR, VLL, VML and VMR are internally connected.

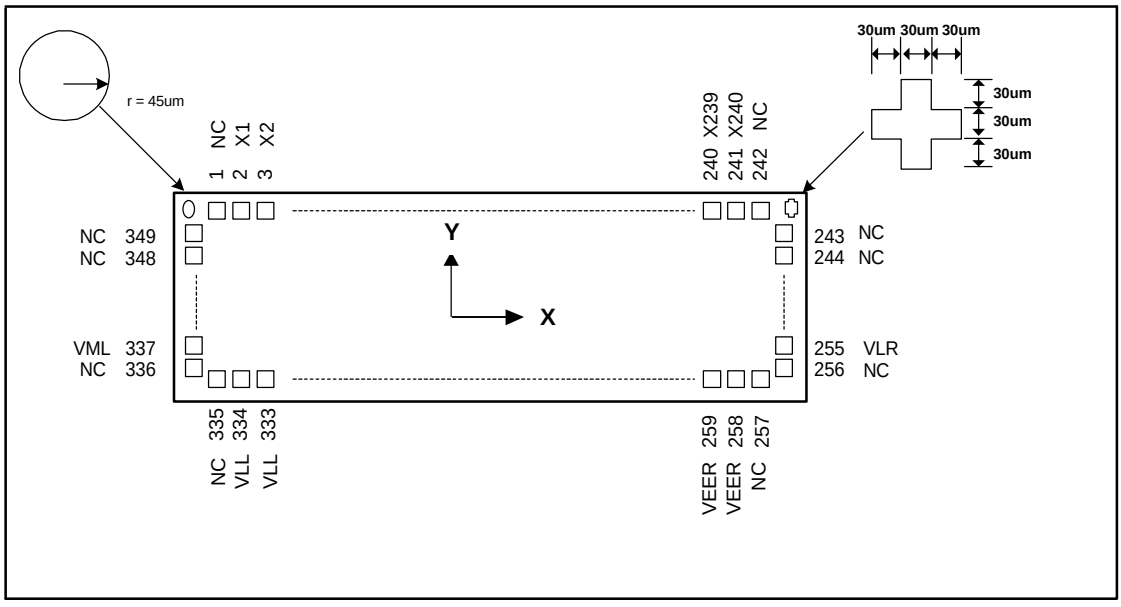
4. Pin Configuration

4.1 273-pin TCP



Note: The shape above does not indicate the actual outline.

4.2 Bare-chip Package



1. Chip size: 16565µm * 1520µm (excluding scribe line).
2. Coordinate: Bump center.
3. Origin: Chip center.
4. Chip window: (-8282.5, -760), (8282.5, 760).
5. Minimum bump pitch: 66µm
6. Chip thickness: 675um (typical)

Table 4-1. IT7020H Bump Name and Bump Size

Bump No.	Bump Name	Bump Size (Typical)		
		X (mm)	Y (mm)	h (mm)
1, 242, 257, 335	NC	58	65	18
2-241	X1 - X240	46	65	18
243, 256, 336, 349	NC	65	58	18
244, 245	NC	65	46	18
246 - 248	VLCDR	65	46	18
249 - 251	VHR	65	46	18
252, 253	VMR	65	46	18
254, 255	VLR	65	46	18
337 - 339	VML	65	46	18
340 - 342	VHL	65	46	18
343, 344	VLCDL	65	46	18
345 - 348	NC	65	46	18
*****	Other bumps	58	65	18

Table 4-2. IT7020H Align Mark Locations

Align Mark Type	Align Mark Center Coordinate		Align Mark Size or Diameter (mm)
	X (mm)	Y (mm)	
Cross	8192.2	673.7	90
Circle	-8191.45	673.7	90

Notes:

1. Dont connect any wires to NC bumps.

Table 4-3. Bump Center Coordinates (Unit: mm)

Bump No.	Bump Name	Coordinate X-axis	Coordinate Y-axis	Bump No.	Bump Name	Coordinate X-axis	Coordinate Y-axis	Bump No.	Bump Name	Coordinate X-axis	Coordinate Y-axis
1	NC	-7963	691.75	51	X50	-4653	691.75	101	X100	-1353	691.75
2	X1	-7887	691.75	52	X51	-4587	691.75	102	X101	-1287	691.75
3	X2	-7821	691.75	53	X52	-4521	691.75	103	X102	-1221	691.75
4	X3	-7755	691.75	54	X53	-4455	691.75	104	X103	-1155	691.75
5	X4	-7689	691.75	55	X54	-4389	691.75	105	X104	-1089	691.75
6	X5	-7623	691.75	56	X55	-4323	691.75	106	X105	-1023	691.75
7	X6	-7557	691.75	57	X56	-4257	691.75	107	X106	-957	691.75
8	X7	-7491	691.75	58	X57	-4191	691.75	108	X107	-891	691.75
9	X8	-7425	691.75	59	X58	-4125	691.75	109	X108	-825	691.75
10	X9	-7359	691.75	60	X59	-4059	691.75	110	X109	-759	691.75
11	X10	-7293	691.75	61	X60	-3993	691.75	111	X110	-693	691.75
12	X11	-7227	691.75	62	X61	-3927	691.75	112	X111	-627	691.75
13	X12	-7161	691.75	63	X62	-3861	691.75	113	X112	-561	691.75
14	X13	-7095	691.75	64	X63	-3795	691.75	114	X113	-495	691.75
15	X14	-7029	691.75	65	X64	-3729	691.75	115	X114	-429	691.75
16	X15	-6963	691.75	66	X65	-3663	691.75	116	X115	-363	691.75
17	X16	-6897	691.75	67	X66	-3597	691.75	117	X116	-297	691.75
18	X17	-6831	691.75	68	X67	-3531	691.75	118	X117	-231	691.75
19	X18	-6765	691.75	69	X68	-3465	691.75	119	X118	-165	691.75
20	X19	-6699	691.75	70	X69	-3399	691.75	120	X119	-99	691.75
21	X20	-6633	691.75	71	X70	-3333	691.75	121	X120	-33	691.75
22	X21	-6567	691.75	72	X71	-3267	691.75	122	X121	33	691.75
23	X22	-6501	691.75	73	X72	-3201	691.75	123	X122	99	691.75
24	X23	-6435	691.75	74	X73	-3135	691.75	124	X123	165	691.75
25	X24	-6369	691.75	75	X74	-3069	691.75	125	X124	231	691.75
26	X25	-6303	691.75	76	X75	-3003	691.75	126	X125	297	691.75
27	X26	-6237	691.75	77	X76	-2937	691.75	127	X126	363	691.75
28	X27	-6171	691.75	78	X77	-2871	691.75	128	X127	429	691.75
29	X28	-6105	691.75	79	X78	-2805	691.75	129	X128	495	691.75
30	X29	-6039	691.75	80	X79	-2739	691.75	130	X129	561	691.75
31	X30	-5973	691.75	81	X80	-2673	691.75	131	X130	627	691.75
32	X31	-5907	691.75	82	X81	-2607	691.75	132	X131	693	691.75
33	X32	-5841	691.75	83	X82	-2541	691.75	133	X132	759	691.75
34	X33	-5775	691.75	84	X83	-2475	691.75	134	X133	825	691.75
35	X34	-5709	691.75	85	X84	-2409	691.75	135	X134	891	691.75
36	X35	-5643	691.75	86	X85	-2343	691.75	136	X135	957	691.75
37	X36	-5577	691.75	87	X86	-2277	691.75	137	X136	1023	691.75
38	X37	-5511	691.75	88	X87	-2211	691.75	138	X137	1089	691.75
39	X38	-5445	691.75	89	X88	-2145	691.75	139	X138	1155	691.75
40	X39	-5379	691.75	90	X89	-2079	691.75	140	X139	1221	691.75
41	X40	-5313	691.75	91	X90	-2013	691.75	141	X140	1287	691.75
42	X41	-5247	691.75	92	X91	-1947	691.75	142	X141	1353	691.75
43	X42	-5181	691.75	93	X92	-1881	691.75	143	X142	1419	691.75
44	X43	-5115	691.75	94	X93	-1815	691.75	144	X143	1485	691.75
45	X44	-5049	691.75	95	X94	-1749	691.75	145	X144	1551	691.75
46	X45	-4983	691.75	96	X95	-1683	691.75	146	X145	1617	691.75
47	X46	-4917	691.75	97	X96	-1617	691.75	147	X146	1683	691.75
48	X47	-4851	691.75	98	X97	-1551	691.75	148	X147	1749	691.75
49	X48	-4785	691.75	99	X98	-1485	691.75	149	X148	1815	691.75
50	X49	-4719	691.75	100	X99	-1419	691.75	150	X149	1881	691.75

Table 4-3. Bump Center Coordinates (Unit: μm) [continued]

Bump No.	Bump Name	Coordinate X-axis	Coordinate Y-axis	Bump No.	Bump Name	Coordinate X-axis	Coordinate Y-axis	Bump No.	Bump Name	Coordinate X-axis	Coordinate Y-axis
151	X150	1947	691.75	201	X200	5247	691.75	251	VHR	8111	-25.45
152	X151	2013	691.75	202	X201	5313	691.75	252	VMR	8111	-91.45
153	X152	2079	691.75	203	X202	5379	691.75	253	VMR	8111	-157.45
154	X153	2145	691.75	204	X203	5445	691.75	254	VLR	8111	-223.45
155	X154	2211	691.75	205	X204	5511	691.75	255	VLR	8111	-289.45
156	X155	2277	691.75	206	X205	5577	691.75	256	NC	8111	-365.45
157	X156	2343	691.75	207	X206	5643	691.75	257	NC	7963	-616.65
158	X157	2409	691.75	208	X207	5709	691.75	258	VEER	7800	-616.65
159	X158	2475	691.75	209	X208	5775	691.75	259	VEER	7667.2	-616.65
160	X159	2541	691.75	210	X209	5841	691.75	260	VEER	7554.9	-616.65
161	X160	2607	691.75	211	X210	5907	691.75	261	DIO1	7176	-616.65
162	X161	2673	691.75	212	X211	5973	691.75	262	DIO1	7055.5	-616.65
163	X162	2739	691.75	213	X212	6039	691.75	263	M_S	6642.8	-616.65
164	X163	2805	691.75	214	X213	6105	691.75	264	M_S	6552	-616.65
165	X164	2871	691.75	215	X214	6171	691.75	265	M_S	6244.9	-616.65
166	X165	2937	691.75	216	X215	6237	691.75	266	CCL	6018.8	-616.65
167	X166	3003	691.75	217	X216	6303	691.75	267	CCL	5928	-616.65
168	X167	3069	691.75	218	X217	6369	691.75	268	CCL	5620.9	-616.65
169	X168	3135	691.75	219	X218	6435	691.75	269	CL	5394.8	-616.65
170	X169	3201	691.75	220	X219	6501	691.75	270	CL	5304	-616.65
171	X170	3267	691.75	221	X220	6567	691.75	271	CL	4996.9	-616.65
172	X171	3333	691.75	222	X221	6633	691.75	272	GND	4789	-616.65
173	X172	3399	691.75	223	X222	6699	691.75	273	GND	4680	-616.65
174	X173	3465	691.75	224	X223	6765	691.75	274	GND	4550.4	-616.65
175	X174	3531	691.75	225	X224	6831	691.75	275	GND	4417.6	-616.65
176	X175	3597	691.75	226	X225	6897	691.75	276	GND	4305.3	-616.65
177	X176	3663	691.75	227	X226	6963	691.75	277	GND	4193	-616.65
178	X177	3729	691.75	228	X227	7029	691.75	278	SHL	4008.3	-616.65
179	X178	3795	691.75	229	X228	7095	691.75	279	SHL	3898.4	-616.65
180	X179	3861	691.75	230	X229	7161	691.75	280	SHL	3807.6	-616.65
181	X180	3927	691.75	231	X230	7227	691.75	281	SHL	3500.5	-616.65
182	X181	3993	691.75	232	X231	7293	691.75	282	AMP	3384	-616.65
183	X182	4059	691.75	233	X232	7359	691.75	283	AMP	3293.2	-616.65
184	X183	4125	691.75	234	X233	7425	691.75	284	AMP	2986.1	-616.65
185	X184	4191	691.75	235	X234	7491	691.75	285	DISPOFF	2869.6	-616.65
186	X185	4257	691.75	236	X235	7557	691.75	286	DISPOFF	2778.8	-616.65
187	X186	4323	691.75	237	X236	7623	691.75	287	DISPOFF	2471.7	-616.65
188	X187	4389	691.75	238	X237	7689	691.75	288	DOC	2304.5	-616.65
189	X188	4455	691.75	239	X238	7755	691.75	289	DOC	2184	-616.65
190	X189	4521	691.75	240	X239	7821	691.75	290	MODE0	1770.2	-616.65
191	X190	4587	691.75	241	X240	7887	691.75	291	MODE0	1679.4	-616.65
192	X191	4653	691.75	242	NC	7963	691.75	292	MODE0	1372.3	-616.65
193	X192	4719	691.75	243	NC	8111	512.55	293	MODE1	1146.2	-616.65
194	X193	4785	691.75	244	NC	8111	436.55	294	MODE1	1055.4	-616.65
195	X194	4851	691.75	245	NC	8111	370.55	295	MODE1	748.3	-616.65
196	X195	4917	691.75	246	VLCDR	8111	304.55	296	Vcc	552.1	-616.65
197	X196	4983	691.75	247	VLCDR	8111	238.55	297	Vcc	443.1	-616.65
198	X197	5049	691.75	248	VLCDR	8111	172.55	298	Vcc	313.5	-616.65
199	X198	5115	691.75	249	VHR	8111	106.55	299	Vcc	180.7	-616.65
200	X199	5181	691.75	250	VHR	8111	40.55	300	Vcc	68.4	-616.65

Table 4-3. Bump Center Coordinates (Unit: mm) [continued]

Bump No.	Bump Name	Coordinate	
		X-axis	Y-axis
301	Vcc	-43.9	-616.65
302	MWS0	-221.2	-616.65
303	MWS0	-312	-616.65
304	MWS0	-619.1	-616.65
305	MWS1	-784.8	-616.65
306	MWS1	-875.6	-616.65
307	MWS1	-1182.7	-616.65
308	MWS2	-1408.8	-616.65
309	MWS2	-1499.6	-616.65
310	MWS2	-1806.7	-616.65
311	MWS3	-2032.8	-616.65
312	MWS3	-2123.6	-616.65
313	MWS3	-2430.7	-616.65
314	MWS4	-2597.8	-616.65
315	MWS4	-2688.6	-616.65
316	MWS4	-2995.7	-616.65
317	RESET	-3177.1	-616.65
318	RESET	-3267.9	-616.65
319	RESET	-3575	-616.65
320	M	-3941.5	-616.65
321	M	-4062	-616.65
322	DIO2	-4680	-616.65
323	DIO2	-4800.5	-616.65
324	C2	-5291	-616.65
325	C2	-5518.4	-616.65
326	C1	-5805.7	-616.65
327	C1	-6033.1	-616.65
328	VEO	-6296.8	-616.65
329	VEO	-6524.2	-616.65
330	VEEL	-6791.1	-616.65
331	VEEL	-7018.5	-616.65
332	VEEL	-7233.6	-616.65
333	VLL	-7520.1	-616.65
334	VLL	-7747.5	-616.65
335	NC	-7963	-616.65
336	NC	-8111	-365.45
337	VML	-8111	-289.45
338	VML	-8111	-223.45
339	VML	-8111	-157.45
340	VHL	-8111	-91.45
341	VHL	-8111	-25.45
342	VHL	-8111	40.55
343	VLCDL	-8111	106.55
344	VLCDL	-8111	172.55
345	NC	-8111	238.55
346	NC	-8111	304.55
347	NC	-8111	370.55
348	NC	-8111	436.55
349	NC	-8111	512.55

5. IT7020C/H Pin Descriptions

Table 5-1. Pin Descriptions of Power Signals

Pin(s) No.	Symbol	Attribute	Description
267, 266	**C1, C2**	-	Connect the external capacitance here when the power circuit is enabled for VEE generation. It is advisable that users should not connect any traces to these pins if the built-in power circuit is not used.
273, 241 **269, 245** **257, 250**	**VLCDL/R** **VEEL/R** **Vcc, GND**	-	VLCDL/R and VEEL/R are used to provide the power supply for the usage of LCD drive. VEEL/R are used to provide the power supply for the usage of power circuits. Vcc, GND are used to provide the power supply for the usage of logic circuits.
272, 242 **270, 244** **271, 243**	**VHL/R** **VLL/R** **VML/R**	Input	These pins are used to provide the power supply for LCD drive level. VHL/R and VLL/R indicate the selected level of LCD drive. Note that VHL/R is set to the same voltage as VLCDL/R while VLL/R is set to the same voltage as VEEL/R. VML/R indicates the non-selected LCD drive level. It provides the power supply for the built-in power circuits as well.
268	**VEO**	Output	Connect VEO pin to the VEEL/R pins when the built-in power circuit is enabled to generate VEE voltage. In this case, the VM voltage is used as the point of reference and the output voltage of VEO is equal to (2*VM – VLCD). Users are advised not to connect any lines to this pin if the built-in power circuit is not used.

Table 5-2. Pin Descriptions of Control Signals

Pin(s) No.	Symbol	Attribute	Description
252	**AMP**	Input	This signal is used to control the on and off states the built-in power circuit. When the circuit is used, this pin must be tied to Vcc. When the built-in power circuit is not used, this pin must be tied to GND.
248	**CCL**	Input	Indicates the built-in power circuit clock input. When the built-in power circuit is enabled and VEE is generated, this pin is connected to the CL pin. When the built-in power circuit is not used, CCL must be tied to GND.
249	**CL**	Input	***Shift Clock Input.*** Data is shifted and latched at the falling edge of CL in the shift register.
246 **265**	**DIO1** **DIO2**	Input/ Output	***Serial Data Input/Output Pin.*** When the SHL is high, the DIO1 is the serial output pin and DIO2 is the serial input pin. When the SHL is low, the DIO1 is the serial input pin and DIO2 is the serial output pin.

Table 5-2. Pin Descriptions of Control Signals (continued)

<table>
<tr><th>Pin(s) No.</th><th>Symbol</th><th>Attribute</th><th>Description</th></tr>
<tr><td>253</td><td>DISPOFF</td><td>Input</td><td>Set LCD drive outputs of X1 to X240 to the VM level by connecting this pin to GND.</td></tr>
<tr><td>254</td><td>DOC</td><td>Output</td><td>When the M_S pin is set to high level, the output level of DOC pin is the same as the DISPOFF pin.
When the M_S pin is set to low level, DOC pin outputs low level until serial data input 16 times. See Figure 5-1 for more details.
Note that when M_S is set to low level, the DOC pin should be connected to IT7010C DOF_N control pin.</td></tr>
<tr><td>264</td><td>M</td><td>Input/Output</td><td>Input or output the toggling waveform for LCD drive output level.</td></tr>
<tr><td>247</td><td>M_S</td><td>Input</td><td>Control the LCD display-off function and determine the LCD display-off signal to output from DOC pin.
When the M_S is set to high level and the DISPOFF is low level, X1-X240 pins will set to the VM level.
When the M_S is set to low level, the X1-X240 pins will stay on the VM level until serial data input 16 times (See Figure 5-1).</td></tr>
<tr><td>255
256</td><td>MODE0
MODE1</td><td>Input</td><td>Input terminals for specifying the effective number of LCD drive output pins.
<table>
<tr><th>MODE0</th><th>MODE1</th><th>Shift Direction</th></tr>
<tr><td>“H”</td><td>“H”</td><td>240-output (X1, X2, X3…X238, X239, X240)</td></tr>
<tr><td>“H”</td><td>“L”</td><td>200-output (X21, X22, X23…X218, X219, X220)</td></tr>
<tr><td>“L”</td><td>“H”</td><td>160-output (X41, X42, X43…X198, X199, X200)</td></tr>
<tr><td>“L”</td><td>“L”</td><td>Undefined. Use at your own risk!</td></tr>
</table></td></tr>
<tr><td>258
259
260
261
262</td><td>MWS0
MWS1
MWS2
MWS3
MWS4</td><td>Input</td><td>These pins are used to specify the frequency of the toggling signal (M signal) in the unit of number of display lines. The number of display lines is an integer ranging from 2 to 31 and is specified in the table below. Typically, the number of display lines ranges from 10 to 31.
If IT7020 is configured in the slave mode, i.e., driven by an external M signal, MWS0 – MWS4 should be tied to low level.
<table>
<tr><th>Number of lines</th><th>MWS 4</th><th>MWS 3</th><th>MWS 2</th><th>MWS 1</th><th>MWS 0</th><th>Line toggling waveform</th><th>M-pin status</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>-</td><td>Input</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Prohibited</td><td rowspan="5">Output</td></tr>
<tr><td>2</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2 lines alternated</td></tr>
<tr><td>3</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>3 lines alternated</td></tr>
<tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr>
<tr><td>31</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>31 lines alternated</td></tr>
</table></td></tr>
<tr><td>263</td><td>RESET</td><td>Input</td><td>Initialize the toggling signal (M signal) circuit by connecting this pin to GND. Tied to Vcc for normal operation.</td></tr>
</table>

Table 5-2. Pin Descriptions of Control Signals (continued)

Pin(s) No.	Symbol	Attribute	Description
251	**SHL**	Input	***This pin is used to switch the shift directions.***

SHL	MODE0	MODE1	Shift Direction
			Right shift
"H" level	"H"	"H"	DIO2→SR1…SR240→DIO1
	"H"	"L"	DIO2→SR21…SR220→DIO1
	"H"	"H"	DIO2→SR41…SR200→DIO1
			Left shift
"L" level	"H"	"H"	DIO1→SR240…SR1→DIO2
	"H"	"L"	DIO1→SR220…SR21→DIO2
	"L"	"H"	DIO1→SR200…SR41→DIO2

SR1, SR2...SR240 are the outputs of the shift registers and correspond to X1, X2...X240.
Note: The 40 or 80 pins, which are invalidated at the 200 or 160-output mode, will output the non-selected level (VM).

Table 5-3. Pin Descriptions of LCD Drive Output Signals

Pin(s) No.	Symbol	Attribute	Description
1 to 240	**X1 to X240**	Output	***LCD Drive Output.*** When DISPOFF is set to Vcc, the output level of X1 – X240 are determined by the combination of the display data and the M signal. Either one of VH, VL, or VM is selected and then transmitted to the output circuit. See Figure 5-2 for more details.

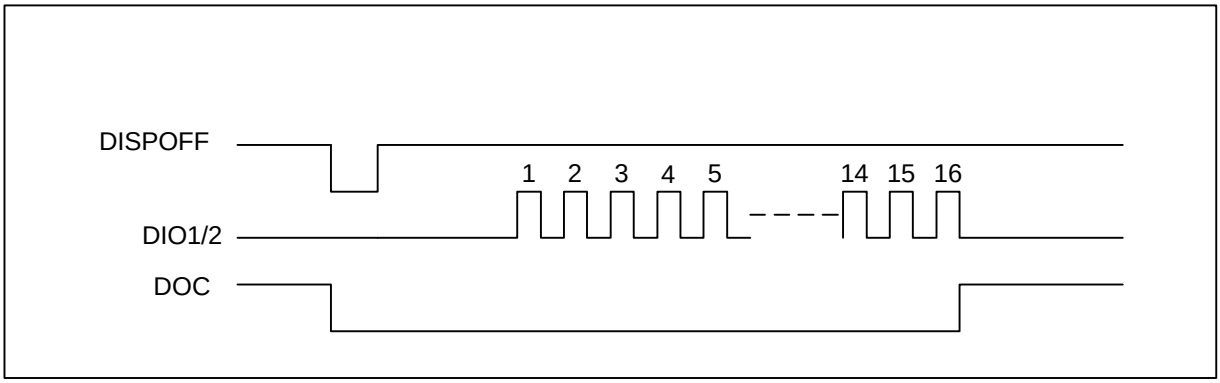


Figure 5-1. DOC Waveform

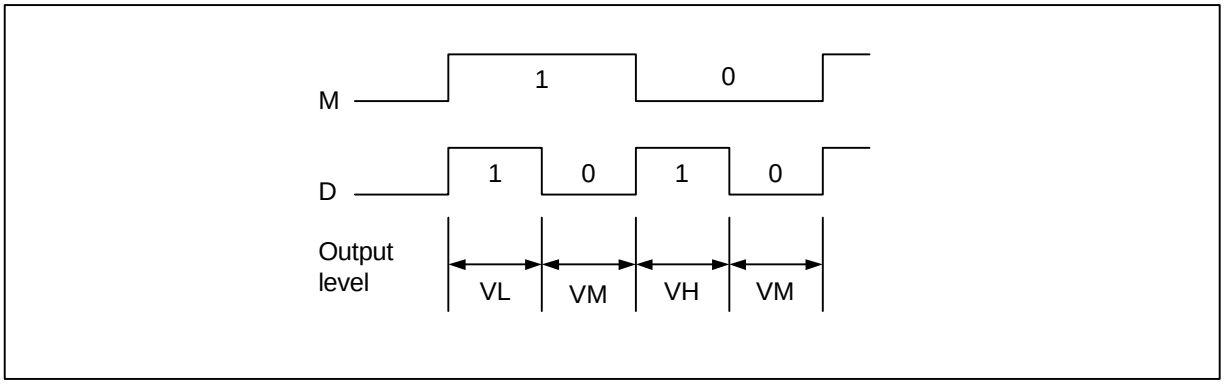


Figure 5-2. LCD Driver Terminal Output Voltage Level

6. System Configuration

6.1 Overview

The IT7020 is composed of 4 main elements to work properly: LCD Drive Circuits, Level Shifter, Shift Register Circuit, and Alternating Signal Generation Circuits. The functional descriptions for each of the 4 elements are described below:

6.2 LCD Drive Circuit

The device consists of 240 LCD drive circuits, and each of the LCD drive circuit is responsible to select and output the three level signals for the LCD drive. Either one of VH, VL and VM will be selected and transmitted to the output circuit by combining the data in the shift register and M signal together. The level shifter is responsible for boosting a 5V signal to the high voltage for LCD drive.

6.3 Shift Register Circuit

The shift register circuit is made up of 240 bits and is bi-directional. Through the shift register circuit, the first line marker signal can be generated from the DIO1 pin and DIO2 pin. The first line marker signal can be then sequentially shifted via the shift clock CL. The shifting direction is determined by SHL pin.

6.4 Alternating Signal (M) Generation Circuit

The alternating Signal Generation circuit is used to generate an alternating signal (M signal) for proper LCD display. To restrain the crosstalk function, the signal is alternated from several lines to a host of lines. If pins MWS0 to MWS4 are connected to Vcc or GND, the intended number of signals can be alternated. Note that the connection of pins MWS0 to MWS4 with GND can be done when the alternating signals are input externally.

7. Terminal Configuration

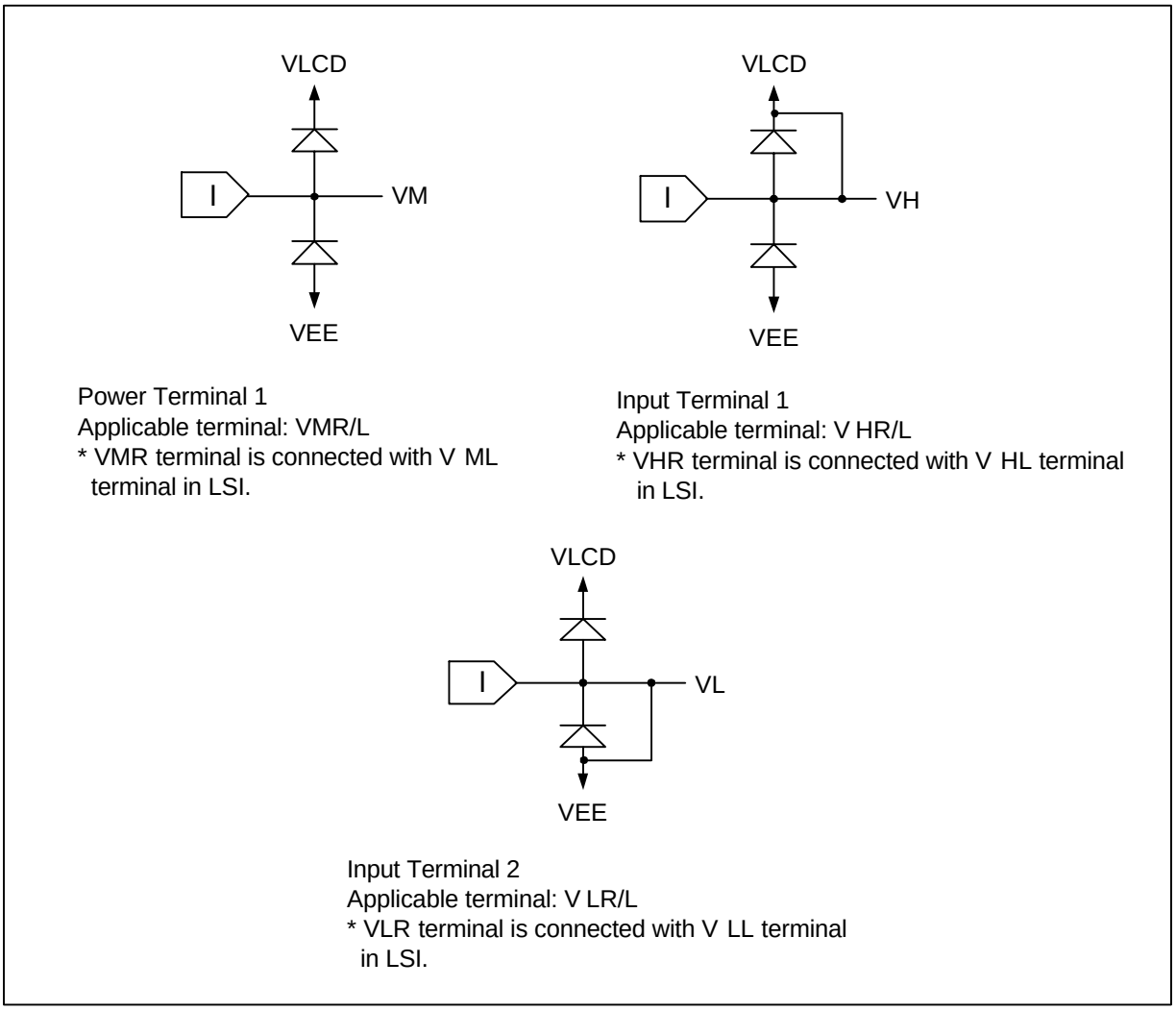


Figure 7-1. IT7020 Power and Input Terminal Configuration

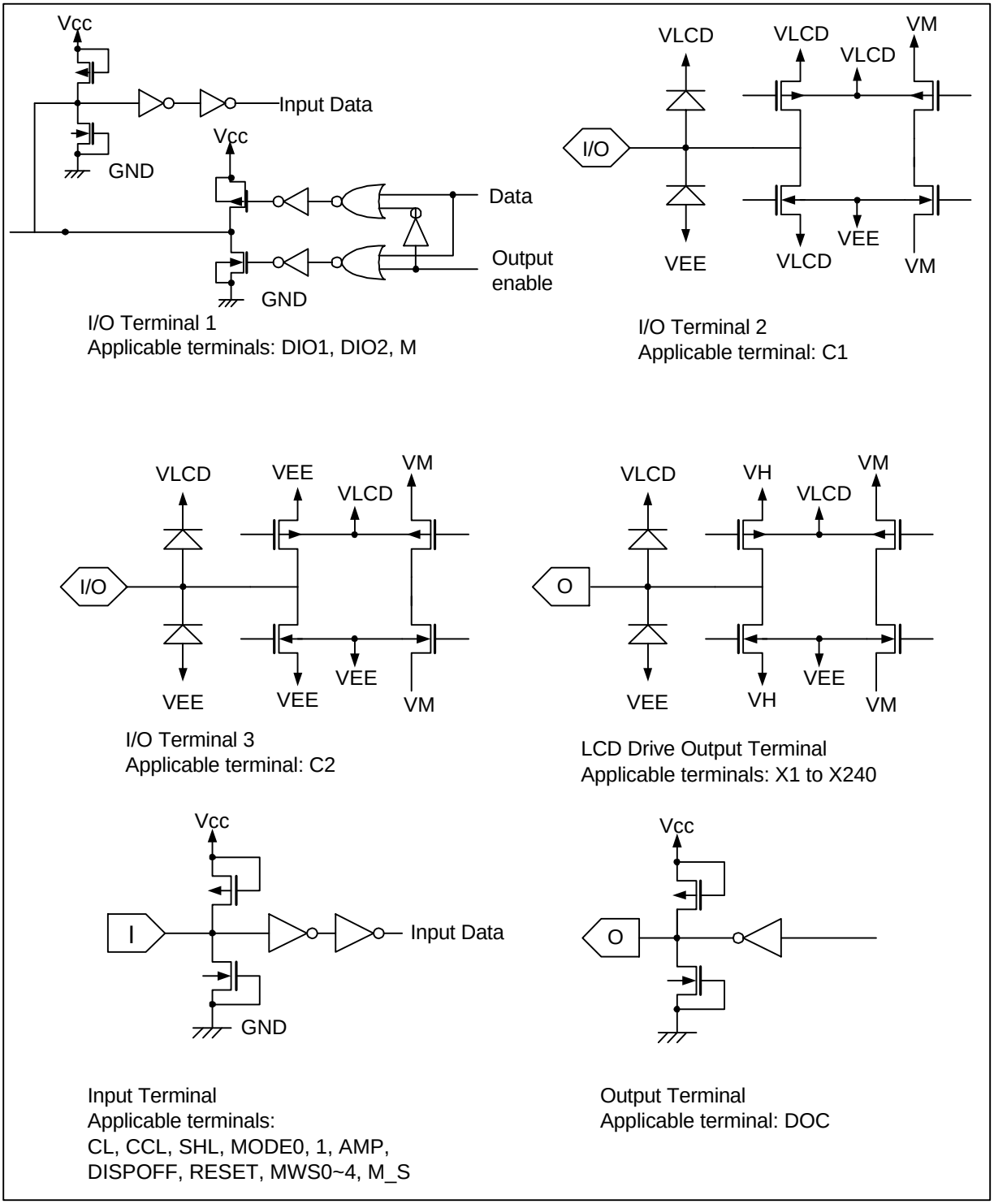


Figure 7-2. IT7020 I/O, Input and Output Terminal Configuration

8. DC Electrical Characteristics

Absolute Maximum Ratings

Power Supply (Vcc) ..... -0.3 to +7.0V
Power Supply (VLCD) ..... -0.3 to +25.0V
Power Supply (VEE).....-23.0 to +0.3V
Input Voltage (1) (VT1)..... -0.3 to Vcc +0.3
Input Voltage (2) (VH)..... -0.3 to VLCD
Input Voltage (3) (VL) ..... -0.3 to VEE
Input Voltage (4) (VM) ..... -0.3 to +5.0V
Operating temperature (Topr)..... -30 to +75V
Storage temperature (Tetg).....- 55 + 110V

***Comments:**

Stresses above those listed under ″Absolute Maximum Ratings″ may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Parameter		Symbol	Ratings	Unit	Notes
Power supply voltage	Logic circuit	Vcc	-0.3 to + 7.0	V	1, 8
	LCD drive circuit	VLCD	-0.3 to + 25.0	V	1, 3, 8
		VEE	-23.0 to + 0.3	V	1, 4, 8
Input voltage (1)		VT1	-0.3 to Vcc + 0.3	V	1, 2
Input voltage (2)		VH	-0.3 to VLCD	V	1, 5, 8
Input voltage (3)		VL	-0.3 to VEE	V	1, 6, 8
Input voltage (4)		VM	-0.3 to + 5.0	V	1, 7, 8
Operating temperature		Topr	-30 to + 75	°C	-
Storage temperature		Tetg	-55 to + 110	°C	-

Notes: 1. Indicates the voltage from GND.
2. The input voltage (1) is applicable to DIO1, DISPOFF, SHL, M, MWS0-MWS4, RESET, MODE0, MODE1, CL, M_S, AMP, CCL, and DIO2.
3. The power supply voltage for LCD drive circuits can be applied to VLCDL/R pins.
4. The power supply voltage for LCD drive circuits can be applied to VEE/R pins.
5. The input voltage (2) is applied to VHL/R pins.
6. The input voltage (3) is applied to VLL/R pins.
7. The input voltage (4) is applied to VML/R pins.
8. See section 8.1 for details.

8.1 Activation and Inactivation Sequence

Make sure to follow activation and inactivation sequence for power supplies and signals as illustrated in the Figure 8-1. This sequence is applied to the built-in power circuit. It is recommended that users must follow the sequence correctly; otherwise, the device malfunction, permanent damage, or undesired effects may occur.

8.1.1 Power On Sequence

1. Power on the power supply in the order listed below:
   Power On order: GND-Vcc, GND-VLCD (VH), and VM.
   VM-VEE is generated automatically. Input GND power to the DISPOFF pin.
2. The LCD level is forced to output the VM level through the DISPOFF function.
3. The DISPOFF function has a higher priority even if the input signal distortion occurs instantly after Vcc input.
4. Then input the preset signals to get the driver registers initialized. In this case, make sure a period that lasts more than one frame is reserved.
5. The preceding work for normal display is completed here. At this point, users should cancel the DISPOFF function by setting the DISPOFF pin to Vcc. The voltage levels of VEE (VL), VLCD (VH) and VM must have reached the preset voltage respectively.

8.1.2 Power Down Sequence

Shut down the power in an opposite order described for power on sequence on the last page.

1. Firstly, the DISPOFF pin should be set to GND.
2. Secondly, the LCD power supply of GND-VLCD (VH) should be turned off. At the same time, GND-VEE (VL) gets to VM. Shut off the VM next.
3. Vcc should be set, and the input signal should be set to GND.
4. At this moment, the inputs of pins VEE (VL), VLCD (VH) and VM must go down to 0 V completely.
   In addition, an incorrect display may occur at power down or power on. This is because the function of DISPOFF is inactivated when the Vcc level goes down to GND, which may cause the LCD to output a level other than VM.

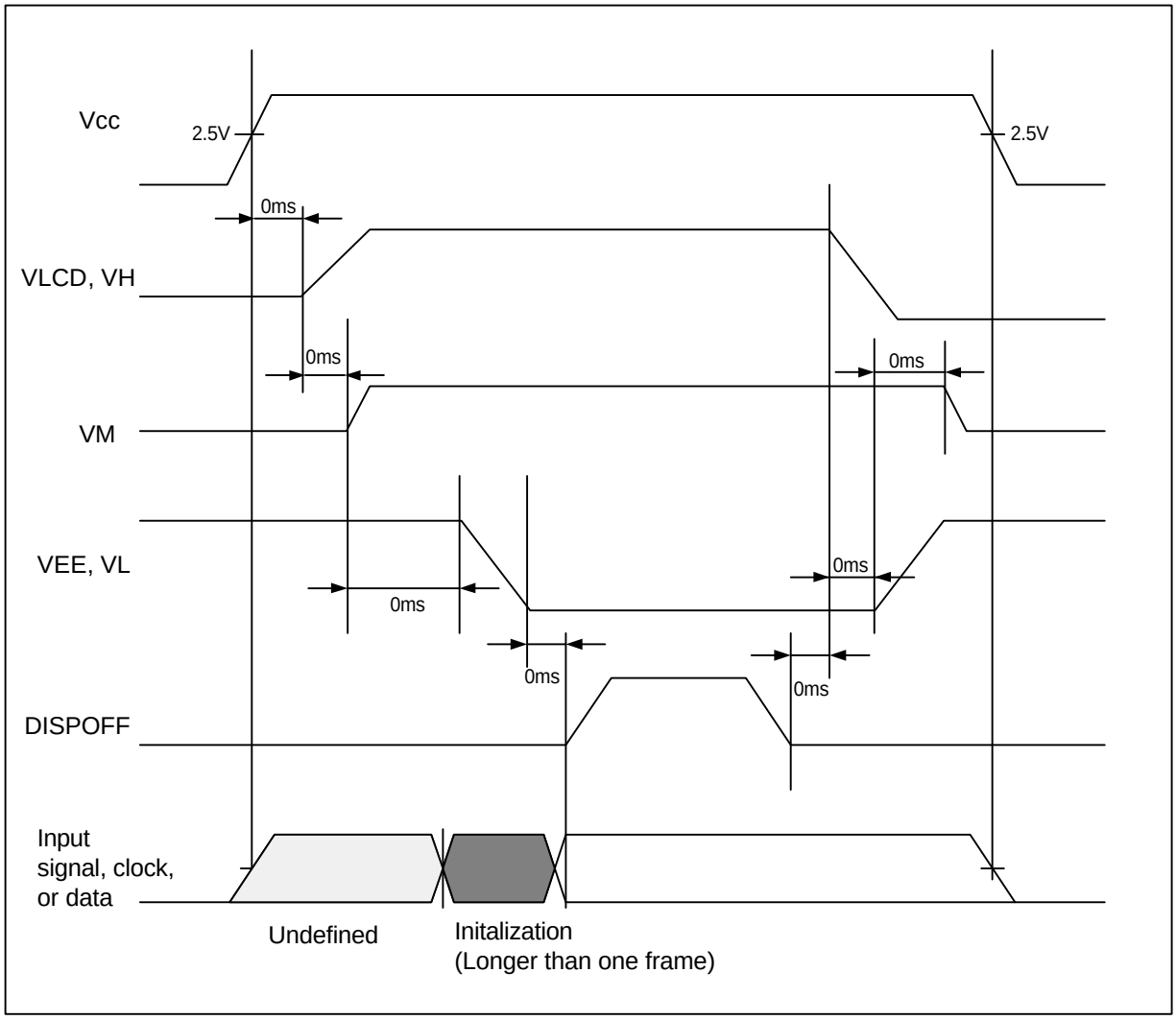


Figure 8-1. IT7020 Power On/Down Scenario

8.2 DC Electrical Characteristics (Vcc = 3 to 5.5V, GND = 0V, VLCD - VEE = 15 to 43V, Ta = -30 to +75 °C)

1. The parameter "ON resistance between Vi—Xj" in the table below indicates a resistance value between of the X and one of the V pins (either one of VH, VL, or VM) when a load current is applied to one of X1 to X240 pins. These resistance values are specified under the conditions listed below:
   VLCD = VH = 21.75V, VEE = VL =-18.5V, VM = 1.75V, GND = 0V.
   Use VH, VL, and VM in the range of VLCD – VM ≥ VH – VM = 21.5 to 7.5V, VEE – VM≤VL – VM = -21.5 to –7.5V in the relation of VH>VM>VL.
2. The current applied between the input and output is removed. The power supply current will increase through the current flows between the power supplies under the condition that an input to a CMOS gate is at an intermediate level. Therefore, use V_{IH} = Vcc and V_{IL} = GND.
3. The voltage relationship of each signal is illustrated in Figure 8-2:

Table 8-1. DC Characteristics (Vcc = 3 to 5.5V, GND = 0V, VLCD - VEE = 15 to 43V, Ta = -30 to +75 °C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions	Applicable Pin(s)
V_{IH}	Input high-level voltage	0.7×Vcc	—	Vcc	V		DIO1, DISPOFF, SHL, M, M_S, MWS0~4, RESET
V_{IL}	Input low-level voltage	0	—	0.3×Vcc	V		CL, MODE0, MODE1, DOC, AMP, CCL, DIO2
V_{OH}	Output high-level voltage	Vcc-0.4	—	—	V	I_{OH} = -0.4 mA	M, DOC, DIO1, DIO2
V_{OL}	Output low-level voltage	—	—	0.4	V	I_{OL} = 0.4 mA	M, DOC, DIO1, DIO2
RON	ON resistance between Vi—Xj	—	0.7	2.0	kΩ	I_{ON} = 150 µA	X1-X240, V pin
$I_{IL}1$	Input leak current (1)	TBD	TBD	TBD	µA		DIO1, DISPOFF, SHL, M, M_S, MWS0~4, RESET, CL, MODE0, MODE1, DOC, AMP, CCL, DIO2
$I_{IL}2$	Input leak current (2)	TBD	TBD	TBD	µA		VH, VL, VM, C1, C2
$I_{CC}1$	Current consumption (1)	TBD	TBD	TBD	µA		Vcc
$I_{CC}2$	Current consumption (2)	TBD	TBD	TBD	µA		Vcc
I_{LCD}	Current consumption (3)	TBD	TBD	TBD	µA		VLCD

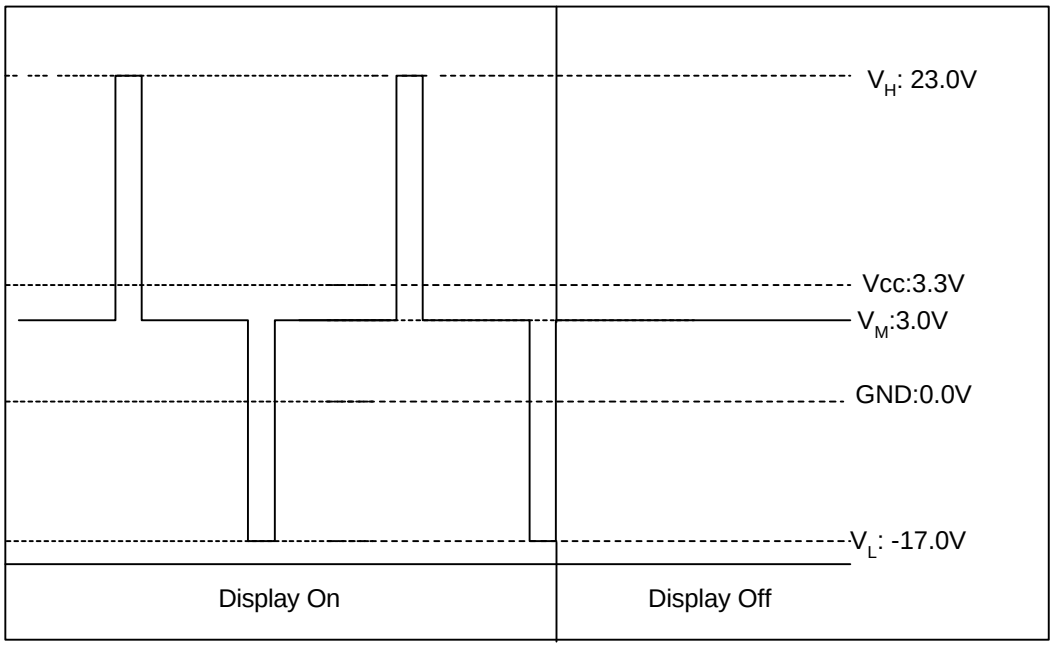


Figure 8-2. LCD Common Drive Output Waveform & Voltage Level

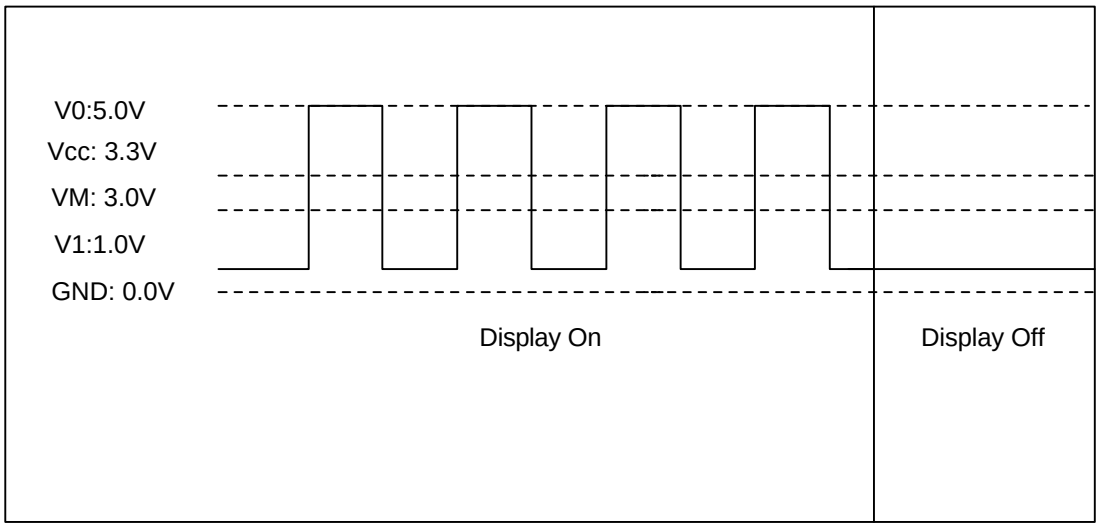


Figure 8-3. LCD Segment Drive Output Waveform & Voltage Level

9. AC Characteristics

9.1 AC Characteristics 1 (Vcc = 3 to 5.5V, GND = 0V, VLCD - VEE = 15 to 43V, Ta = -30 to +75 °C)

Table 9-1. AC Characteristics 1(Vcc = 3 to 5.5V, GND = 0V, VLCD - VEE = 15 to 43V, Ta = -30 to +75 °C)

Symbol	Parameter	Applicable Pins	Typ.	Min.	Max.	Unit
t_{CYC}	Clock cycle time	CL		400	—	ns
t_{CWH}	CL high-level width	CL		25	—	ns
t_{CWL}	CL low-level width	CL		370	—	ns
t_r	CL rising time	CL		—	30	ns
t_f	CL falling time	CL		—	30	ns
t_{DS}	Data set-up time	DIO1, DIO2, CL		100	—	ns
t_{DH}	Data hold time	DIO1, DIO2, CL		10	—	ns
t_{DD}	Data output delay time	DIO1, DIO2, CL	615	—	200	ns
t_{MD}	M output delay time	M, CL	585	—	200	ns
t_{MS}	M setup time	M, CL		20	—	ns
t_{MH}	M hold time	M, CL		20	—	ns
t_{DOC1}	DOC delay time 1	DISPOFF, DOC		—	300	ns
t_{DOC2}	DOC delay time 2	DIO1, DIO2, DOC		—	300	ns

9.2 AC Characteristics 2 (Vcc = 3 to 4.5V, GND = 0V, VLCD - VEE = 43V, Ta = -30 to +75 °C)

Table 9-2. AC Characteristics 2 (Vcc = 3 to 4.5V, GND = 0V, VLCD - VEE = 43V, Ta = -30 to +75 °C)

Symbol	Parameter	Applicable Pins	Typ.	Min.	Max.	Unit
t_{pd1}	Output delay time 1	X (n), M	1.44	—	1.2	µs

9.3 AC Characteristics 3 (Vcc = 4.5 to 5.5V, GND = 0V, VLCD - VEE = 43V, Ta = -30 to +75 °C)

Table 9-3. AC Characteristics 3 (Vcc = 4.5 to 5.5V, GND = 0V, VLCD - VEE = 43V, Ta = -30 to +75 °C)

Symbol	Parameter	Applicable Pins	Typ.	Min.	Max.	Unit
t_{pd1}	Output delay time 1	X (n), M		—	0.7	µs

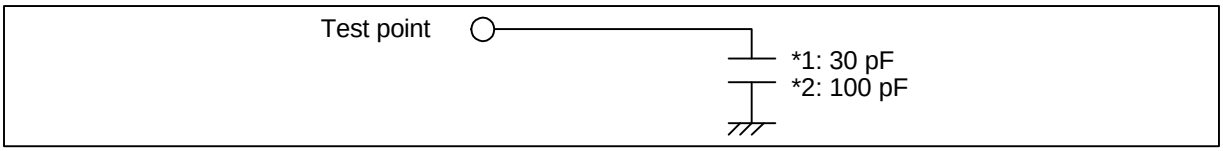


Figure 9-1. AC Characteristics Testing Configuration

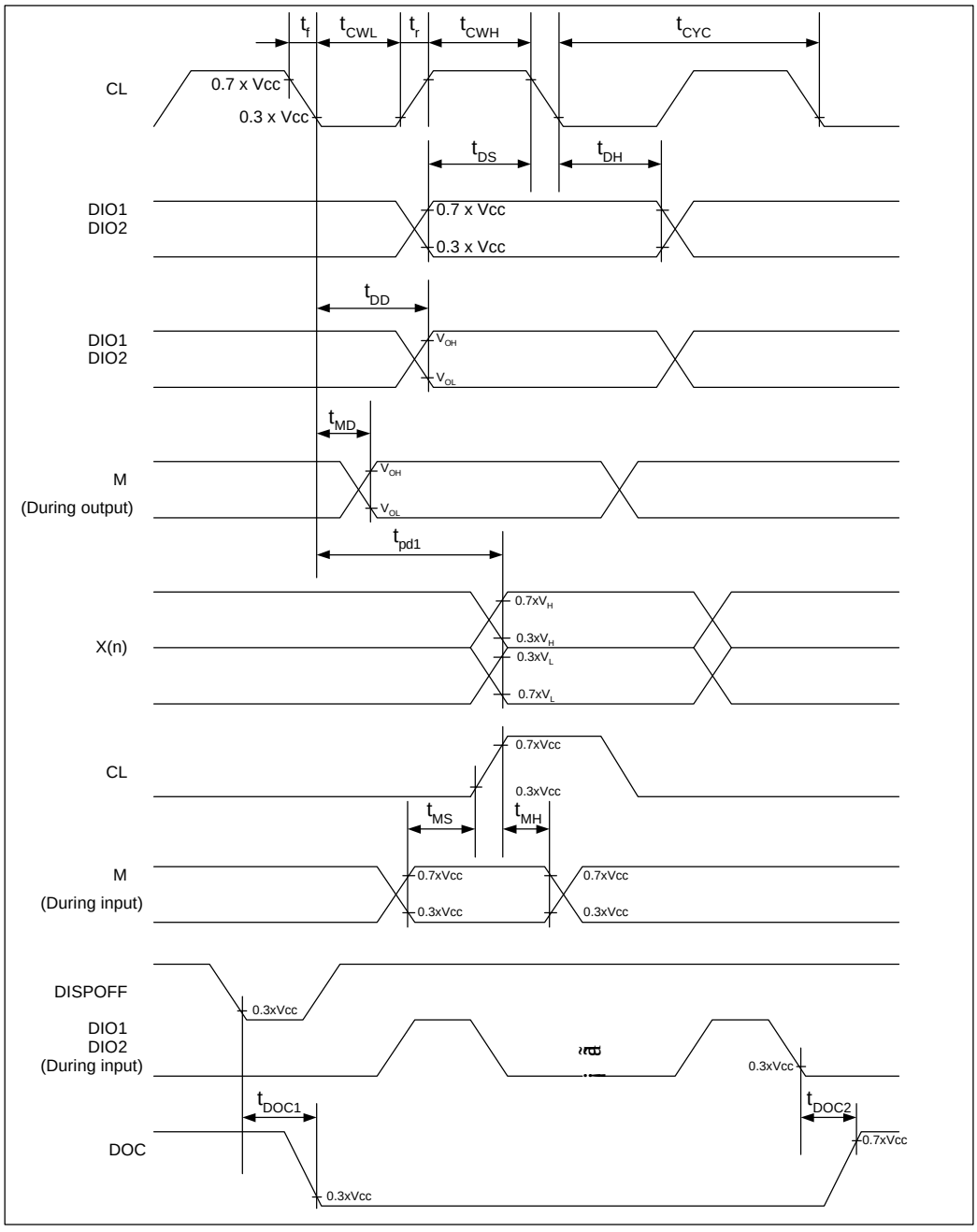


Figure 9-2. IT7020 Timing Diagram

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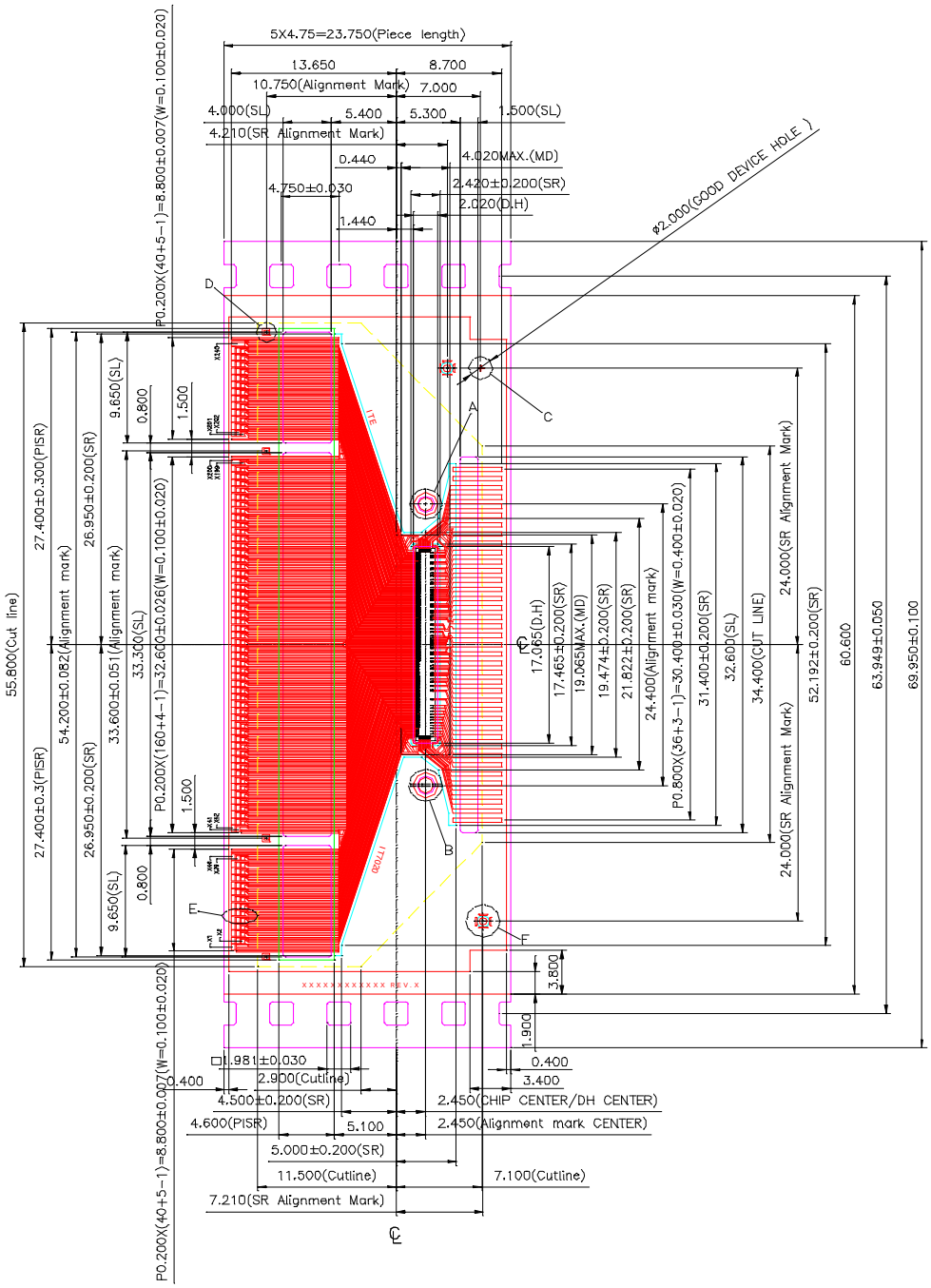
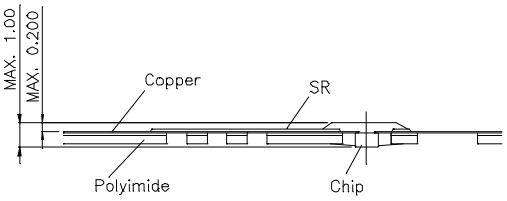
10. Package Information

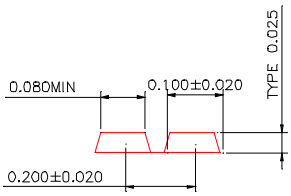
TCP Outline Dimensions **unit: mm**



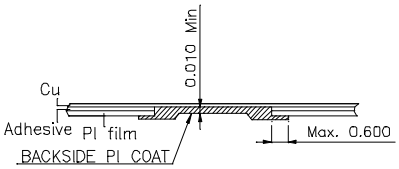
INPUT LEAD NAME

NC
NC
NC
VLCDR
VHR
VMR
VLR
VEER
DIO1
M_S
CCL
CL
GND
SHL
AMP
DISPOFF
DOC
MODE0
MODE1
Vcc
MWS0
MWS1
MWS2
MWS3
MWS4
RESET
M
DIO2
C2
C1
VEO
VEEL
VLL
VML
VHL
VLCDL
NC
NC
NC

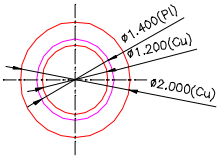




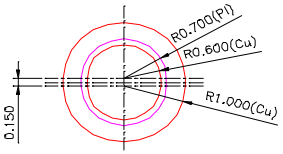
CROSS SECTION OF OUTPUT LEADs



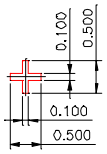
Detail of flex



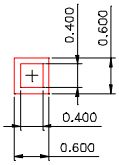
DETAIL : A



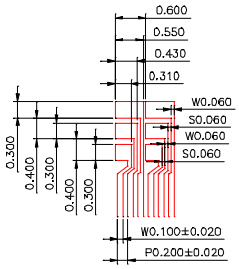
DETAIL : B



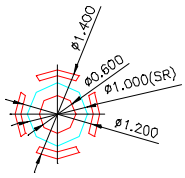
DETAIL : C



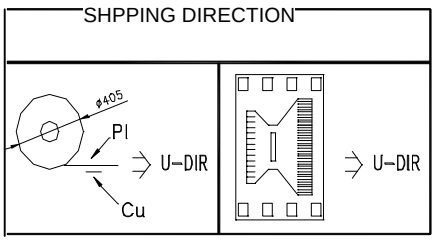
DETAIL : D



DETAIL : E
(Output Side TEST PADS)



DETAIL : F



NOTE:

1. Film: UPILEX-S 75±5um thickness
   Copper: FQ-VLP 25±5um thickness
   Adhesive: Toray #7100 12±2um thickness
   Solder resist: AE-70-M11 26±14um thickness
   Flex Coating: FS-100L Min. 10um
2. Plating: Pure Sn thickness : 0.21±0.05um unless otherwise noted
3. All corner radius of Base Film are less than 0.2mm
4. Other specs than displayed in this drawing are based on the standard spec lists
5. All dimensional tolerances of "SR" are ±0.2mm unless otherwise noted
6. All dimensional tolerances of "base film" are ±0.05mm unless otherwise noted
7. Inner lead accumulative pitch :
   Output side : 15.926±0.0096 mm
   Input side : 15.926±0.0096 mm

11. Ordering Information

Part No.	Package
IT7020C	273-TCP
IT7020H	Bare-chip (349 bumps)