PRELIMINARY

Integrated Circuit Systems, Inc.

ICS83947

LOW SKEW, 1-TO-9 LVCMOS FANOUT BUFFER

GENERAL DESCRIPTION

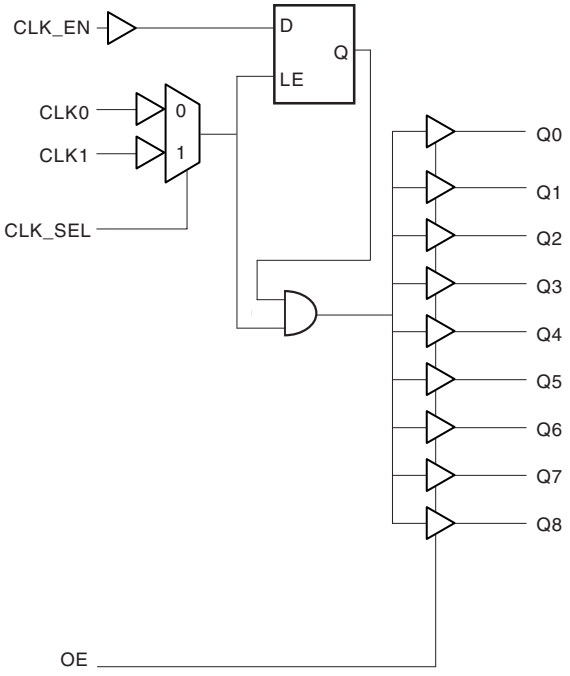
The ICS83947 is a low skew, 1-to-9 LVCMOS Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 9 to 18 by utilizing the ability of the outputs to drive two series terminated lines.

Guaranteed output and part-to-part skew characteristics make the ICS83947 ideal for high performance, single ended applications that also require a limited output voltage.

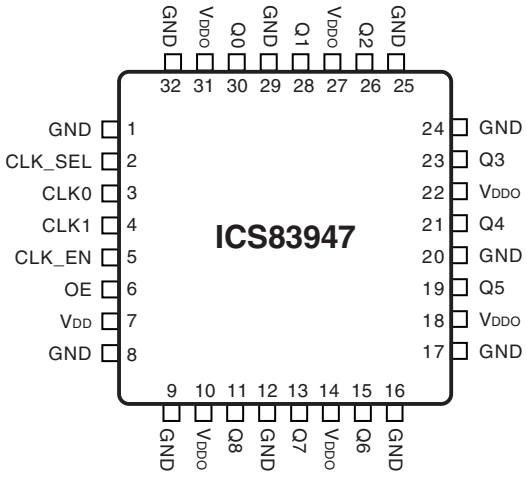
FEATURES

- 9 LVCMOS outputs
- Selectable CLK0 and CLK1 can accept the following input levels: LVCMOS and LVTTL
- Maximum output frequency: 250MHz
- Output skew: 500ps (maximum)
- Part-to-part skew: 2ns (maximum)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Pin compatible with the MPC947

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 8, 9, 12, 16, 17, 20, 24, 25, 29, 32	GND	Power		Power supply ground. Connect to ground.
2	CLK_SEL	Input	Pullup	Clock select input. When HIGH, selects CLK1. When LOW, selects CLK0. LVCMOS / LVTTL interface levels.
3, 4	CLK0, CLK1	Input	Pullup	Reference clock inputs. LVCMOS / LVTTL interface levels.
5	CLK_EN	Input	Pullup	Clock enable. LVCMOS / LVTTL interface levels.
6	OE	Input	Pullup	Output enable.
7	V_{DD}	Power		Positive supply pin. Connect 3.3V.
10, 14, 18, 22, 27, 31	V_{DDO}	Power		Output supply pins. Connect 3.3V.
11, 13, 15, 19, 21, 23, 26, 28, 30	Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Q0 thru Q8 clock outputs.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDO} = 3.6V				pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
R_{OUT}	Output Impedance			7		Ω

TABLE 3. OUTPUT ENABLE AND CLOCK ENABLE FUNCTION TABLE

Control Inputs		Output
OE	CLK_EN	Q0 thru Q8
0	X	Hi-Z
1	0	LOW
1	1	Follows CLK input

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, Tstg	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Input Supply Voltage		3.0	3.3	3.6	V
V_{DDO}	Output Supply Voltage		3.0	3.3	3.6	V
I_{DD}	Input Supply Current			33		mA
I_{DDO}	Output Supply Current			8		mA

TABLE 4B. LVCMOS DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK0, CLK1		2		V_{DD} + 0.3	V
		CLK_SEL, CLK_EN, OE		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	CLK0, CLK1		-0.3		1.3	V
		CLK_SEL, CLK_EN, OE		-0.3		0.8	V
I_{IH}	Input High Current	CLK0, CLK1, CLK_SEL, OE, CLK_EN	$V_{DD} = V_{IN} = 3.6V$			5	µA
I_{IL}	Input Low Current	CLK0, CLK1, CLK_SEL, OE, CLK_EN	$V_{DD} = 3.6V$, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage		I_{OH} = -20mA	2.5			V
V_{OL}	Output Low Voltage		I_{OL} = 20mA			0.4	V
I_{OZL}	Output Tristate Low Current					TBD	µA
I_{OZH}	Output Tristate High Current					TBD	µA

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{pLH}	Propagation Delay, Low to High; NOTE 1	f ≤ 250MHZ		2.6		ns
t_{pHL}	Propagation Delay, High to Low; NOTE 1	f ≤ 250MHZ		2.6		ns
*t*sk(o)	Output Skew; NOTE 2, 5	Measured on rising edge @$V_{DDO}/2$			500	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5	Measured on rising edge @$V_{DDO}/2$			2	ns
t_R	Output Rise Time	0.8V to 2.0V	0.2		1	ns
t_F	Output Fall Time	0.8V to 2.0V	0.2		1	ns
t_{PW}	Output Pulse Width		tCycle/2 - 800		tCycle/2 + 800	ps
t_{EN}	Output Enable Time; NOTE 4				11	ns
t_{DIS}	Output Disable Time; NOTE 4				11	ns
t_S	Clock Enable Setup Time			TBD		ns
t_S	Clock Enable Hold Time			TBD		ns

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

PARAMETER MEASUREMENT INFORMATION

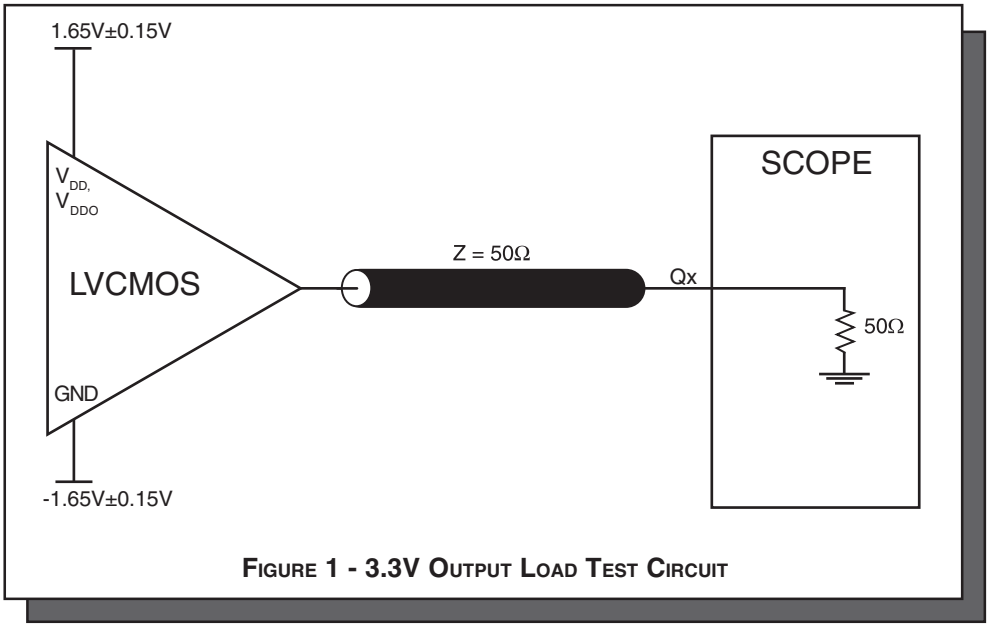


FIGURE 1 - 3.3V OUTPUT LOAD TEST CIRCUIT

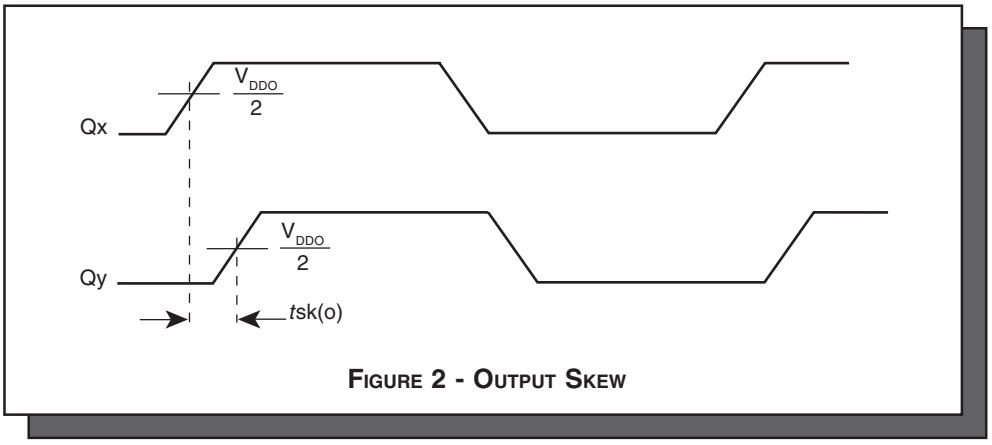


FIGURE 2 - OUTPUT SKEW

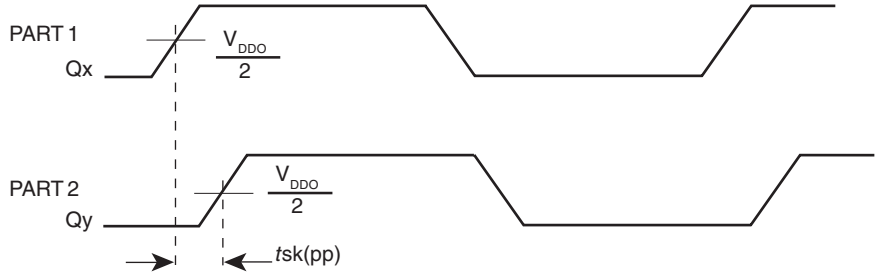


FIGURE 3 - PART-TO-PART SKEW

FIGURE 4 - INPUT AND OUTPUT RISE AND FALL TIME

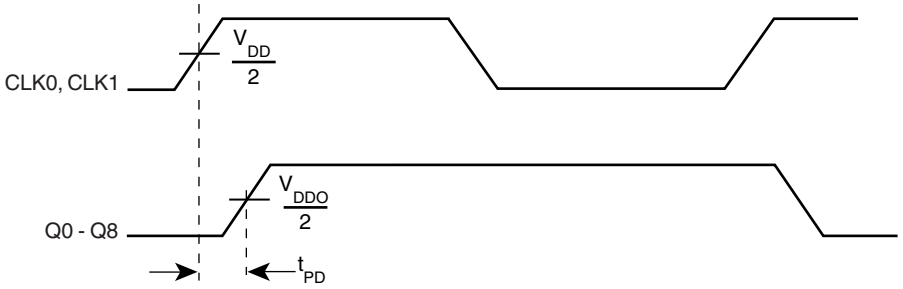


FIGURE 5 - PROPAGATION DELAY

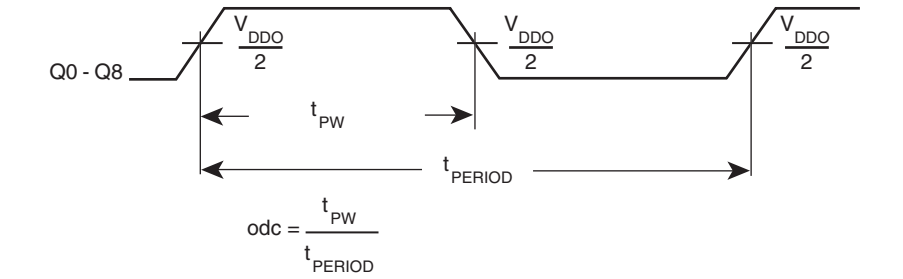


FIGURE 6 - t_{PW} & t_{PERIOD}

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS83947 is: 1040

PACKAGE OUTLINE - Y SUFFIX

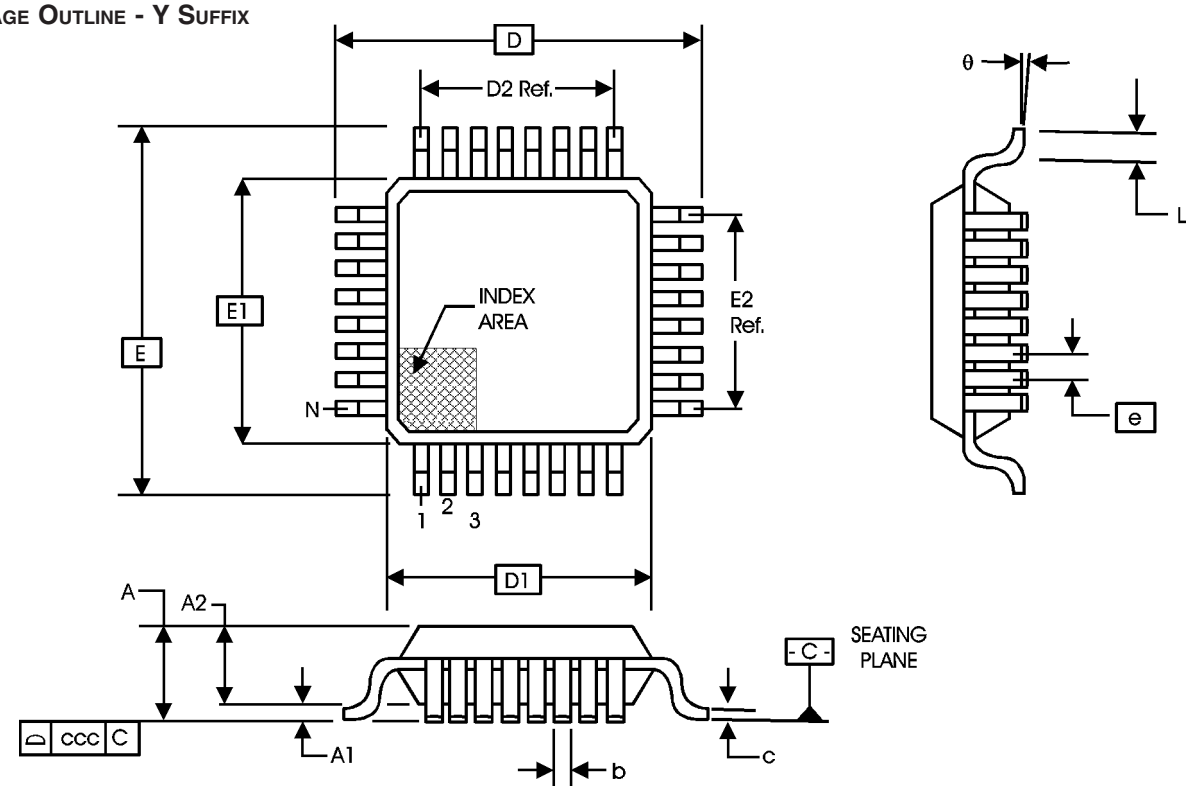


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS83947AY	ICS83947AY	32 Lead LQFP	250 per tray	0°C to 70°C
ICS83947AYT	ICS83947AY	32 Lead LQFP on Tape and Reel	1000	0°C to 70°C