ICS8533-01

LOW SKEW, 1-TO-4 DIFFERENTIAL-TO-3.3V LVPECL FANOUT BUFFER

GENERAL DESCRIPTION

ICS HiPerClockS™

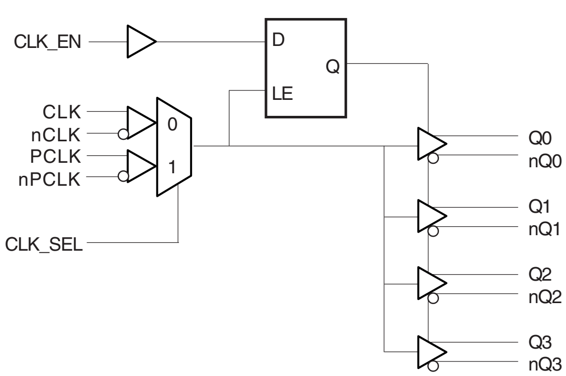
The ICS8533-01 is a low skew, high performance 1-to-4 Differential-to-3.3V LVPECL fanout buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8533-01 has two selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8533-01 ideal for those applications demanding well defined performance and repeatability.

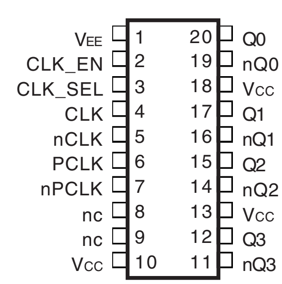
FEATURES

- 4 differential 3.3V LVPECL outputs
- Selectable differential CLK, nCLK or LVPECL clock inputs
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- PCLK, nPCLK supports the following input types: LVPECL, CML, SSTL
- Maximum output frequency up to 650MHz
- Translates any single-ended input signal to 3.3V LVPECL levels with resistor bias on nCLK input
- Output skew: 30ps (maximum)
- Part-to-part skew: 150ps (maximum)
- Propagation delay: 1.4ns (maximum)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS8533-01
20-Lead TSSOP
6.5mm x 4.4mm x 0.92mm Package Body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{EE}	Power		Negative supply pin. Connect to ground.
2	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVCMOS / LVTTL interface levels.
3	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects differential PCLK, nPCLK inputs. When LOW, selects CLK, nCLK inputs. LVCMOS / LVTTL interface levels.
4	CLK	Input	Pulldown	Non-inverting differential clock input.
5	nCLK	Input	Pullup	Inverting differential clock input.
6	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
7	nPCLK	Input	Pullup	Inverting differential LVPECL clock input.
8, 9	nc	Unused		No connect.
10, 13, 18	V_{CC}	Power		Positive supply pins. Connect to 3.3V.
11, 12	nQ3, Q3	Output		Differential output pair. LVPECL interface levels.
14, 15	nQ2, Q2	Output		Differential output pair. LVPECL interface levels.
16, 17	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
19, 20	nQ0, Q0	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup* and *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	CLK, nCLK				4	pF
		PCLK, nPCLK				4	pF
		CLK_EN, CLK_SEL				4	pF
R_{PULLUP}	Input Pullup Resistor				51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		KΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs			Outputs	
CLK_EN	CLK_SEL	Selected Source	Q0 thru Q3	nQ0 thru nQ3
0	0	CLK, nCLK	Disabled; LOW	Disabled; HIGH
0	1	PCLK, nPCLK	Disabled; LOW	Disabled; HIGH
1	0	CLK, nCLK	Enabled	Enabled
1	1	PCLK, nPCLK	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1.
In the active mode, the state of the outputs are a function of the CLK , nCLK and PCLK, nPCLK inputs as described in Table 3B.

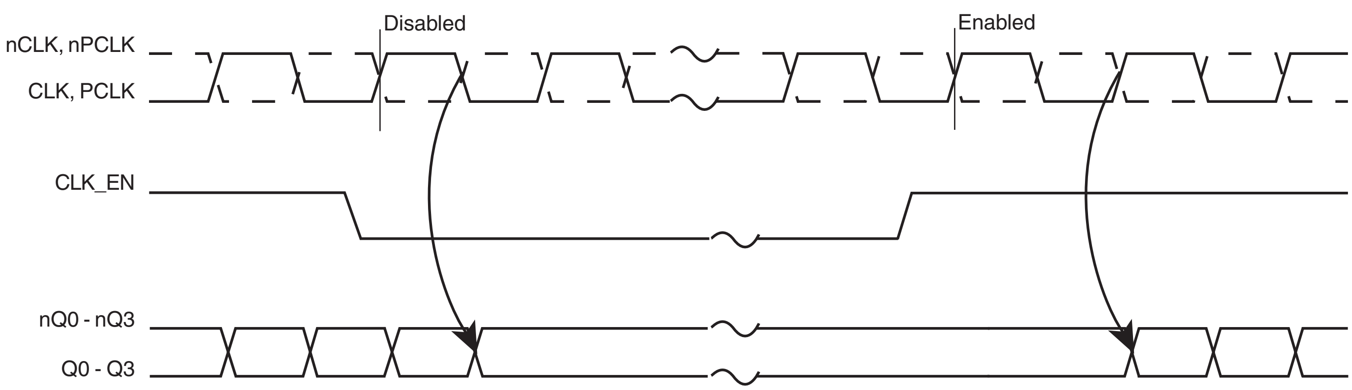


FIGURE 1 - CLK_EN TIMING DIAGRAM

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
CLK or PCLK	nCLK or nPCLK	Q0 thru Q3	nQ0 thru nQ3		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section on page 8, Figure 8, which discusses wiring the differential input to accept single ended levels.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CCx}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, V_O	-0.5V to V_{CC} + 0.5V
Package Thermal Impedance, θ_{JA}	73.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				50	mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{EE} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK_EN	$V_{IN} = V_{CC}$ = 3.465V			5	µA
		CLK_SEL	$V_{IN} = V_{CC}$ = 3.465V			150	µA
I_{IL}	Input Low Current	CLK_EN	V_{IN} = 0V, V_{CC} = 3.465V	-150			µA
		CLK_SEL	V_{IN} = 0V, V_{CC} = 3.465V	-5			µA

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK	$V_{CC} = V_{IN}$ = 3.465V			5	µA
		CLK	$V_{CC} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	nCLK	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
		CLK	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK and nCLK is V_{CC} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4D. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK	$V_{CC} = V_{IN}$ = 3.465V			150	µA
		nPCLK	$V_{CC} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	PCLK	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA
		nPCLK	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.3		1	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 1.5		V_{CC}	V
V_{OH}	Output High Voltage; NOTE 3			V_{CC} - 1.4		V_{CC} - 1.0	V
V_{OL}	Output Low Voltage; NOTE 3			V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing			0.6		0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications the maximum input voltage for PCLK and nPCLK is V_{CC} + 0.3V.
NOTE 3: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 5. AC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency				650	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 650MHz	1.0		1.4	ns
*t*sk(o)	Output Skew; NOTE 2, 4				30	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				150	ps
t_R	Output Rise Time	20% to 80% @ 50MHz	300		700	ps
t_F	Output Fall Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		47		53	%

All parameters measured at 500MHz unless noted otherwise.
The cycle to cycle jitter on the input will equal the jitter on the output. The part does not add jitter.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

PARAMETER MEASUREMENT INFORMATION

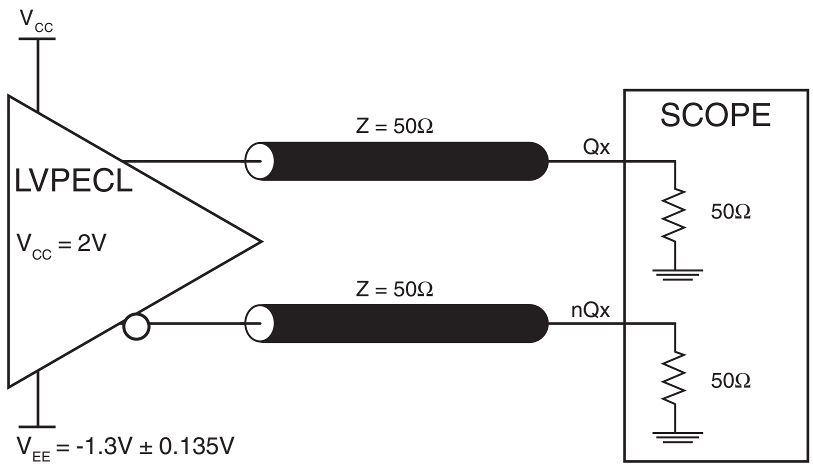


FIGURE 2 - 3.3V OUTPUT LOAD TEST CIRCUIT

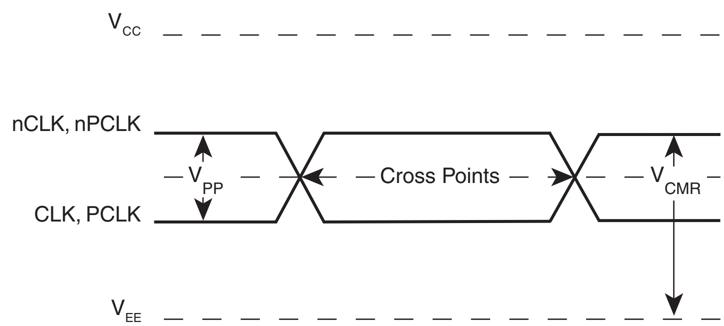


FIGURE 3 - DIFFERENTIAL INPUT LEVEL

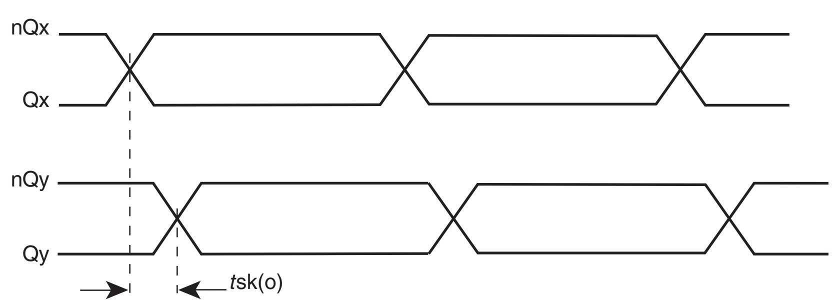


FIGURE 4 - OUTPUT SKEW

FIGURE 5 - INPUT AND OUTPUT RISE AND FALL TIME

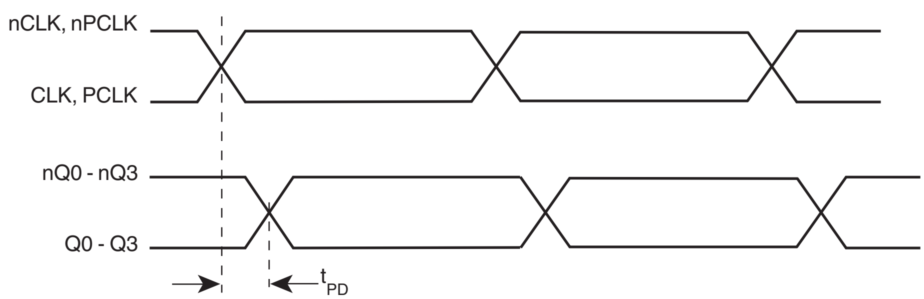
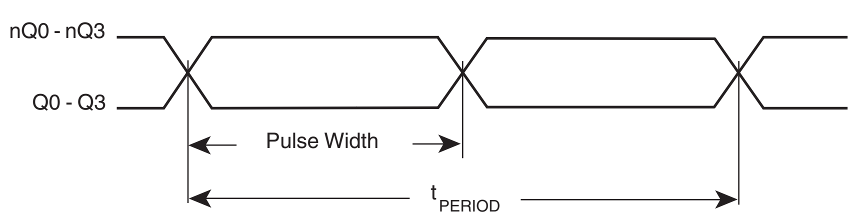


FIGURE 6 - PROPAGATION DELAY



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

FIGURE 7 - odc & t_{PERIOD}

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 8 shows how the differential input can be wired to accept single end levels. The reference voltage V_REF = $V_{CC}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

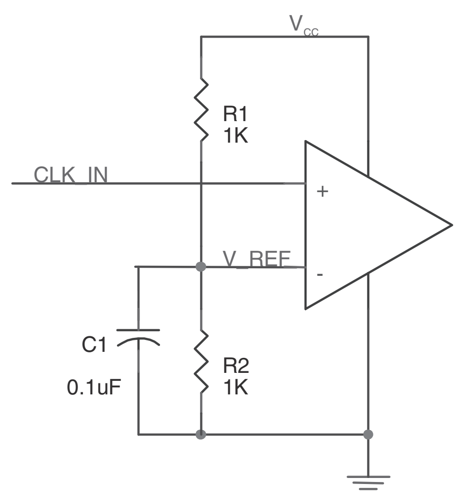


FIGURE 8 - SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8533-01.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS8533-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 50mA = **173.3mW**
- Power (outputs)$_{MAX}$ = **30.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 30.2mW = **120.8mW**

Total Power $_{\_MAX}$ (3.465V, with all outputs switching) = 173.3mW + 120.8mW = **294.1mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = junction-to-ambient thermal resistance

Pd_total = Total device power dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.294W * 66.6°C/W = 89.6°C. This is well below the limit of 125°C

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 20-pin TSSOP, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 9.*

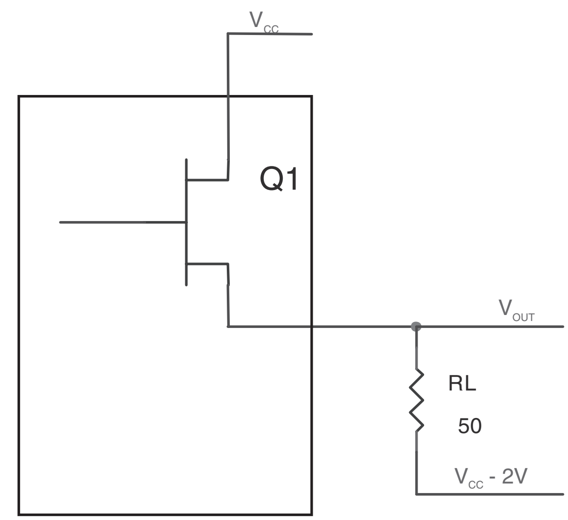


FIGURE 9 - LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX})$

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX})$

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 1.0V}$

  Using V_{CC_MAX} = 3.465, this results in V_{OH_MAX} = **2.465V**

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.7V}$

  Using V_{CC_MAX} = 3.465, this results in V_{OL_MAX} = **1.765V**

Pd_H = [(2.465V - (3.465V - 2V))/50Ω] * (3.465V - 2.465V) = **20mW**
Pd_L = [(1.765V - (3.465V - 2V))/50Ω] * (3.465V - 1.765V) = **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.2mW**

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)

	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8533-01 is: 404

PACKAGE OUTLINE - G SUFFIX

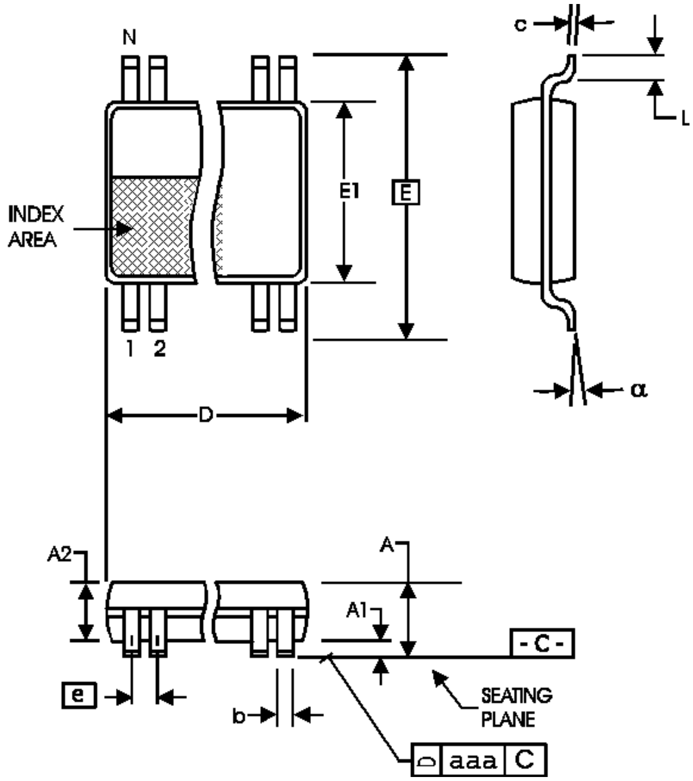


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MS-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8533AG-01	ICS8533AG-01	20 lead TSSOP	72 per tube	0°C to 70°C
ICS8533AG-01T	ICS8533AG-01	20 lead TSSOP on Tape and Reel	2500	0°C to70°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	4C 4D 5	4 5 5	V_{PP} values changed from 0.1 Min. to 0.15 Min. V_{CMR} values changed from 0.13 Min., 1.3 Max. to 1.5 Min, V_{CC} Max. Deleted V_{IH} and V_{IL} rows. t_R values changed from 100 Min. to 300 Min, and added 700 Max. t_F values changed from 100 Min., 600 Max. to 300 Min. to 700 Max. For t_R and t_F rows changed test conditions from 30% to 70% to 20% to 80%. tjit(cc) values changed 150 Max. to 0 Max.	5/22/01
B	5	5	Deleted t_S and t_H rows.	6/4/01
B	4D	5	V_{PP} values changed from 0.15 Min., 1.3 Max. to 0.3 Min., 1 Max. V_{CMR} values changed from 1.5 Min., to V_{EE} + 1.5 Min.	6/28/01
C	4B 5	4 5	V_{IH} values changed from 3.765 Max. to V_{CC} + 0.3 Max. Deleted tjit(cc) row.	10/15/01
C		6, 7	Revised Parameter Measurement diagrams.	10/18/01
C		3	Updated Figure 1, CLK_EN Timing Diagram.	11/1/01