Integrated Circuit Systems, Inc.

ICS8535I-11

LOW SKEW, 1-TO-4, CRYSTAL OSCILLATOR/ LVCMOS-TO-3.3V LVPECL FANOUT BUFFER

GENERAL DESCRIPTION

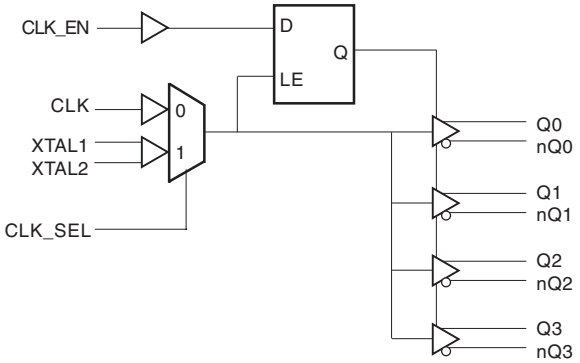
The ICS8535I-11 is a low skew, high performance 1-to-4 3.3V LVPECL clock fanout buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8535I-11 has selectable single ended clock or crystal inputs. The single ended clock input accepts LVCMOS or LVTTL input levels and translate them to 3.3V LVPECL levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8535I-11 ideal for those applications demanding well defined performance and repeatability.

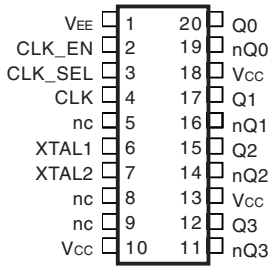
FEATURES

- 4 differential 3.3V LVPECL outputs
- Selectable CLK or crystal inputs
- CLK can accept the following input levels: LVCMOS, LVTTL
- Maximum output frequency: 266MHz
- Output skew: 40ps (maximum)
- Part-to-part skew: 200ps (maximum)
- 3.3V operating supply
- -40°C to 85°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS8535I-11

20-Lead TSSOP

6.5mm x 4.4mm x 0.92 Package Body

G Package

Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{EE}	Power		Negative supply pin. Connect to ground.
2	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follows clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVCMOS / LVTTL interface levels.
3	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK input. When LOW, selects XTAL inputs. LVCMOS / LVTTL interface levels.
4	CLK	Input	Pulldown	Non-inverting LVCMOS / LVTTL clock input.
5, 8, 9	nc	Unused		No connect.
6	XTAL1	Input	Pulldown	Crystal oscillator input.
7	XTAL2	Input	Pullup	Crystal oscillator input.
10, 13, 18	V_{CC}	Power		Positive supply pin. Connect to 3.3V.
11, 12	nQ3, Q3	Output		Differential clock outputs. LVPECL interface levels.
14, 15	nQ2, Q2	Output		Differential clock outputs. LVPECL interface levels.
16, 17	nQ1, Q1	Output		Differential clock outputs. LVPECL interface levels.
19, 20	nQ0, Q0	Output		Differential clock outputs. LVPECL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs			Outputs	
CLK_EN	**CLK_SEL**	**Selected Source**	**Q0 thru Q3**	**nQ0 thru nQ3**
0	0	CLK	Disabled; LOW	Disabled; HIGH
0	1	XTAL1, XTAL2	Disabled; LOW	Disabled; HIGH
1	0	CLK	Enabled	Enabled
1	1	XTAL1, XTAL2	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock or crystal oscillator edge as shown in Figure 1.
In the active mode the state of the output is a function of the CLK input as described in Table 3B.

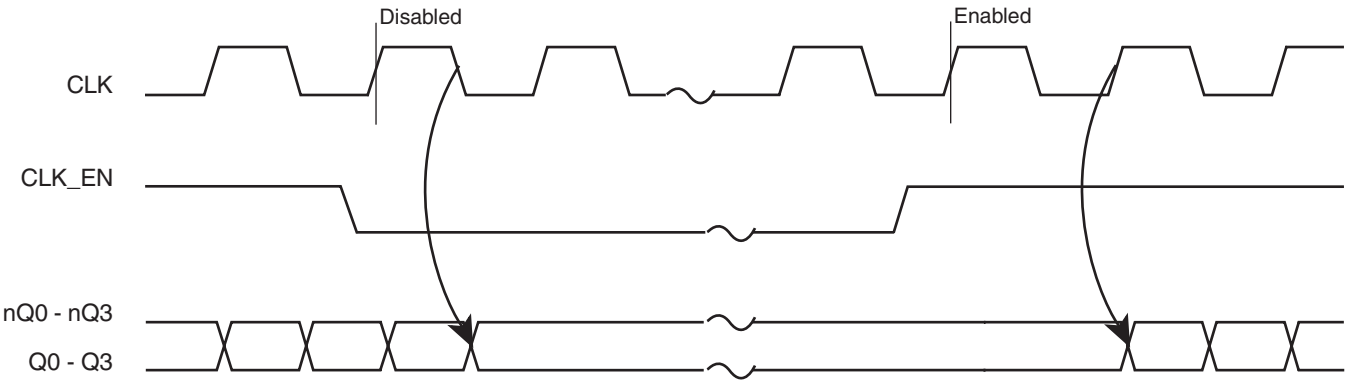


FIGURE 1 - CLK_EN TIMING DIAGRAM

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs	Outputs	
CLK	**Q0 thru Q3**	**nQ0 thru nQ3**
0	LOW	HIGH
1	HIGH	LOW

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CCx}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, V_O	-0.5V to V_{CC} + 0.5V
Package Thermal Impedance, θ_{JA}	73.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these condition or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				50	mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, V_{CC} = 3 .3V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		3.765	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK, CLK_SEL	V_{IN} = V_{CC} = 3.465V			150	µA
		CLK_EN	V_{IN} = V_{CC} = 3.465V			5	µA
I_{IL}	Input Low Current	CLK, CLK_SEL	V_{IN} = 0V, V_{CC} = 3.465V	-5			µA
		CLK_EN	V_{IN} = 0V, V_{CC} = 3.465V	-150			µA

TABLE 4C. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 1.0	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		0.85	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} 2V.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		14		25	MHz
Equivalent Series Resistance (ESR)				70	Ω
Shunt Capacitance				7	pF

TABLE 6. AC CHARACTERISTICS, V_{CC} = 3.3V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency				266	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 266MHz	1.0		2.4	ns
*t*sk(o)	Output Skew; NOTE 2				40	ps
*t*sk(pp)	Part-to-Part skew; NOTE 3				200	ps
t_R	Output Rise Time	20% to 80% @ 50MHz	300		700	ps
t_F	Output Fall Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle; NOTE 4		48	50	52	%
oscTOL	Crystal Oscillator Tollerance				1000	ppm

All parameters measured at 266MHz unless noted otherwise.
The cycle-to-cyle jitter on the input will equal the jitter on the output. The part does not add jitter.
NOTE 1: Measured from the $V_{CC}/2$ of the input to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross point.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: Measured using CLK input. For XTAL input, refer to Application Note.

PARAMETER MEASUREMENT INFORMATION

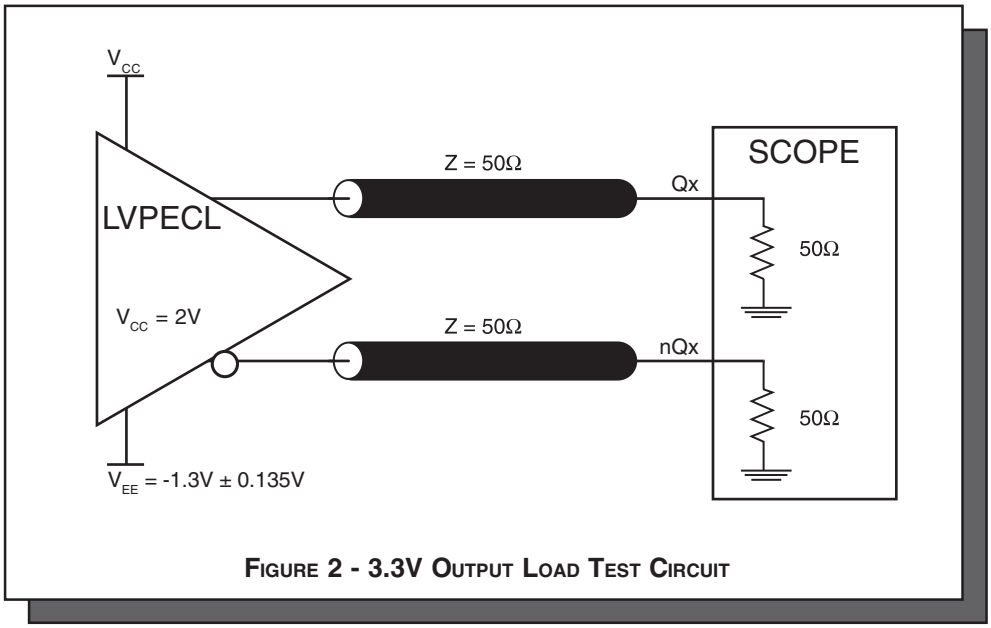


FIGURE 2 - 3.3V OUTPUT LOAD TEST CIRCUIT

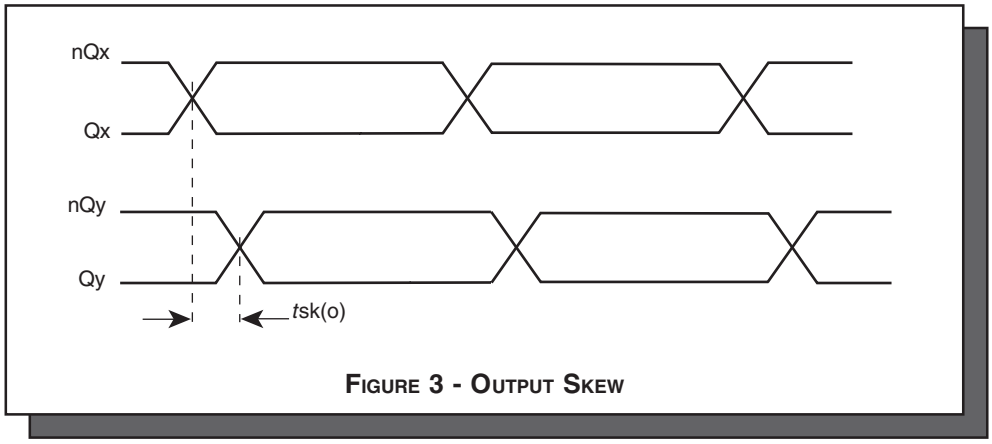


FIGURE 3 - OUTPUT SKEW

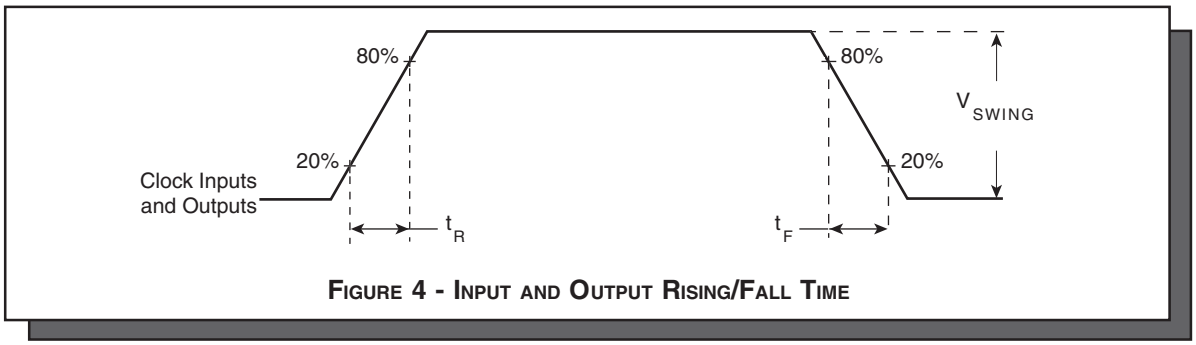


FIGURE 4 - INPUT AND OUTPUT RISING/FALL TIME

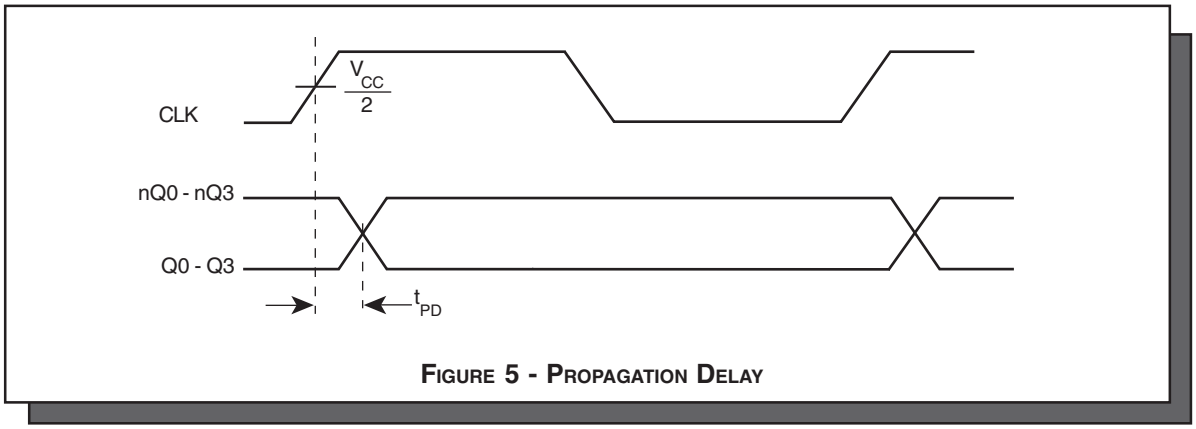


FIGURE 5 - PROPAGATION DELAY

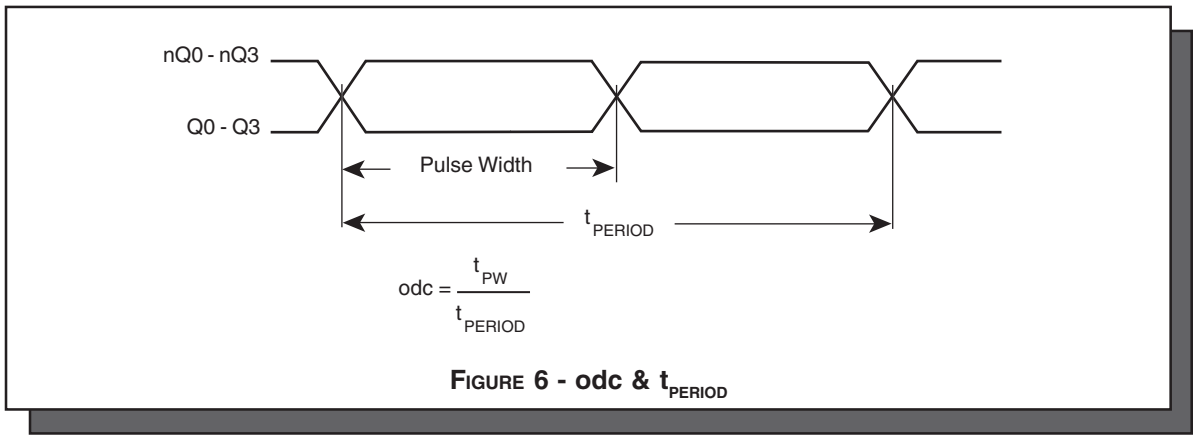


FIGURE 6 - odc & t_{PERIOD}

FIGURE 6 - odc & t_{PERIOD}

APPLICATION INFORMATION

CRYSTAL OSCILLATOR CIRCUIT FREQUENCY FINE TUNING

A crystal can be characterized for either series or parallel mode operation. The ICS8535-11, ICS8535-11I, and ICS8533-11 fanout buffers have built-in crystal oscillator circuits that can accept either a series or parallel crystal without additional components. The frequency accuracy provided by this configuration is sufficient for most computer applications.

For applications requiring highly accurate clock frequencies, the output frequency can be fine tuned by inserting a small series capacitor C1 at the XTAL1 input (Pin 6 for ICS8535-11I) as shown in *Figure 7.* This fine tuning approach can be applied in either parallel or series crystal. The C1 value depends on the crystal type, frequency and the board layout. The parallel crystal fine tuning results in smaller ppm and better performance. It is difficult to provide the precise value of C1. This section provides recommended series capacitor C1 values to start with. The crystals type used in this example are 18pF parallel crystals.

Figure 8 shows the suggested series capacitor value for a parallel crystal. For example, for a 16.666 MHz crystal, the recommended C1 value is about 33pF.

Figure 9 shows frequency accuracy versus series capacitance for 19.44MHz, 16.666MHz and 15MHz crystals. As seen from this figure, a 24pF, 33pF and 43pF series capacitors are used to achieve the lowest ppm error for 19.44MHz, 16.666MHz and 15MHz respectively.

Figure 10 shows the experiment results of crystal oscillator frequency drift due to temperature variation.

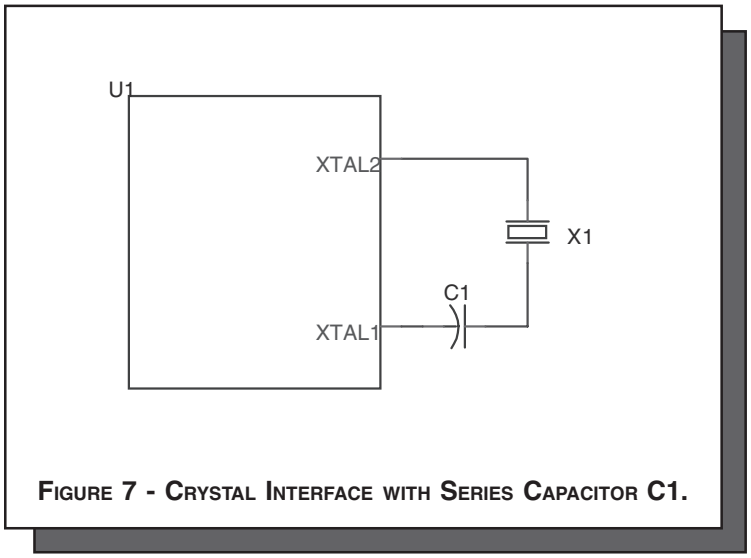


FIGURE 7 - CRYSTAL INTERFACE WITH SERIES CAPACITOR C1.

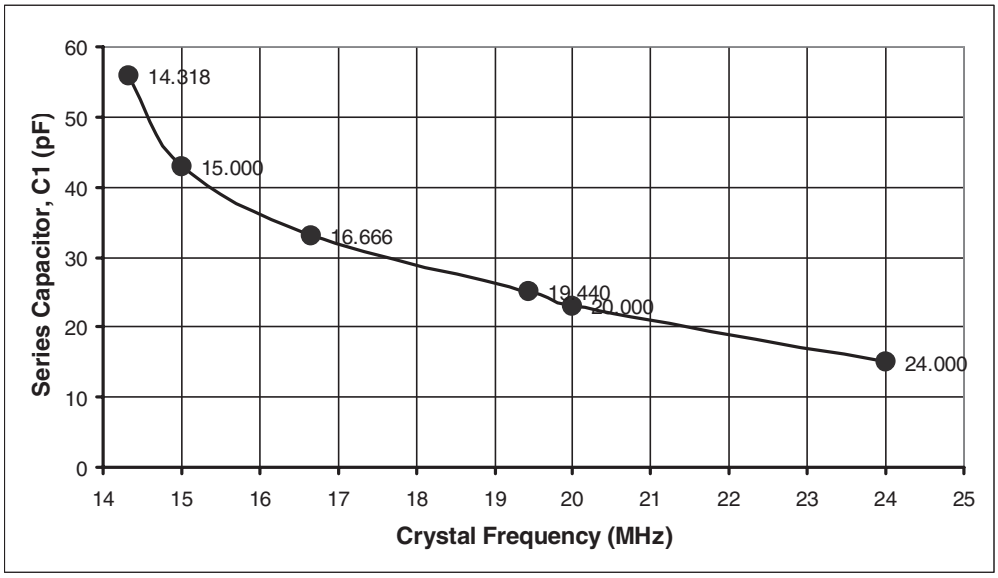


FIGURE 8 - SUGGESTED SERIES CAPACITOR C1 FOR PARALLEL CRYSTAL

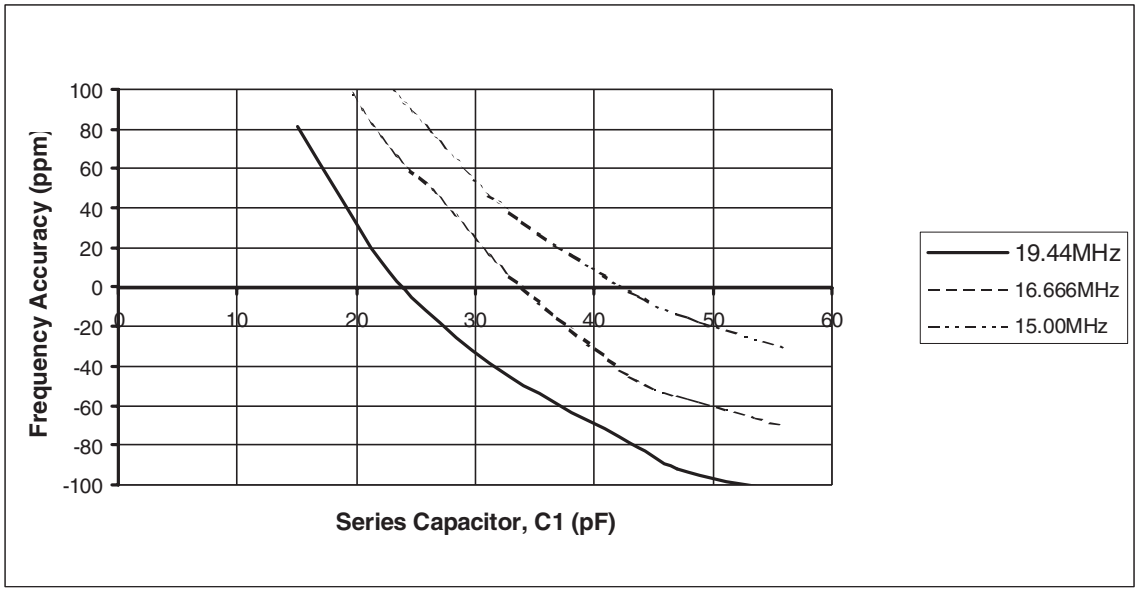


FIGURE 9 - FREQUENCY ACCURACY FOR PARALLEL CRYSTAL USING SERIES CAPACITOR C1.

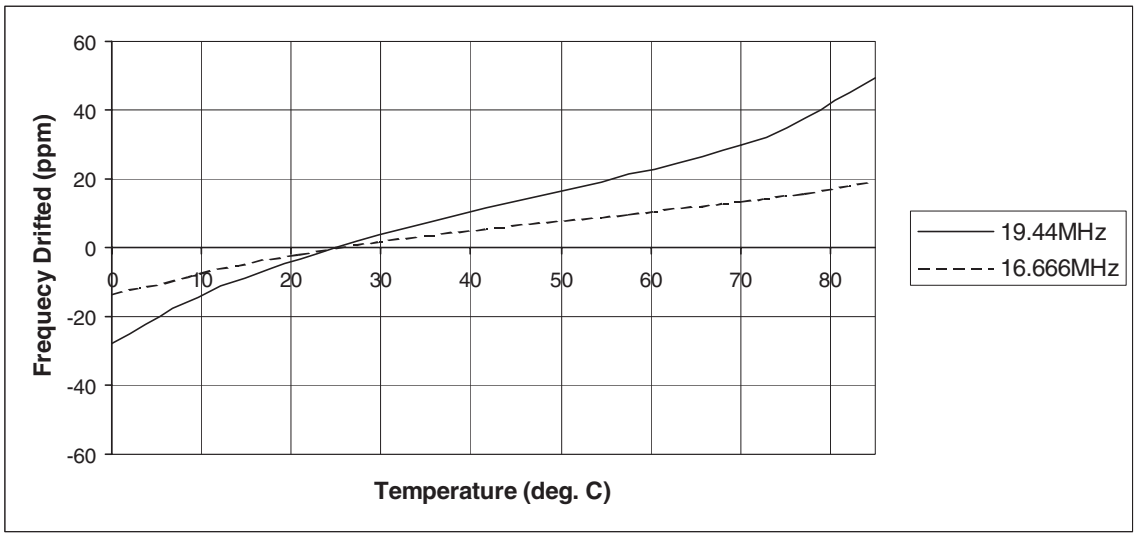


FIGURE 10 - CRYSTAL OSCILLATOR CRCUIT FREQUENCY DRIFTED DUE TO TEMPERATURE VARIATION

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8535I-11.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS8535I-11 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 50mA = **173.25mW**
- Power $(outputs)_{MAX}$ = **30.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 30.2mW = **120.8mW**

Total Power $_{\_MAX}$ **(3.465V, with all outputs switching) = 173.25mW + 120.8mW = 294.05mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.294W * 66.6°C/W = 104.6°C. This is well below the limit of 125°C

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 20-pin TSSOP, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 11.*

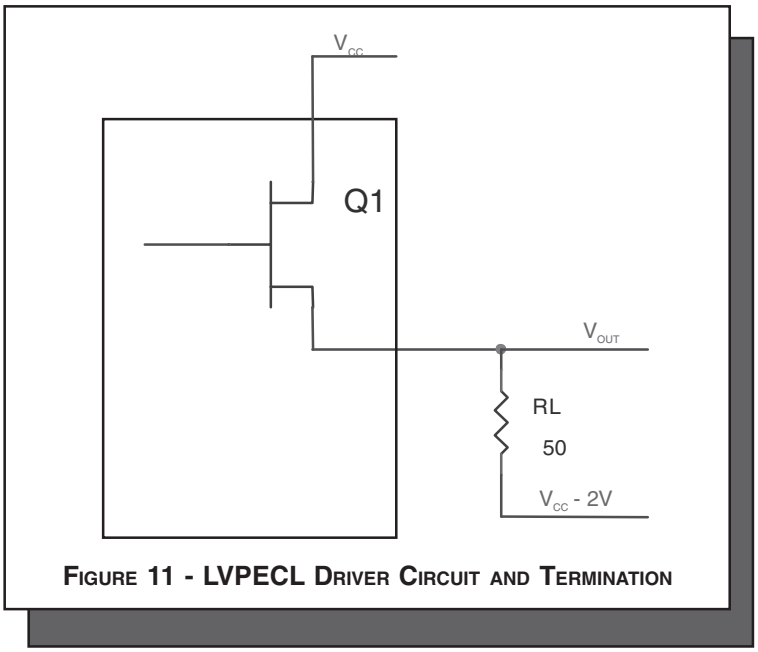


FIGURE 11 - LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 1.0V}$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{1.0V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.7V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 1V)/50\Omega] * 1V = \mathbf{20.0mW}$

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.2mW**

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8535I-11 is: 428

PACKAGE OUTLINE - G SUFFIX

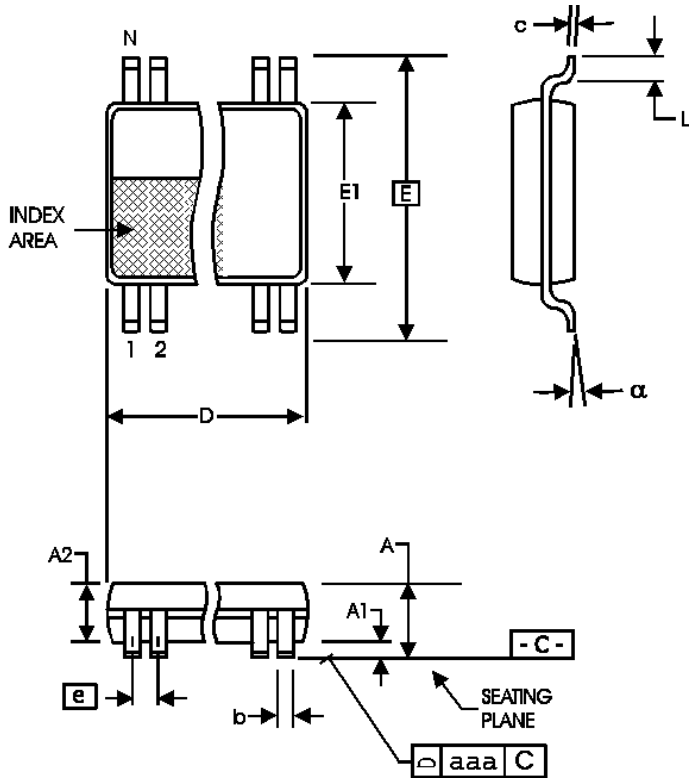


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MIN	MAX
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8535AGI-11	ICS8535AGI11	20 lead TSSOP	72 per tube	-40°C to 85°C
ICS8535AGI-11T	ICS8535AGI11	20 lead TSSOP on Tape and Reel	2500	-40°C to 85°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T6	5	AC Characteristics table. Part-to-Part skew changed from 150ps to 200ps.	9/17/01
B		3	Revised Figure 1, CLK_EN Timing Diagram.	10/18/01
B		3	Revised Figure 1, CLK_EN Timing Diagram.	10/29/01
B	T5	5	Shortened Crystal Characteristics table. ESR row, values have changed from 50Ω Min, 80Ω Max. to 70Ω Max.	1/11/02