PRELIMINARY

Integrated Circuit Systems, Inc.

ICS8516

LOW SKEW, 1-TO-16 DIFFERENTIAL-TO-3.3V LVDS CLOCK DISTRIBUTION CHIP

GENERAL DESCRIPTION

The ICS8516 is a low skew, high performance 1-to-16 Differential-to-3.3V LVDS Clock Distribution Chip and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8516 CLK, nCLK pair can accept any differential input levels and translates them to 3.3V LVDS output levels. Utilizing Low Voltage Differential Signaling (LVDS), the ICS8516 provides a low power, low noise, point-to-point solution for distributing clock signals over controlled impedances of 100Ω.

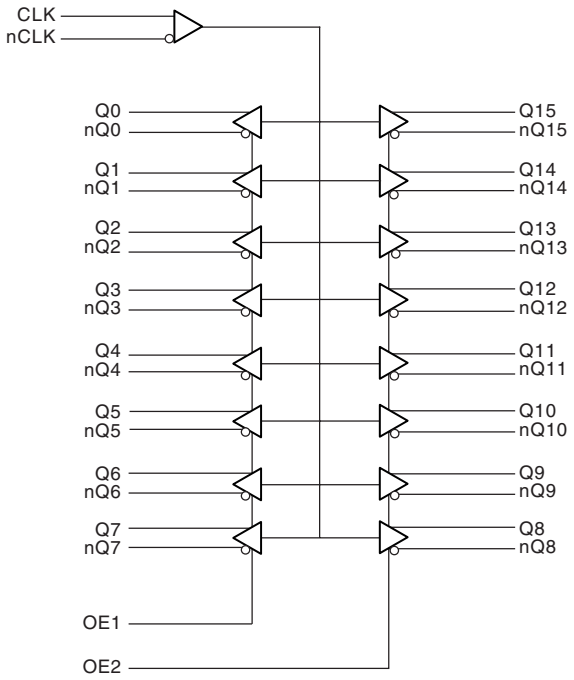
Dual output enable inputs allow the ICS8516 to be used in a 1-to-16 or 1-to-8 input/output mode.

Guaranteed output and part-to-part skew specifications make the ICS8516 ideal for those applications demanding well defined performance and repeatability.

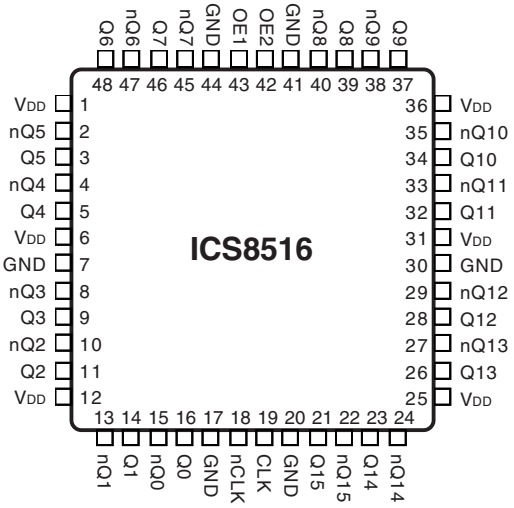
FEATURES

- 16 Differential 3.3V LVDS outputs
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: 700MHz
- Translates any differential input signal (LVPECL, LVHSTL, SSTL, DCM) to LVDS levels without external bias networks
- Translates any single-ended input signal to LVDS with resistor bias on nCLK input
- Multiple output enable inputs for disabling unused outputs in reduced fanout applications
- Designed to meet or exceed the requirements of ANSI TIA/EIA-644
- Output skew: 200ps (maximum)
- Part-to-part skew: TBD
- Propagation delay: 2.9ns (maximum)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



48-Lead LQFP
7mm x 7mm x 1.4mm
Y Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 6, 12, 25, 31, 36	V_{DD}	Power		Positive supply pins. Connect to 3.3V.
2, 3	nQ5, Q5	Output		Differential output pair. LVDS interface levels.
4, 5	nQ4, Q4	Output		Differential output pair. LVDS interface levels.
7, 17, 20, 30, 41, 44	GND	Power		Power supply ground. Connect to ground.
8, 9	nQ3, Q3	Output		Differential output pair. LVDS interface levels.
10, 11	nQ2, Q2	Output		Differential output pair. LVDS interface levels.
13, 14	nQ1, Q1	Output		Differential output pair. LVDS interface levels.
15, 16	nQ0, Q0	Output		Differential output pair. LVDS interface levels.
18	nCLK	Input	Pullup	Inverting differential clock input.
19	CLK	Input	Pulldown	Non-inverting differential clock input.
21, 22	Q15, nQ15	Output		Differential output pair. LVDS interface levels.
23, 24	Q14, nQ14	Output		Differential output pair. LVDS interface levels.
26, 27	Q13, nQ13	Output		Differential output pair. LVDS interface levels.
28, 29	Q12, nQ12	Output		Differential output pair. LVDS interface levels.
32, 33	Q11, nQ11	Output		Differential output pair. LVDS interface levels.
34, 35	Q10, nQ10	Output		Differential output pair. LVDS interface levels.
37, 38	Q9, nQ9	Output		Differential output pair. LVDS interface levels.
39, 40	Q8, nQ8	Output		Differential output pair. LVDS interface levels.
42, 43	OE2, OE1	Input	Pullup	Output enable. OE2 controls outputs Q8, nQ8 thru Q15, nQ15; OE1 controls outputs Q0, nQ0 thru Q7, nQ7.

NOTE: *Pullup* and *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs		Outputs			
OE1	OE2	Q0 thru Q7	nQ0 thru nQ7	Q8 thru Q15	nQ8 thru nQ15
0	0	Hi Z	Hi Z	Hi Z	Hi Z
1	0	ACTIVE	ACTIVE	Hi Z	Hi Z
0	1	Hi Z	Hi Z	ACTIVE	ACTIVE
1	1	ACTIVE	ACTIVE	ACTIVE	ACTIVE

In the active mode, the state of the outputs are a function of the CLK and nCLK inputs as described in Table 3B.

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
CLK	nCLK	Q0 thru Q15	nQ0 thru nQ15		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section on page 10, Figure 13, which discusses wiring the differential input to accept single ended levels.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_{DD}	-0.5V to V_{DD} + 0.5V
Outputs, V_{DDO}	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			140		mA

TABLE 4B. LVCMOS DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	OE1, OE2		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	OE1, OE2		-0.3		0.8	V
I_{IH}	Input High Current	OE1, OE2	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	OE1, OE2	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	V_{IN} = V_{DD} = 3.465V			150	µA
		nCLK	V_{IN} = V_{DD} = 3.465V			5	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{TH}	Differential Input High Threshold Voltage					100	mV
V_{TL}	Differential Input Low Threshold Voltage			-100			mV
V_{PP}	Peak-to-Peak Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			0.5		V_{DD} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined ast V_{IH}.

TABLE 4D. LVDS DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			350		mV
ΔV_{OD}	V_{OD} Magnitude Change			0		mV
V_{OS}	Offset Voltage			1.25		V
ΔV_{OS}	V_{OS} Magnitude Change			5		mV
I_{OZ}	High Impedance Leakage Current			±1		µA
I_{OFF}	Power Off Leakage			±1		µA
I_{OSD}	Differential Output Short Circuit Current			-3.5		mA
I_{OS}	Output Short Circuit Current			-3.5		mA
V_{OH}	Output Voltage High; NOTE 1			1.34		V
V_{OL}	Output Voltage Low; NOTE 1			1.06		V

NOTE 1: Refer to page 6, Figure 1, 3.3V Output Load Test Circuit.

TABLE 5. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				700	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ TBD		2.4		ns
*t*sk(o)	Output Skew; NOTE 2, 4			150		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				TBD	ps
t_R	Output Rise Time	30% to 70% at 50MHz		500		ps
t_F	Output Fall Time	30% to 70% at 50MHz		500		ps
odc	Output Duty Cycle			50		%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

PARAMETER MEASUREMENT INFORMATION

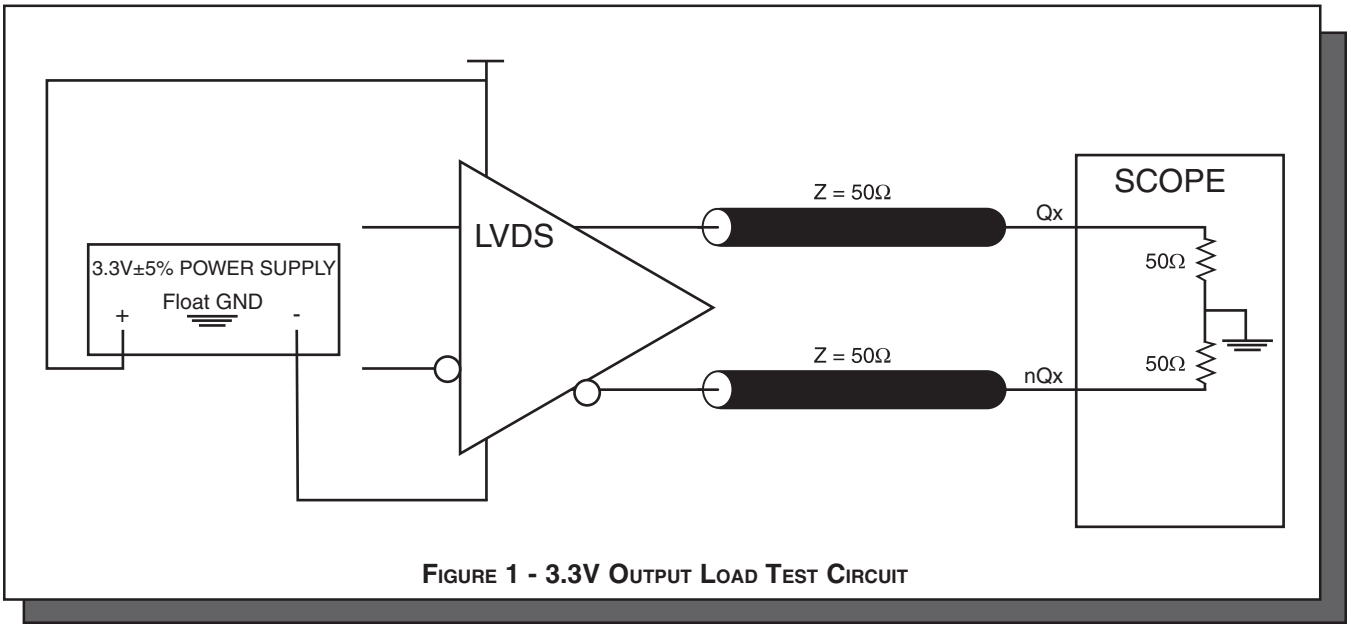


FIGURE 1 - 3.3V OUTPUT LOAD TEST CIRCUIT

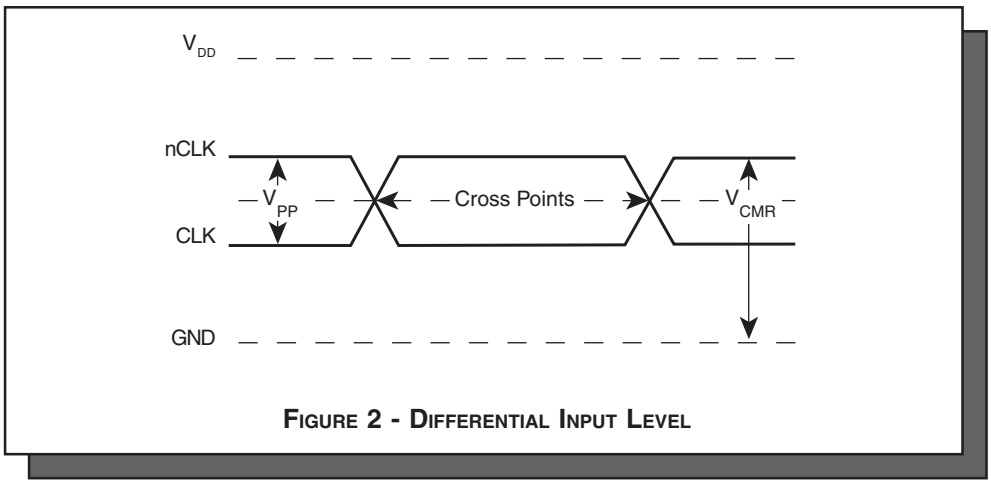


FIGURE 2 - DIFFERENTIAL INPUT LEVEL

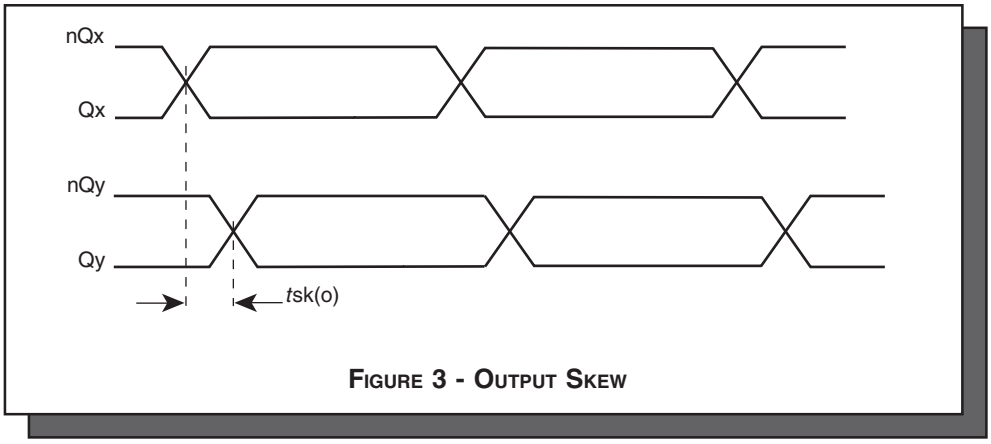


FIGURE 3 - OUTPUT SKEW

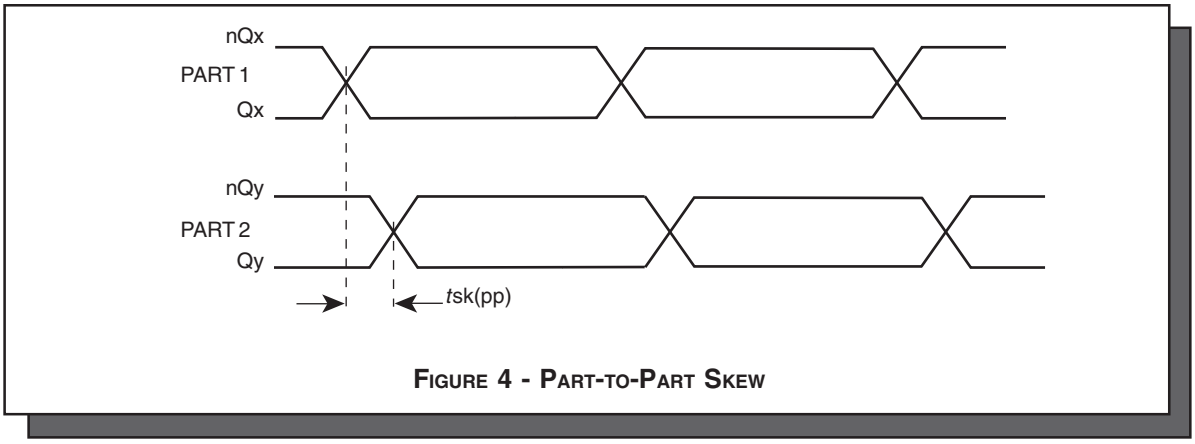


FIGURE 4 - PART-TO-PART SKEW

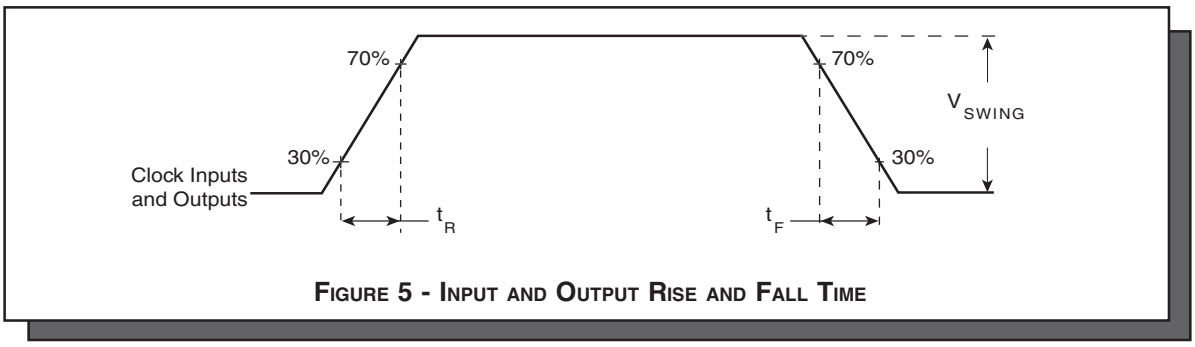


FIGURE 5 - INPUT AND OUTPUT RISE AND FALL TIME

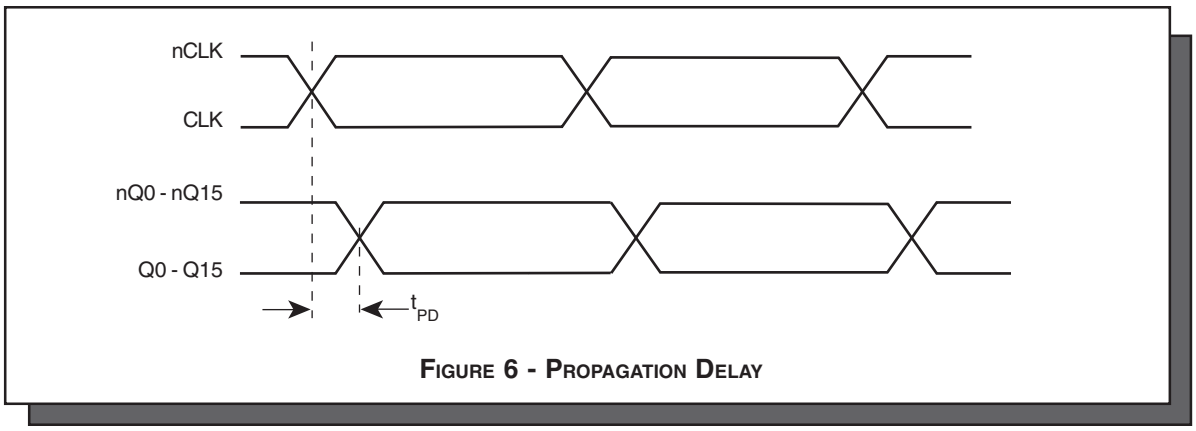


FIGURE 6 - PROPAGATION DELAY

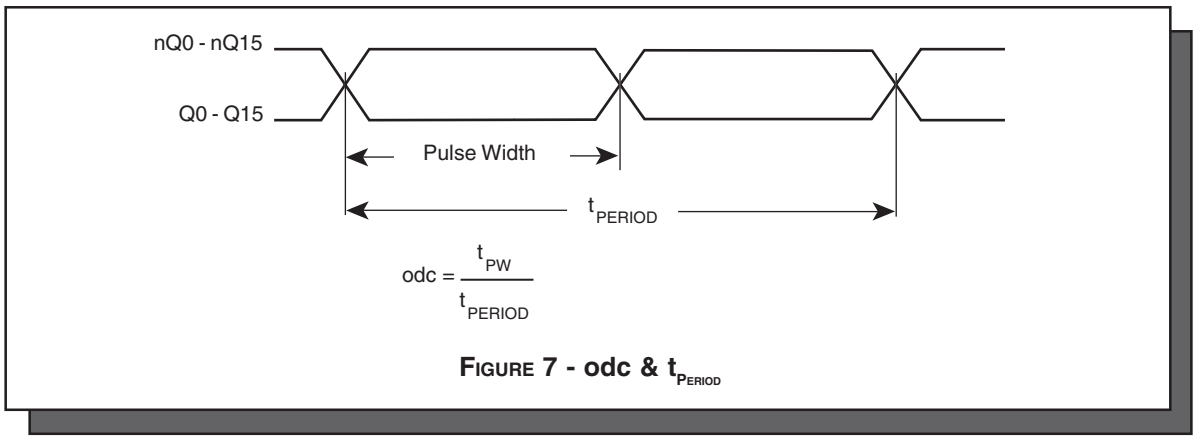


FIGURE 7 - odc & t_{PERIOD}

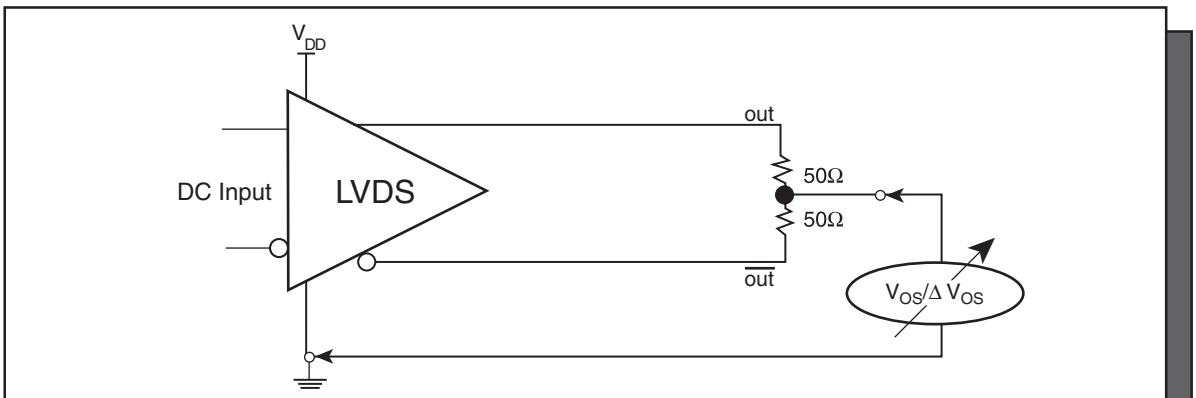


FIGURE 8 - V_{OS} / ΔVOS SETUP

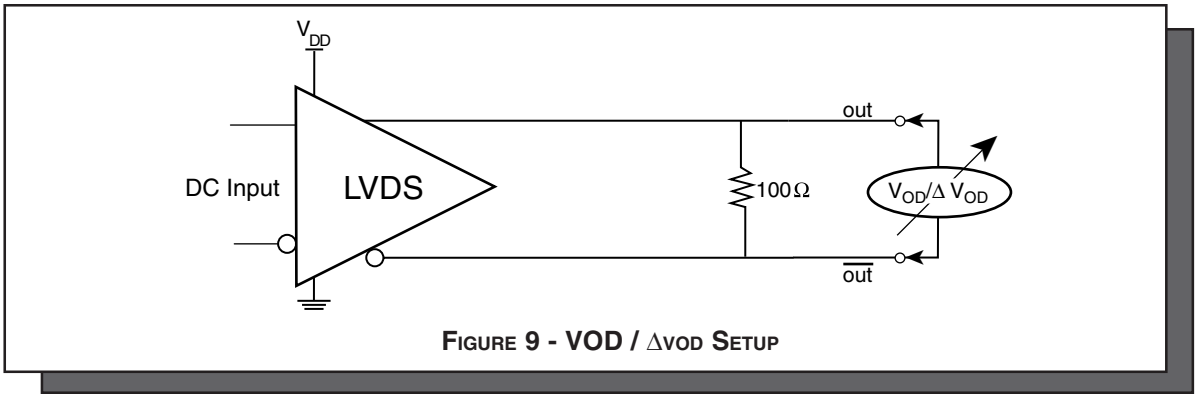


FIGURE 9 - VOD / ΔVOD SETUP

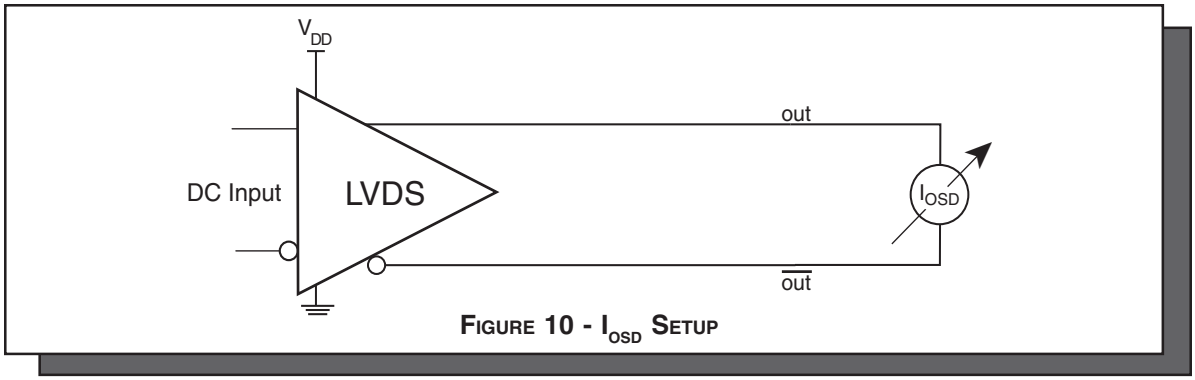


FIGURE 10 - I_{OSD} SETUP

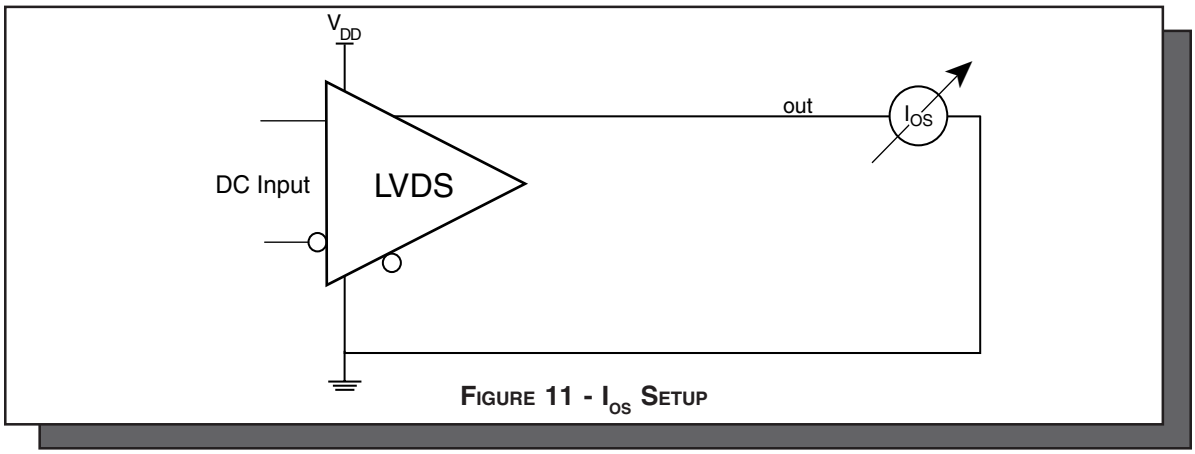


FIGURE 11 - I_{OS} SETUP

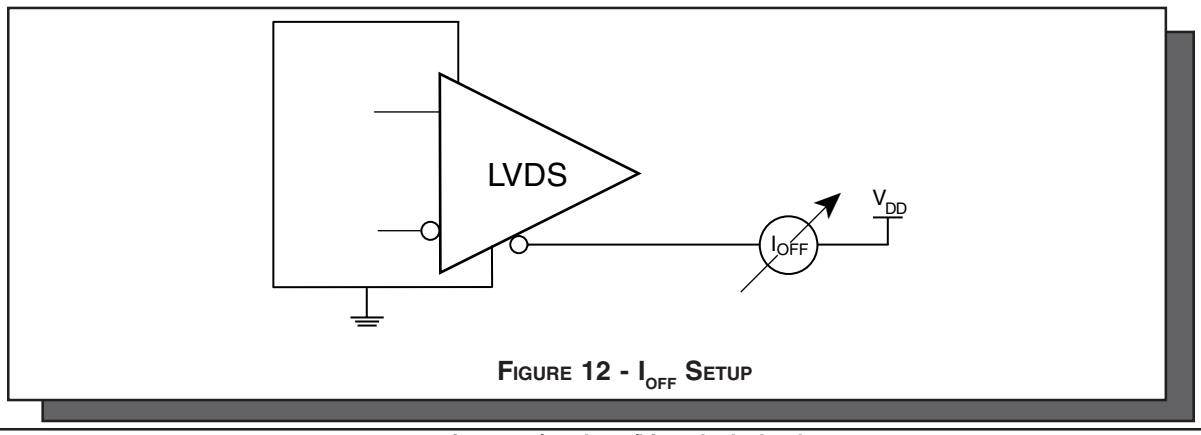


FIGURE 12 - I_{OFF} SETUP

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 13 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD}= 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

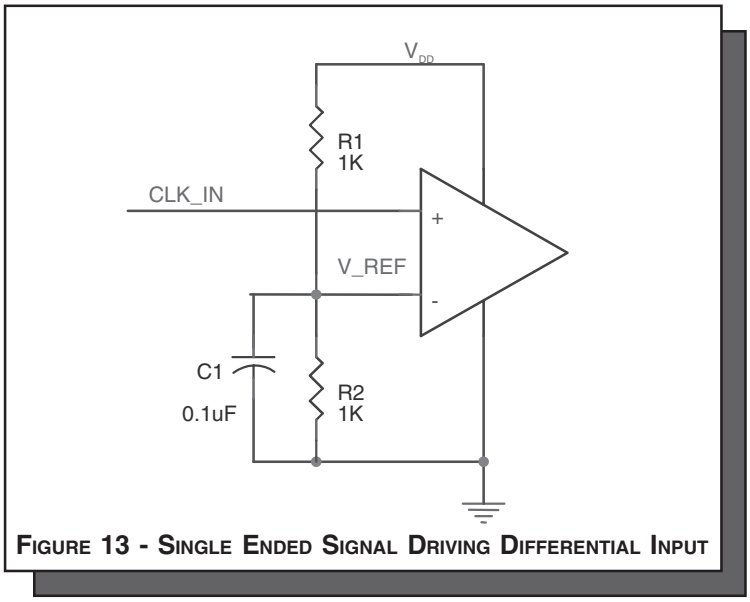


FIGURE 13 - SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

PACKAGE OUTLINE - Y SUFFIX

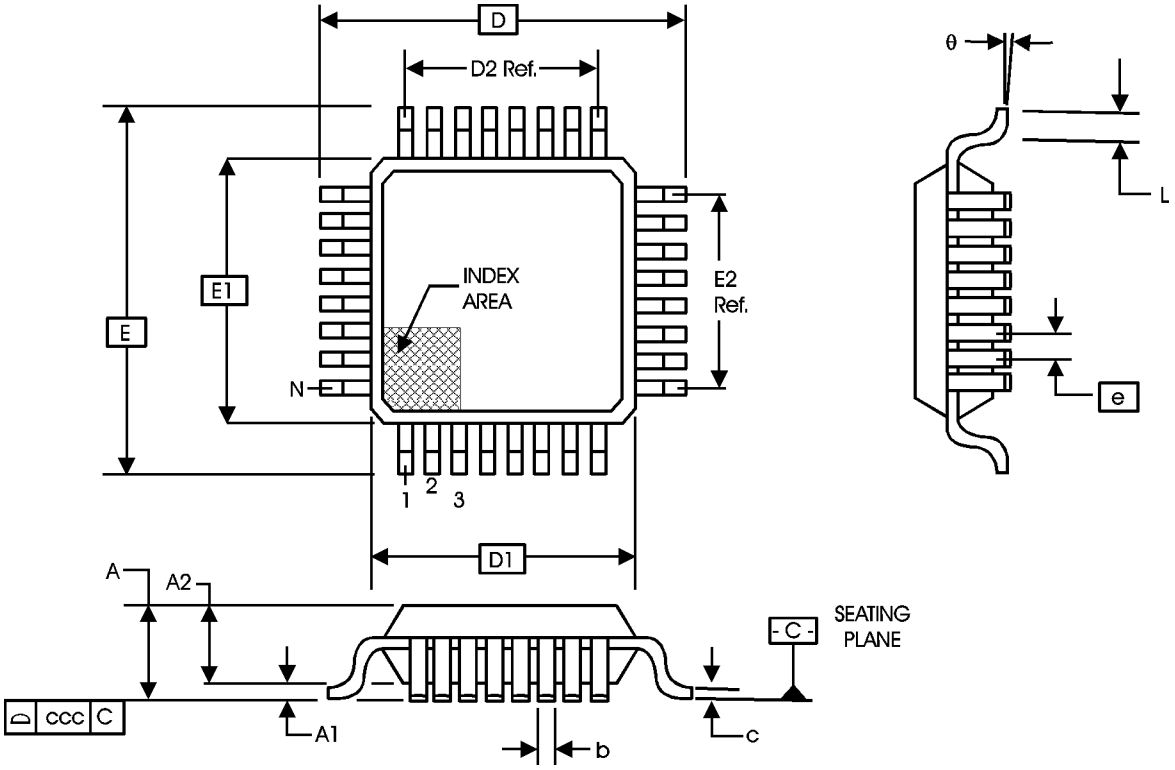


TABLE 6. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBC		
	MINIMUM	NOMINAL	MAXIMUM
N		48	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.50 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.50 Ref.	
e		0.50 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8516FY	ICS8516FY	48 Lead LQFP	250 per tray	0°C to 70°C
ICS8516FY-T	ICS8516FY	48 Lead LQFP on Tape and Reel	1000	0°C to 70°C