



### GENERAL DESCRIPTION



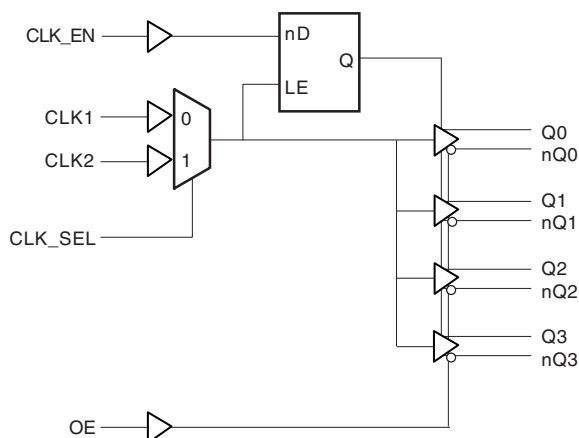
The ICS8545 is a low skew, high performance 1-to-4 LVCMOS-to-LVDS clock fanout buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. Utilizing Low Voltage Differential Signaling (LVDS) the ICS8545 provides a low power, low noise, solution for distributing clock signals over controlled impedances of 100Ω. The ICS8545 accepts a LVCMOS input level and translates it to 3.3V LVDS output levels.

Guaranteed output and part-to-part skew characteristics make the ICS8545 ideal for those applications demanding well defined performance and repeatability.

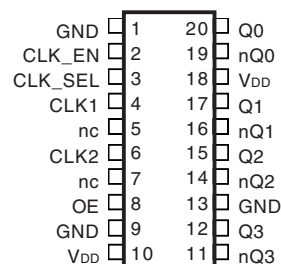
### FEATURES

- 4 LVDS outputs
- 2 LVCMOS clock inputs to support redundant or selectable frequency fanout applications
- Maximum output frequency up to 650MHz
- Translates LVCMOS input signals to LVDS levels
- Output skew: 40ps (maximum)
- Part-to-part skew: 500ps (maximum)
- Propagation delay: 3.6ns (maximum)
- Designed to meet or exceed the requirements of ANSI TIA/EIA-644
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

### BLOCK DIAGRAM



### PIN ASSIGNMENT



### ICS8545

#### 20-Lead TSSOP

6.5mm x 4.4mm x 0.92mm body package

#### G Package

Top View



**TABLE 1. PIN DESCRIPTIONS**

| Number   | Name            | Type   |          | Description                                                                                                                                                                 |
|----------|-----------------|--------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 9, 13 | GND             | Power  |          | Power supply ground. Connect to ground.                                                                                                                                     |
| 2        | CLK_EN          | Input  | Pullup   | Synchronizing clock enable. When HIGH, clock outputs follows clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVCMOS / LVTTTL interface levels. |
| 3        | CLK_SEL         | Input  | Pulldown | Clock select input. When HIGH, selects CLK2 input. When LOW, selects CLK1 input. LVCMOS / LVTTTL interface levels.                                                          |
| 4        | CLK1            | Input  | Pulldown | LVCMOS / LVTTTL clock input.                                                                                                                                                |
| 5, 7     | nc              | Unused |          | Unused pins.                                                                                                                                                                |
| 6        | CLK2            | Input  | Pulldown | LVCMOS / LVTTTL clock input.                                                                                                                                                |
| 8        | OE              | Input  | Pullup   | Output enable. Controls enabling and disabling of outputs Q0, nQ0 thru Q3, nQ3                                                                                              |
| 10, 18   | V <sub>DD</sub> | Power  |          | Positive supply pins. Connect to 3.3V.                                                                                                                                      |
| 11, 12   | nQ3, Q3         | Output |          | Differential output pair. LVDS interface levels.                                                                                                                            |
| 14, 15   | nQ2, Q2         | Output |          | Differential output pair. LVDS interface levels.                                                                                                                            |
| 16, 17   | nQ1, Q1         | Output |          | Differential output pair. LVDS interface levels.                                                                                                                            |
| 19, 20   | nQ0, Q0         | Output |          | Differential output pair. LVDS interface levels.                                                                                                                            |

NOTE: *Pullup* and *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

| Symbol                | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance       |                 |         |         | 4       | pF    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor   |                 |         | 51      |         | KΩ    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor |                 |         | 51      |         | KΩ    |

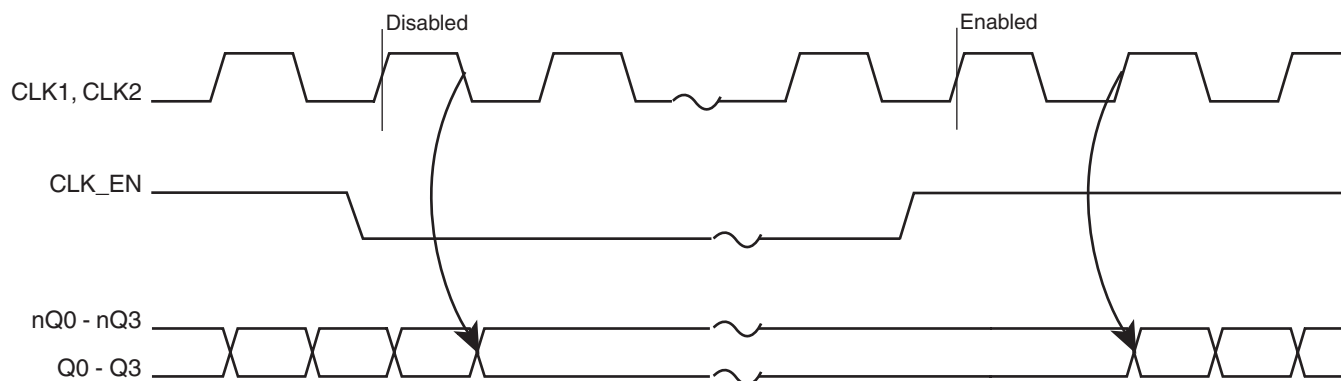


**TABLE 3A. CONTROL INPUT FUNCTION TABLE**

| Inputs |        |         |                 | Outputs    |              |
|--------|--------|---------|-----------------|------------|--------------|
| OE     | CLK_EN | CLK_SEL | Selected Source | Q1 thru Q3 | nQ1 thru nQ3 |
| 0      | X      | X       |                 | Hi Z       | Hi Z         |
| 1      | 0      | 0       | CLK1            | Low        | High         |
| 1      | 0      | 1       | CLK2            | Low        | High         |
| 1      | 1      | 0       | CLK1            | ACTIVE     | ACTIVE       |
| 1      | 1      | 1       | CLK2            | ACTIVE     | ACTIVE       |

After CLK\_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1.

In the active mode, the state of the outputs are a function of the CLK1 and CLK2 inputs as described in Table 3B.



**FIGURE 1 - CLK\_EN TIMING DIAGRAM**

**TABLE 3B. CLOCK INPUT FUNCTION TABLE**

| Inputs        | Outputs    |              |
|---------------|------------|--------------|
| CLK1 or CLK 2 | Q0 thru Q3 | nQ0 thru nQ3 |
| 0             | LOW        | HIGH         |
| 1             | HIGH       | LOW          |



#### ABSOLUTE MAXIMUM RATINGS

|                                          |                          |
|------------------------------------------|--------------------------|
| Supply Voltage, $V_{CCx}$                | 4.6V                     |
| Inputs, $V_I$                            | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, $V_O$                           | -0.5V to $V_{DD} + 0.5V$ |
| Package Thermal Impedance, $\theta_{JA}$ | 73.2°C/W (0 lfpm)        |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C           |

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol   | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-------------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$ | Positive Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $I_{DD}$ | Power Supply Current    |                 |         |         | 50      | mA    |

**TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol   | Parameter          | Test Conditions     | Minimum                        | Typical | Maximum        | Units   |
|----------|--------------------|---------------------|--------------------------------|---------|----------------|---------|
| $V_{IH}$ | Input High Voltage | CLK1, CLK2          | 2                              |         | $V_{DD} + 0.3$ | V       |
|          |                    | CLK_EN, CLK_SEL, OE | 2                              |         | $V_{DD} + 0.3$ | V       |
| $V_{IL}$ | Input Low Voltage  | CLK1, CLK2          | -0.3                           |         | 1.3            | V       |
|          |                    | CLK_EN, CLK_SEL, OE | -0.3                           |         | 0.8            | V       |
| $I_{IH}$ | Input High Current | CLK1, CLK2, CLK_SEL | $V_{DD} = V_{IN} = 3.465V$     |         | 150            | $\mu A$ |
|          |                    | CLK_EN, OE          | $V_{DD} = V_{IN} = 3.465V$     |         | 5              | $\mu A$ |
| $I_{IL}$ | Input Low Current  | CLK1, CLK2, CLK_SEL | $V_{DD} = 3.465V, V_{IN} = 0V$ | -5      |                | $\mu A$ |
|          |                    | CLK_EN, OE          | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150    |                | $\mu A$ |

NOTE: Outputs terminated with  $50\Omega$  to  $V_{DD}/2$ . See page 6, Figure 2, Output Load Test Circuit.

**TABLE 4C. LVDS DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol          | Parameter                                 | Test Conditions | Minimum | Typical | Maximum | Units   |
|-----------------|-------------------------------------------|-----------------|---------|---------|---------|---------|
| $V_{OD}$        | Differential Output Voltage               |                 | 200     | 350     | 360     | mV      |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change                 |                 |         |         | 40      | mV      |
| $V_{OS}$        | Offset Voltage                            |                 | 1.125   | 1.25    | 1.375   | V       |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change                 |                 |         | 5       | 25      | mV      |
| $I_{OZ}$        | High Impedance Leakage Current            |                 | -10     | $\pm 1$ | +10     | $\mu A$ |
| $I_{OFF}$       | Power Off Leakage                         |                 | -20     | $\pm 1$ | +20     | $\mu A$ |
| $I_{OSD}$       | Differential Output Short Circuit Current |                 |         | -3.5    | -5      | mA      |
| $I_{OS}$        | Output Short Circuit Current              |                 |         | -3.5    | -5      | mA      |
| $V_{OH}$        | Output Voltage High                       |                 |         | 1.34    | 1.6     | V       |
| $V_{OL}$        | Output Voltage Low                        |                 | 0.9     | 1.06    |         | V       |



**TABLE 5. AC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol       | Parameter                    | Test Conditions    | Minimum | Typical | Maximum | Units |
|--------------|------------------------------|--------------------|---------|---------|---------|-------|
| $f_{MAX}$    | Output Frequency             |                    |         |         | 650     | MHz   |
| $t_{PD}$     | Propagation Delay; NOTE 1    | $f \leq 650MHz$    | 1.4     |         | 3.6     | ns    |
| $t_{sk(o)}$  | Output Skew; NOTE 2, 4       |                    |         |         | 40      | ps    |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 3, 4 |                    |         |         | 500     | ps    |
| $t_R$        | Output Rise Time             | 20% to 80% @ 50MHz | 200     | 400     | 600     | ps    |
| $t_F$        | Output Fall Time             | 20% to 80% @ 50MHz | 200     | 400     | 600     | ps    |
| odc          | Output Duty Cycle            |                    | 45      | 50      | 55      | %     |

All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 1: Measured from the  $V_{DD}/2$  of the input to the differential output crossing point.

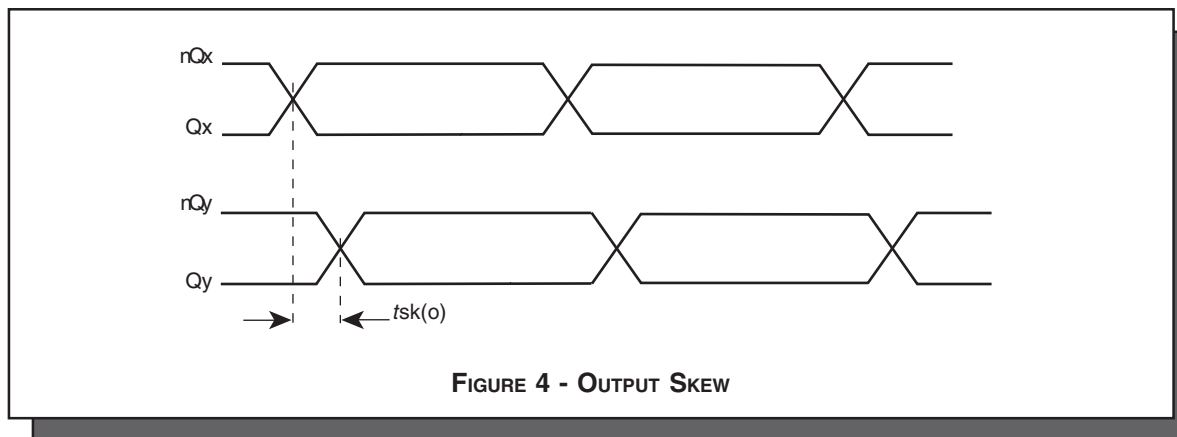
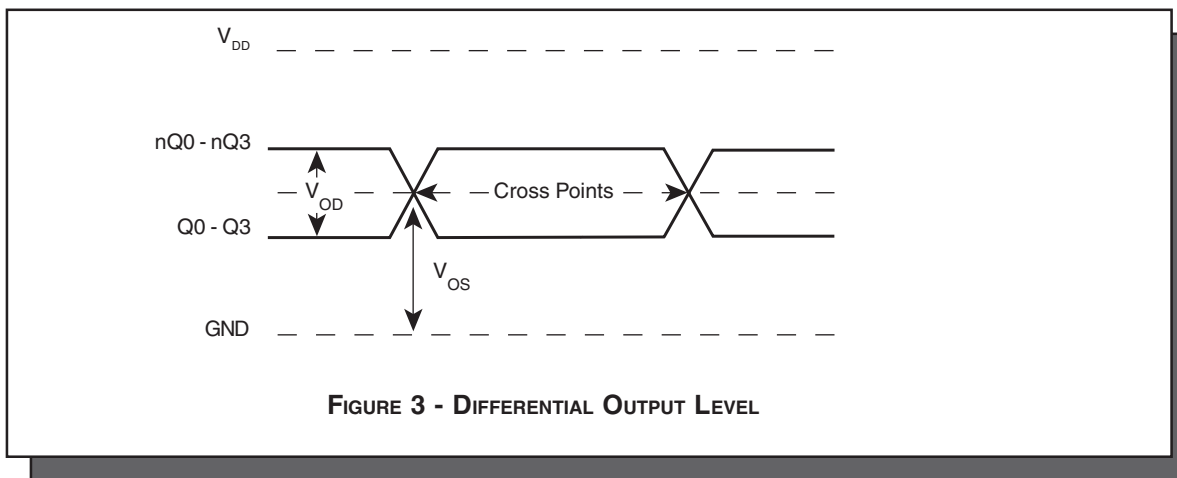
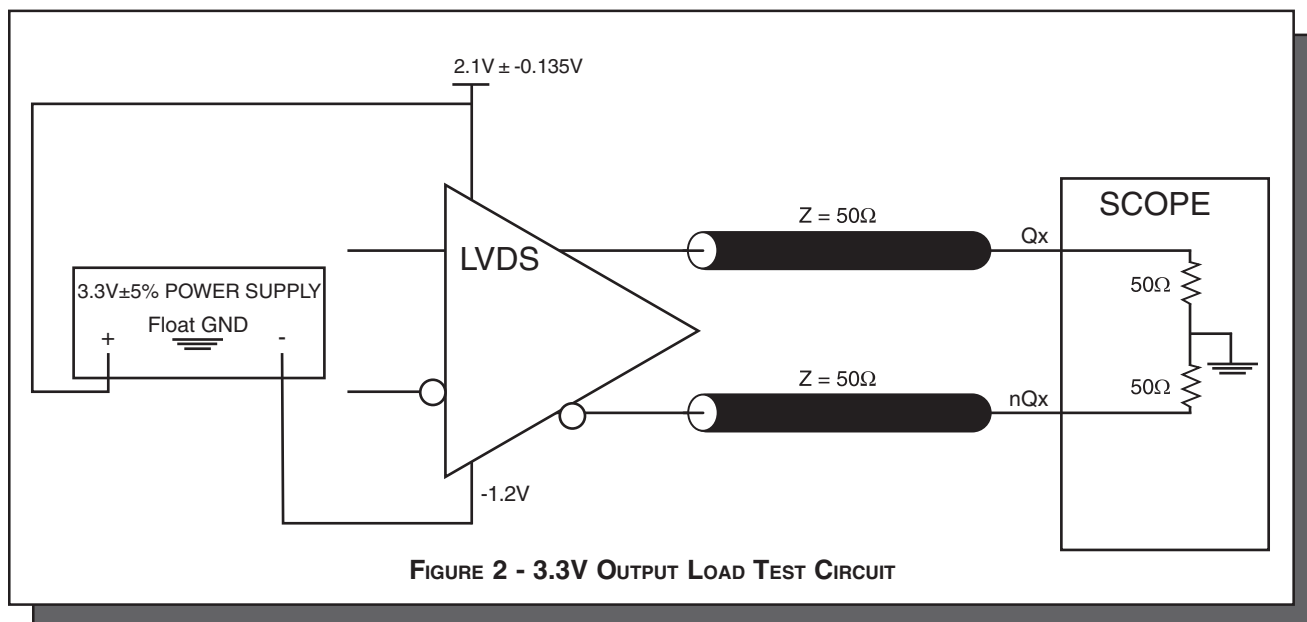
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.  
Measured at  $V_{DD}/2$  of the input to the differential output crossing point.

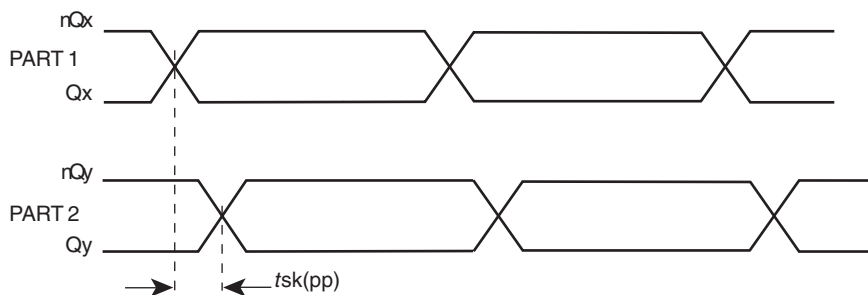
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

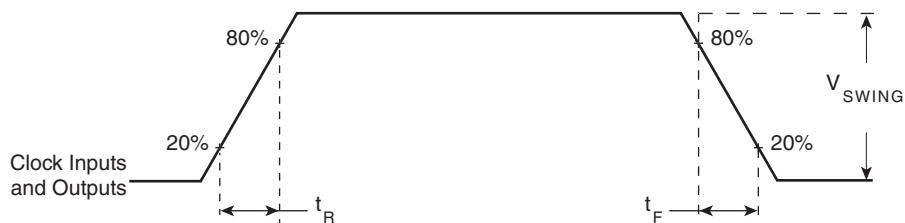


## PARAMETER MEASUREMENT INFORMATION

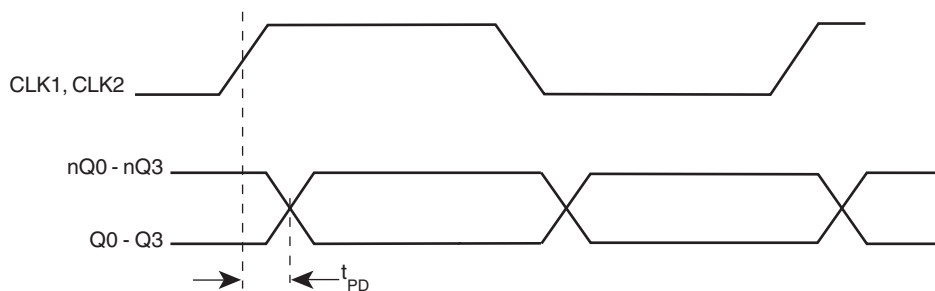




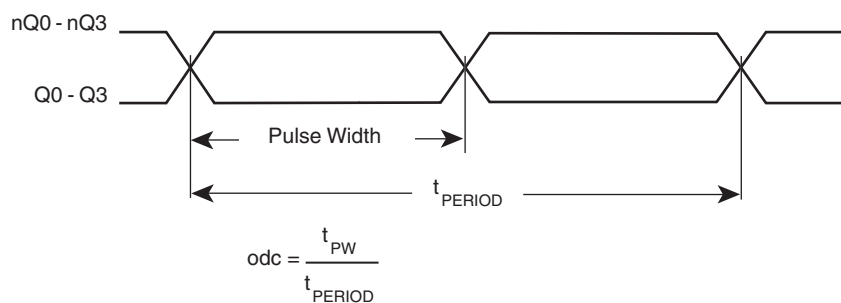
**FIGURE 5 - PART-TO-PART SKEW**



**FIGURE 6 - INPUT AND OUTPUT RISE AND FALL TIME**



**FIGURE 7 - PROPAGATION DELAY**



**FIGURE 8 - odc &  $t_{PERIOD}$**

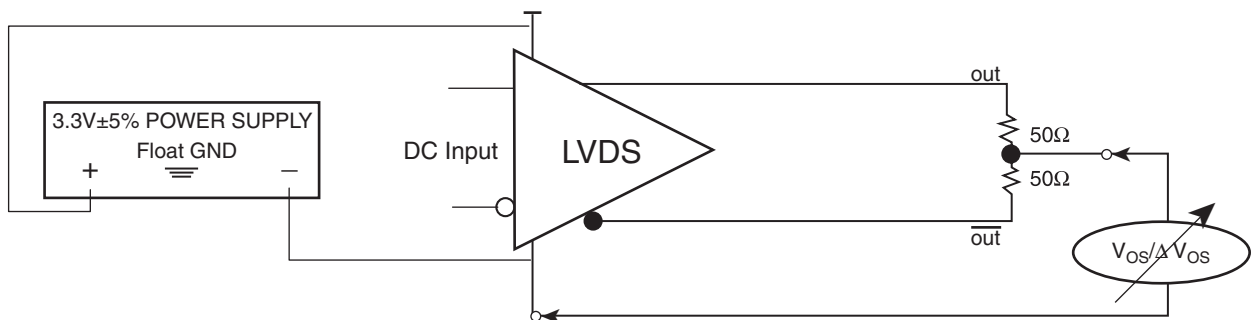


FIGURE 9 -  $V_{OS} / \Delta V_{OS}$  SETUP

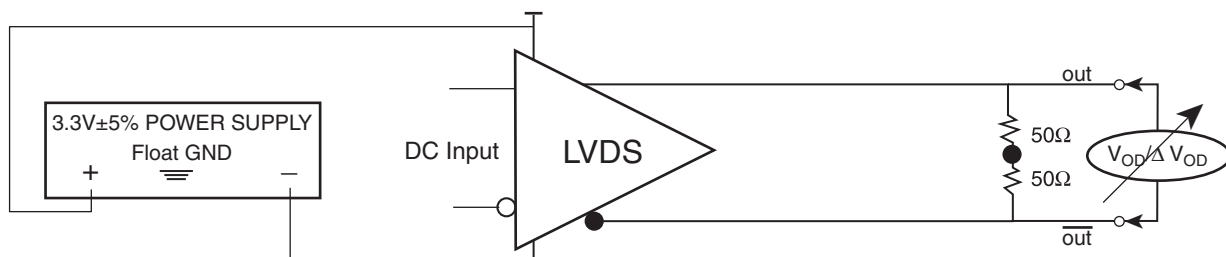


FIGURE 10 -  $V_{OD} / \Delta V_{OD}$  SETUP

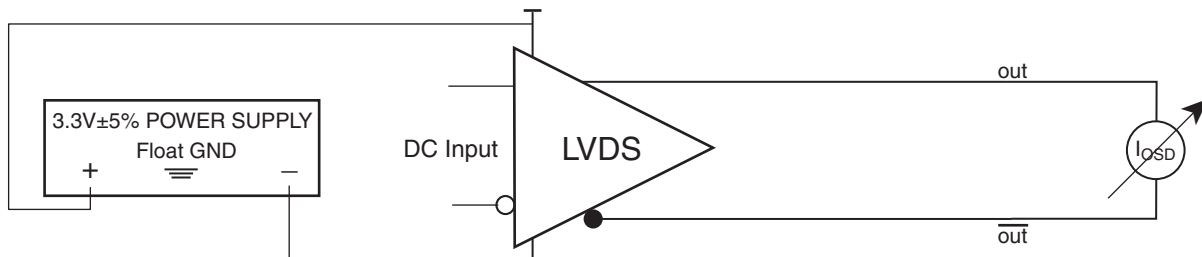


FIGURE 11 -  $I_{ODS}$  SETUP



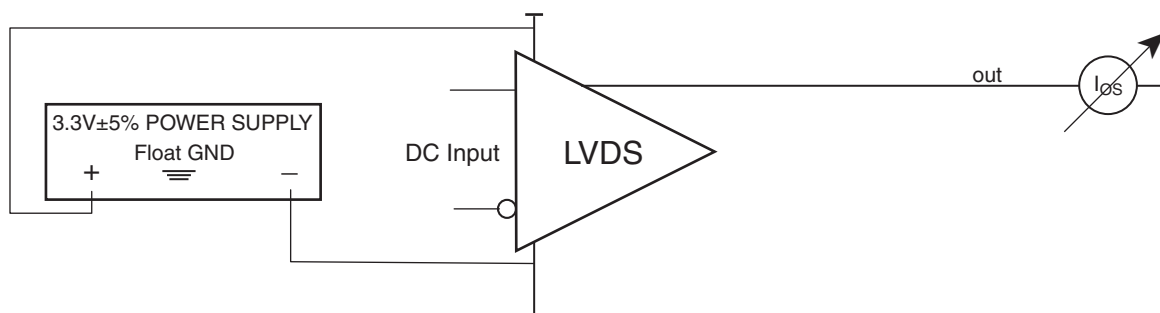


FIGURE 12 -  $I_{OS}$  SETUP

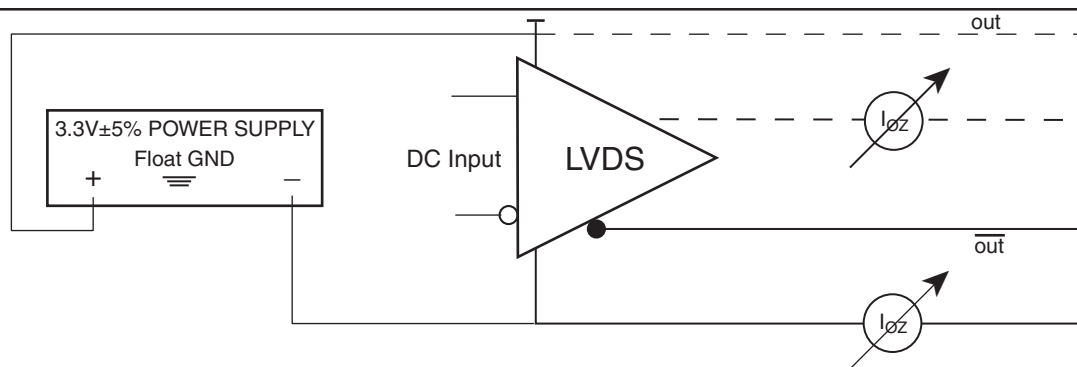


FIGURE 13 -  $I_{OZ}$  SETUP

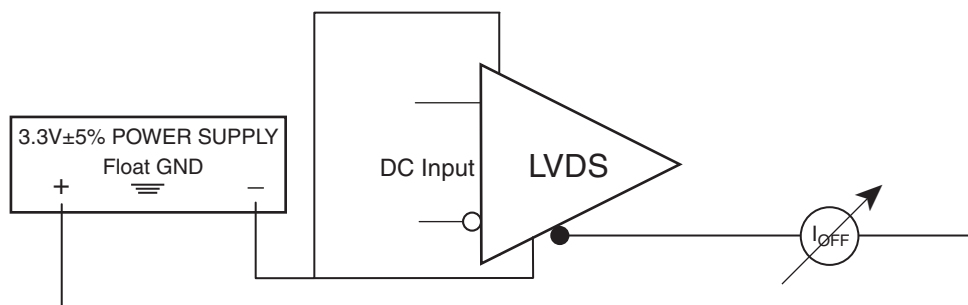


FIGURE 14 -  $I_{OFF}$  SETUP



## RELIABILITY INFORMATION

TABLE 6.  $\theta_{JA}$  VS. AIR FLOW TABLE

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) |           |          |          |
|----------------------------------------------------|-----------|----------|----------|
|                                                    | 0         | 200      | 500      |
| Single-Layer PCB, JEDEC Standard Test Boards       | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards        | 73.2°C/W  | 66.6°C/W | 63.5°C/W |

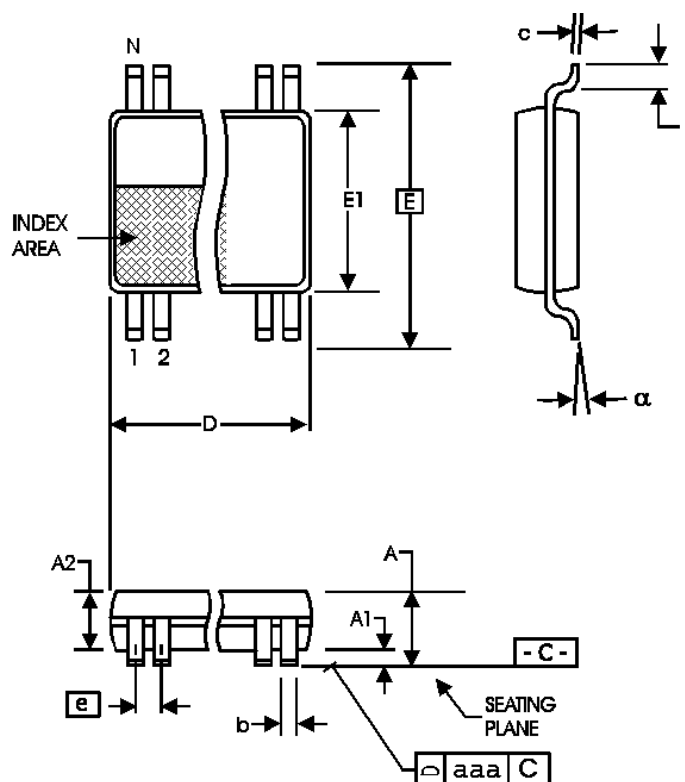
**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS8545 is: 644



**PACKAGE OUTLINE - G SUFFIX**



**TABLE 7. PACKAGE DIMENSIONS**

| SYMBOL   | Millimeters |      |
|----------|-------------|------|
|          | MIN         | MAX  |
| N        | 20          |      |
| A        | --          | 1.20 |
| A1       | 0.05        | 0.15 |
| A2       | 0.80        | 1.05 |
| b        | 0.19        | 0.30 |
| c        | 0.09        | 0.20 |
| D        | 6.40        | 6.60 |
| E        | 6.40 BASIC  |      |
| E1       | 4.30        | 4.50 |
| e        | 0.65 BASIC  |      |
| L        | 0.45        | 0.75 |
| $\alpha$ | 0°          | 8°   |
| aaa      | --          | 0.10 |

Reference Document: JEDEC Publication 95, MO-153



Integrated  
Circuit  
Systems, Inc.

# ICS8545

LOW SKEW, 1-TO-4  
LVCMOS-TO-LVDS FANOUT BUFFER

**TABLE 8. ORDERING INFORMATION**

| Part/Order Number | Marking   | Package                        | Count       | Temperature |
|-------------------|-----------|--------------------------------|-------------|-------------|
| ICS8545BG         | ICS8545BG | 20 lead TSSOP                  | 72 per tube | 0°C to 70°C |
| ICS8545BGT        | ICS8545BG | 20 lead TSSOP on Tape and Reel | 2500        | 0°C to 70°C |

While the information presented herein has been checked for both accuracy and reliability, Integrated Circuit Systems, Incorporated (ICS) assumes no responsibility for either its use or for infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by ICS. ICS reserves the right to change any circuitry or specifications without notice. ICS does not authorize or warrant any ICS product for use in life support devices or critical medical instruments.



Integrated  
Circuit  
Systems, Inc.

**ICS8545**  
LOW SKEW, 1-TO-4  
LVCMOS-TO-LVDS FANOUT BUFFER

| REVISION HISTORY SHEET |       |      |                                                                                         |          |
|------------------------|-------|------|-----------------------------------------------------------------------------------------|----------|
| Rev                    | Table | Page | Description of Change                                                                   | Date     |
| A                      | 4C    | 4    | In the $V_{OL}$ row, 1.06 has been moved to the Typical column from the maximum column. | 9/21/01  |
| A                      |       | 3    | Revised Figure 1, CLK_EN Timing Diagram.                                                | 10/17/01 |
| A                      |       | 3    | Revised Figure 1, CLK_EN Timing Diagram.                                                | 11/2/01  |