PRELIMINARY

Integrated Circuit Systems, Inc.

ICS83026

LOW SKEW, 1-TO-2 DIFFERENTIAL-TO-LVCMOS FANOUT BUFFER

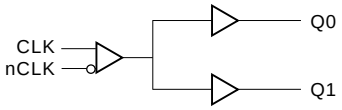
GENERAL DESCRIPTION

The ICS83026 is a low skew, 1-to-2 Differential-to-LVCMOS Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS.

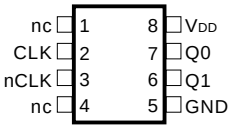
FEATURES

- 2 LVCMOS / LVTTL outputs
- Differential CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: 350MHz (typical)
- Output skew: 10ps (typical)
- Part-to-part skew: 500ps (typical)
- Small 8 lead SOIC package saves board space
- 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Pin-to-pin compatible with MC100EPT26

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS83026

8-Lead SOIC
3.8mm x 4.8mm, x 1.47mm package body
M Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 4	nc	Unused		No connect.
2	CLK	Input	Pulldown	Non-inverting differential clock input.
3	nCLK	Input	Pullup	Inverting differential clock input.
5	GND	Power		Power supply ground. Connect to ground.
6	Q1	Output		Single clock output. LVCMOS / LVTTL interface levels.
7	Q0	Output		Single clock output. LVCMOS / LVTTL interface levels.
8	V_{DD}	Power		Positive supply pin. Connect to 3.3V.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD} = 3.6V				pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
R_{OUT}	Output Impedance			7		Ω

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	112.7°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±0.3V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.0	3.3	3.6	V
I_{DD}	Power Supply Current			16		mA

TABLE 3B. LVCMOS / LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±0.3V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		2.6			V
V_{OL}	Output Low Voltage; NOTE 1				0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DD}/2$. See Parameter Measurement Information, 3.3V Output Load Test Circuit.

TABLE 3C. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 3.3V±0.3V, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK	$V_{IN} = V_{DD} = 3.6V$			5	µA
		CLK	$V_{IN} = V_{DD} = 3.6V$			150	µA
I_{IL}	Input Low Current	nCLK	$V_{IN} = 0V, V_{DD} = 3.6V$	-150			µA
		CLK	$V_{IN} = 0V, V_{DD} = 3.6V$	-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

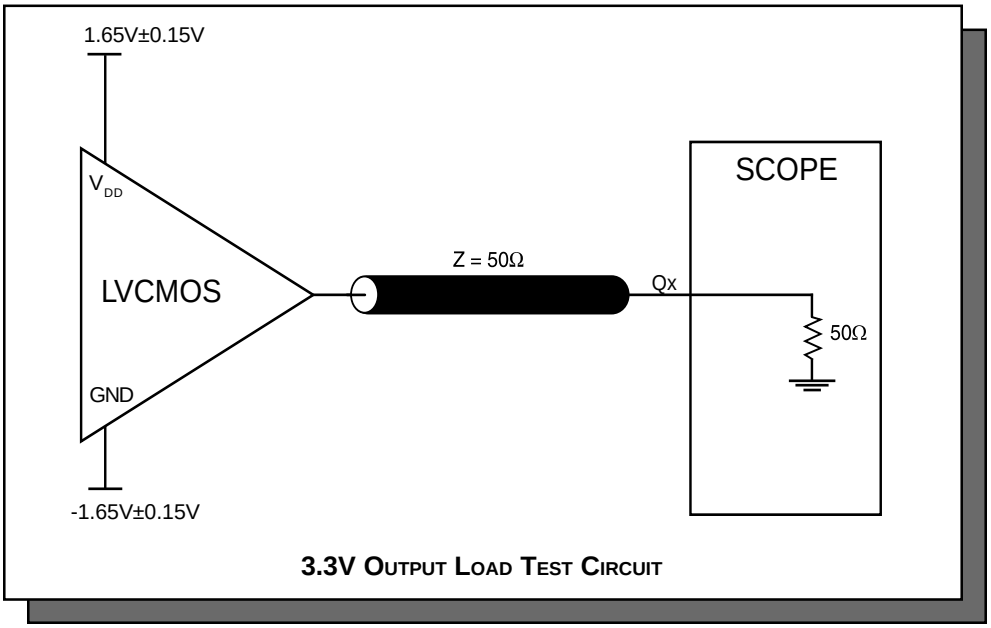
NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4. AC CHARACTERISTICS, V_{DD} = 3.3V±0.3V, T_A = -40°C TO 85°C

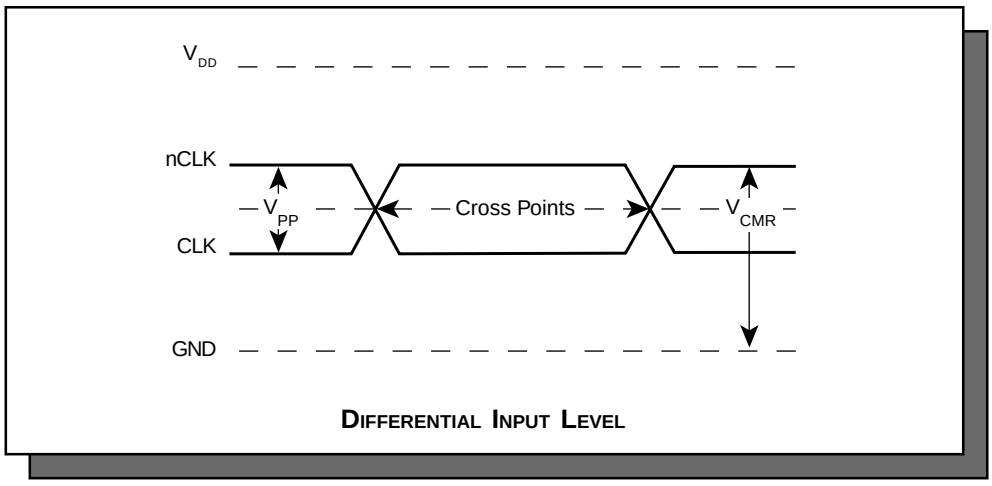
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			350		MHz
t_{PD}	Propagation Delay, NOTE 1	$f \leq$ 350MHz		2.8		ns
*t*sk(o)	Output Skew; NOTE 2, 4			10		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				500	ps
t_R	Output Rise Time	0.8V to 2V		250		ps
t_F	Output Fall Time	0.8V to 2V		250		ps
odc	Output Duty Cycle			50		%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at $V_{DD}/2$.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DD}/2$.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DD}/2$.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

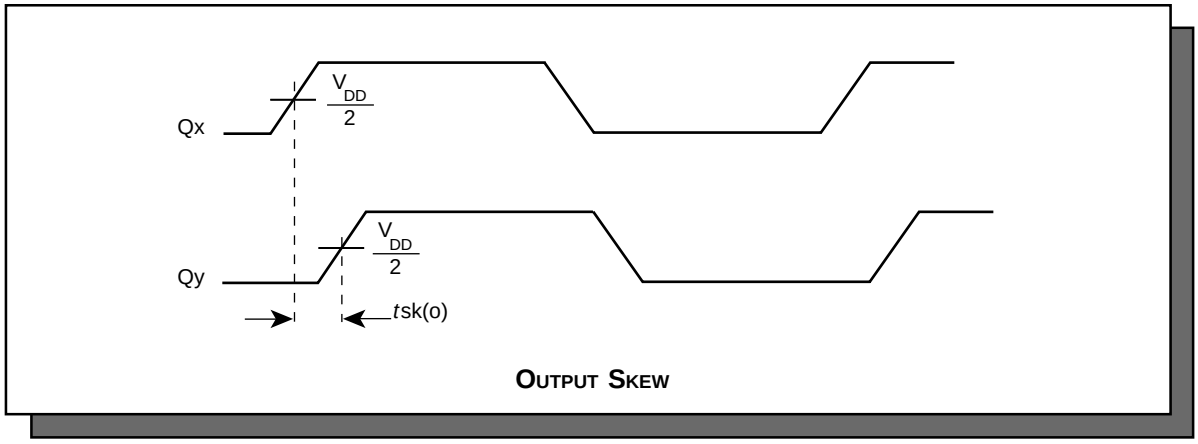
PARAMETER MEASUREMENT INFORMATION



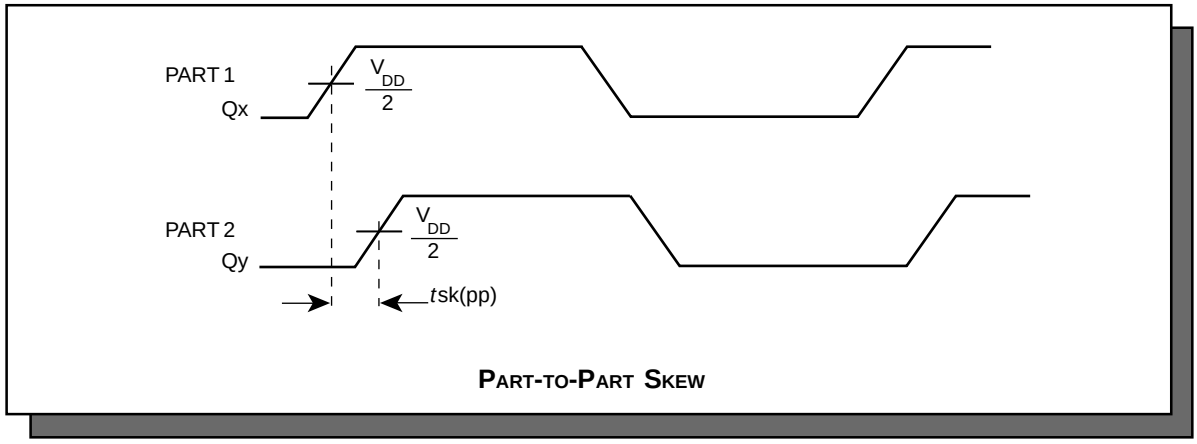
3.3V OUTPUT LOAD TEST CIRCUIT



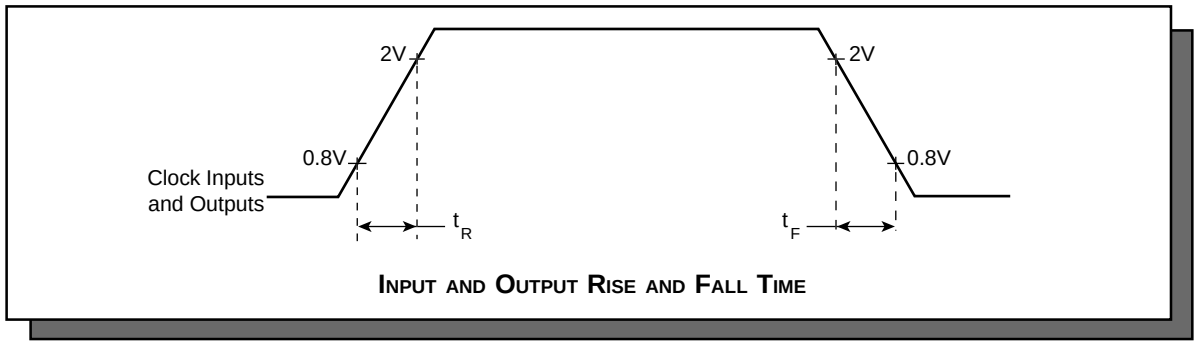
DIFFERENTIAL INPUT LEVEL



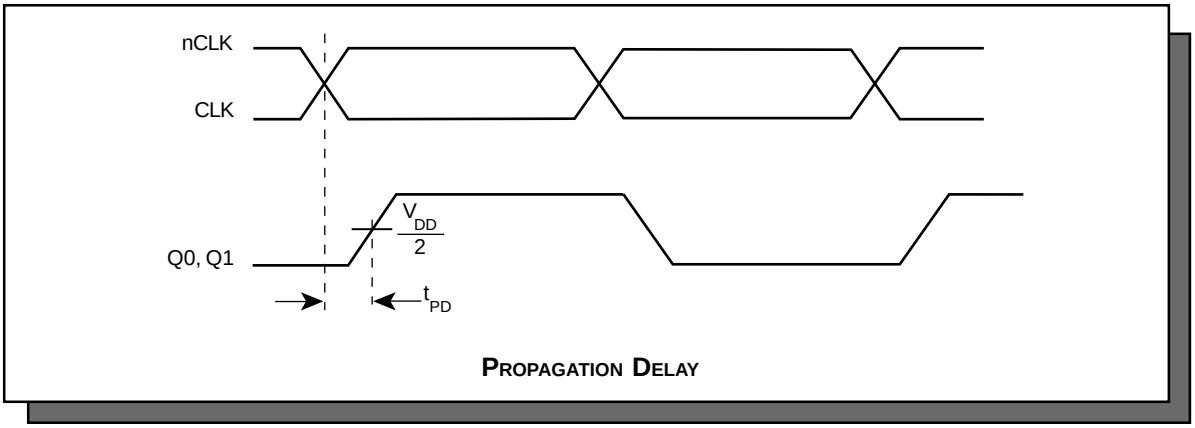
OUTPUT SKEW



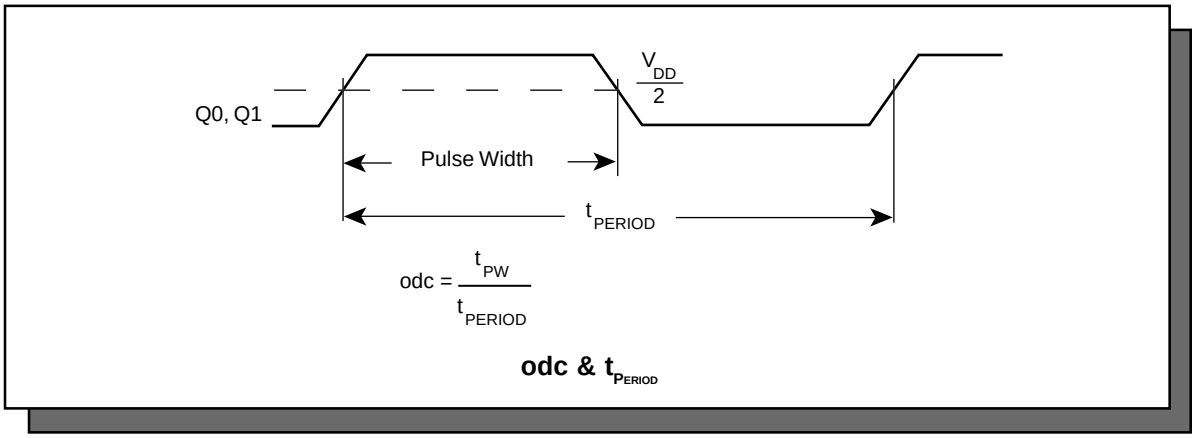
PART-TO-PART SKEW



INPUT AND OUTPUT RISE AND FALL TIME



PROPAGATION DELAY



odc & t_{PERIOD}

TABLE 5. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS83026 is: 416

PACKAGE OUTLINE - SUFFIX M

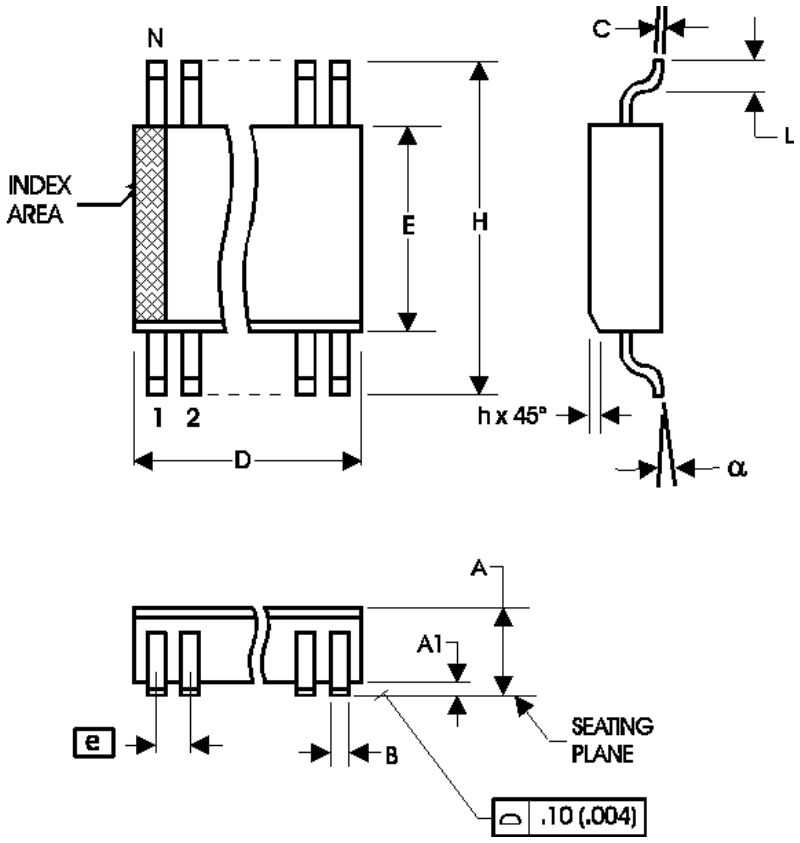


TABLE 6. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MINIMUM	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS83026AM	83026AM	8 lead SOIC	96 per tube	-40°C to 85°C
ICS83026AMT	83026AM	8 lead SOIC on Tape and Reel	2500	-40°C to 85°C