PRELIMINARY

Integrated
Circuit
Systems, Inc.

ICS8432-51

700MHz, Crystal-to-3.3V Differential LVPECL Frequency Synthesizer

General Description

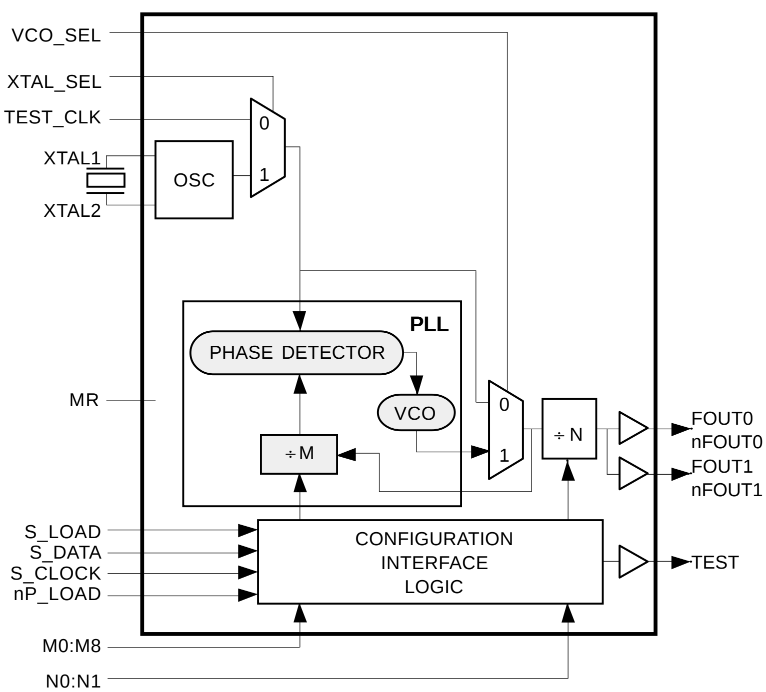
HiPerClockS™

The ICS8432-51 is a general purpose, dual output Crystal-to-3.3V Differential LVPECL High Frequency Synthesizer and a member of the HiPerClockS™ family of High Performance Clocks Solutions from ICS. The ICS8432-51 has a selectable TEST_CLK or crystal inputs. The TEST_CLK input accepts LVCMOS or LVTTL input levels and translates them to 3.3V LVPECL levels. The VCO operates at a frequency range of 200MHz to 700MHz. The VCO frequency is programmed in steps equal to the value of the input reference or crystal frequency. The VCO and output frequency can be programmed using the serial or parallel interfaces to the configuration logic. The low phase noise characteristics of the ICS8432-51 makes it an ideal clock source for Gigabit Ethernet, Fiber Channel 1 and 2, and Infiniband applications.

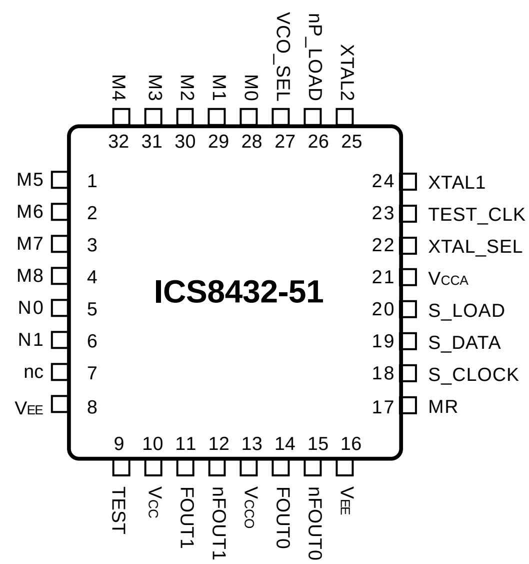
Features

- Dual differential 3.3V LVPECL output
- Selectable crystal oscillator interface or LVCMOS TEST_CLK
- TEST_CLK can accept the following input levels: LVCMOS or LVTTL
- Maximum output frequency up to 700MHz
- Maximum crystal or TEST_CLK input frequency up to 25MHz
- VCO range: 200MHz to 700MHz
- Parallel or serial interface for programming counter and output dividers
- RMS period jitter: TBDps (typical)
- Cycle-to-cycle jitter: 30ps (typical)
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature

Block Diagram



Pin Assignment



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

Functional Description

NOTE: The functional description that follows describes operation using a 25MHz crystal. Valid PLL loop divider values for different crystal or input frequencies are defined in the Input Frequency Characteristics, Table 6, NOTE 1.

The ICS8432-51 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A fundamental crystal is used as the input to the on-chip oscillator. The output of the oscillator is fed into the phase detector. A 25MHz crystal provides a 25MHz phase detector reference frequency. The VCO of the PLL operates over a range of 200MHz to 700MHz. The output of the loop divider is also applied to the phase detector.

The phase detector and the loop filter divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVPECL output buffers. The divider provides a 50% output duty cycle.

The programmable features of the ICS8432-51 support two input modes and programmable PLL loop divider and output divider. The two input operational modes are parallel and serial. *Figure 1* shows the timing diagram for each mode. In parallel mode the nP_LOAD input is initially LOW. The data on inputs M0 through M8 and N0 and N1 is passed directly to the ripple counter. On the LOW-to-HIGH transition of the nP_LOAD input the data is latched and the ripple counter remains loaded until the next LOW transition on nP_LOAD or until a serial event occurs. As a result the M and N bits can be hardwired to set the ripple counter to a specific default state that will automatically occur during power-up. The TEST output is LOW when operating in the parallel input mode. The relationship between the VCO frequency, the crystal frequency and the loop divider is defined as follows:

$$fVCO = fxtal \times M$$

The M count and the required values of M0 through M8 are shown in Table 4B, Programmable VCO Frequency Function. Valid M values for which the PLL will achieve lock for a 25MHz reference are defined as $8 \leq M \leq 28$. The frequency out is defined as follows:

$$FOUT = \frac{fVCO}{N} = fxtal \times \frac{M}{N}$$

Serial operation occurs when nP_LOAD is HIGH and S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the ripple counter when S_LOAD transitions from LOW-to-HIGH. The ripple counter divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH data at the S_DATA input is passed directly to the ripple counter on each rising edge of S_CLOCK. The serial mode can be used to program the M and N bits and test bits T1 and T0. The internal registers T0 and T1 determine the state of the TEST output as follows:

T1	T0	TEST Output
0	0	LOW
0	1	S_Data
1	0	Output of M divider
1	1	CMOS Fout

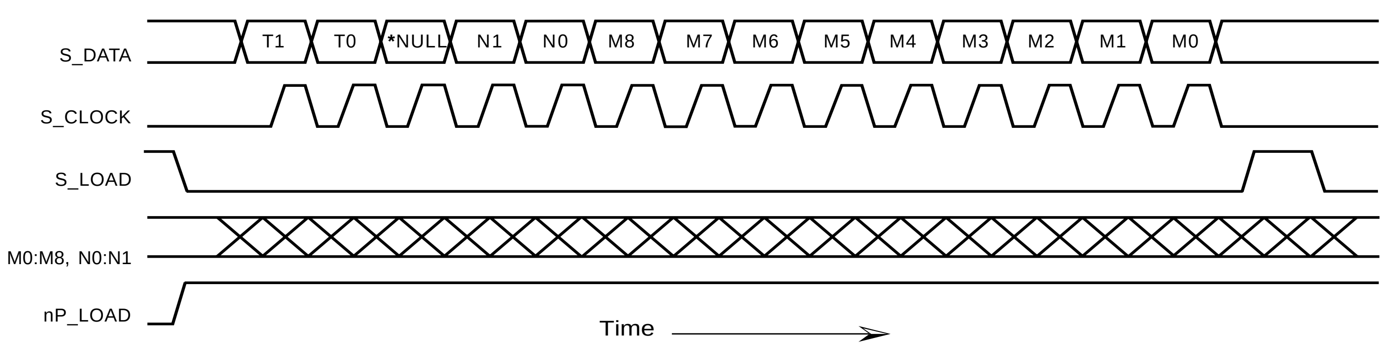


Figure 1. Parallel & Serial Load Operations

***NOTE:** The NULL timing slot must be observed.

Table 1. Pin Descriptions

Number	Name	Type		Description
1	M5	Input	Pullup	M counter/divider inputs. Data latched on LOW-to-HIGH transistion of nP_LOAD input. LVCMOS / LVTTL interface levels.
2, 3, 4, 28, 29, 30, 31, 32	M6, M7, M8, M0, M1, M2, M3, M4	Input	Pulldown	
5, 6	N0, N1	Input	Pulldown	Determines output divider value as defined in Table 4C Function table. LVCMOS / LVTTL interface levels.
7	nc	Unused		No connect.
8, 16	V_{EE}	Power		Negative supply pins. Connect to ground.
9	TEST	Output		Test output which is ACTIVE in the serial mode of operation. Output driven LOW in parallel mode. LVCMOS interface levels.
10	V_{CC}	Power		Positive supply pin.
11, 12	FOUT1, nFOUT1	Output		Differential output for the synthesizer. 3.3V LVPECL interface levels.
13	V_{CCO}	Power		Output supply pin. Connect to 3.3V.
14, 15	FOUT0, nFOUT0	Output		Differential output for the synthesizer. 3.3V LVPECL interface levels.
17	MR	Input	Pulldown	Forces outputs LOW, but does not effect loaded M, N, and T values. LVCMOS / LVTTL interface levels.
18	S_CLOCK	Input	Pulldown	Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLK.
19	S_DATA	Input	Pulldown	Shift register serial input. Data sampled on the rising edge of S_CLK.
20	S_LOAD	Input	Pulldown	Controls transition of data from shift register into the ripple counter. LVCMOS / LVTTL interface levels.
21	V_{CCA}	Power		Analog supply pin. Connect to 3.3V.
22	XTAL_SEL	Input	Pullup	Selects between crystal or test inputs as the PLL reference source. LVCMOS / LVTTL interface levels. Selects XTAL inputs when HIGH. Selects TEST_CLK when LOW.
23	TEST_CLK	Input	Pulldown	Test clock input. LVCMOS / LVTTL interface levels.
24, 25	XTAL1, XTAL2	Input		Crystal oscillator inputs.
26	nP_LOAD	Input	Pulldown	Parallel load input. Determines when data present at M8:M0 is loaded into ripple counter, and when data present at N1:N0 sets the output divide value. LVCMOS / LVTTL interface levels.
27	VCO_SEL	Input	Pullup	Determines whether synthesizer is in PLL or bypass mode. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

Table 3A. Parallel and Serial Mode Function Table

Inputs							Conditions
MR	nP_LOAD	M	N	S_LOAD	S_CLOCK	S_DATA	
H	X	X	X	X	X	X	Reset. M and N counters reset.
L	L	Data	Data	X	X	X	Data on M and N inputs passed directly to the ripple counter and output divider. TEST output forced LOW.
L	↑	Data	Data	L	X	X	Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs.
L	H	X	X	L	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
L	H	X	X	↑	L	Data	Contents of the shift register are passed to the ripple counter and output divider.
L	H	X	X	↓	L	Data	Ripple counter and output divide values are latched.
L	H	X	X	L	X	X	Parallel or serial input do not affect shift registers.

Table 3B. Programmable VCO Frequency Function Table

VCO Frequency (MHz)	M Count	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
200	8	0	0	0	0	0	1	0	0	0
225	9	0	0	0	0	0	1	0	0	1
250	10	0	0	0	0	0	1	0	1	0
275	11	0	0	0	0	0	1	0	1	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
650	26	0	0	0	0	1	1	0	1	0
675	27	0	0	0	0	1	1	0	1	1
700	28	0	0	0	0	1	1	1	0	0

NOTE 1: These M count values and the resulting frequency correspond to crystal or test clock input frequency of 25MHz.

Table 3C. Programmable Output Divider Function Table

Inputs		N Divider Value	Output Frequency (MHz)	
N1	N0		Minimum	Maximum
0	0	1	200	700
0	1	2	100	350
1	0	4	50	175
1	1	8	25	87.5

Absolute Maximum Ratings

Supply Voltage, V_{CCx}	4.6V
Inputs, V_{CC}	-0.5V to V_{CC} + 0.5 V
Outputs, V_{CCO}	-0.5V to V_{CCO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 5A. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				110	mA

Table 5B. LVCMOS / LVTTL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	All input pins, except for XTAL1 and XTAL2		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	All input pins, except for XTAL1 and XTAL2		-0.3		0.8	V
I_{IH}	Input High Current	M0-M4, M6-M8, N0, N1, MR, S_CLOCK, TEST_CLK, S_DATA, S_LOAD, nP_LOAD	*$V_{CCx} = V_{IN}$ = 3.465V			150	µA
		M5, XTAL_SEL, VCO_SEL	$V_{CCx} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	M0-M4, M6-M8, N0, N1, MR, S_CLOCK, TEST_CLK, S_DATA, S_LOAD, nP_LOAD	V_{CCx} = 3.465V, V_{IN} = 0V	-5			µA
		M5, XTAL_SEL, VCO_SEL	V_{CCx} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage	TEST	V_{CCx} = 3.135V, I_{OH} = -36mA	2.6			V
V_{OL}	Output Low Voltage	TEST	V_{CCx} = 3.135V, I_{OL} = 36mA			0.5	V

***NOTE 1:** V_{CCx} denotes V_{CC}, V_{CCA}, and V_{CCO}.

Table 5C. LVPECL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 2.1		V_{CCO} - 1.0	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} -1.6	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		0.85	V

NOTE 1: Outputs terminated with 50 Ω to V_{CCO} - 2V.

Table 6. Input Frequency Characteristics, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Maximum Input Frequency	TEST_CLK; NOTE 1		12		25	MHz
		XTAL1, XTAL2; NOTE 1		12		25	MHz
		S_CLOCK				50	MHz

NOTE 1: For the input crystal and TEST_CLK frequency range the M value must be set for the VCO to operate within the 200MHz to 700MHz range. Using the minimum input frequency of 12MHz valid values of M are $17 \le M \le 58$. Using the maximum frequency of 25MHz valid values of M are $8 \le M \le 28$.

Table 7. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		12		25	MHz
Equivalent Series Resistance (ESR)		50		80	Ω
Shunt Capacitance				7	pF
Series Pin Inductance		3		7	nH
Operating Temperature Range		0		70	°C

Table 8. AC Characteristics, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Maximum Output Frequency			25		700	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter, RMS; NOTE 1, 3				30		ps
*t*jit(per)	Period Jitter, RMS; NOTE 1, 3						ps
*t*sk(o)	Output Skew; NOTE 2, 3					10	ps
t_R	Output Rise Time		20% to 80% @ 50MHz	300		700	ps
t_F	Output Fall Time		20% to 80% @ 50MHz	300		700	ps
t_S	Setup Time	M, N to nP_LOAD				5	ns
		S_DATA to S_CLOCK				5	
		S_CLOCK to S_LOAD				5	
t_H	Hold Time	M, N to nP_LOAD				5	ns
		S_DATA to S_CLOCK				5	
		S_CLOCK to S_LOAD				5	
odc	Output Duty Cycle			47		53	%
t_{LOCK}	PLL Lock Time					10	ms

All parameters measured at 500MHz unless noted otherwise.
NOTE 1: Jitter performance using Xtal inputs.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

Parameter Measurement Information

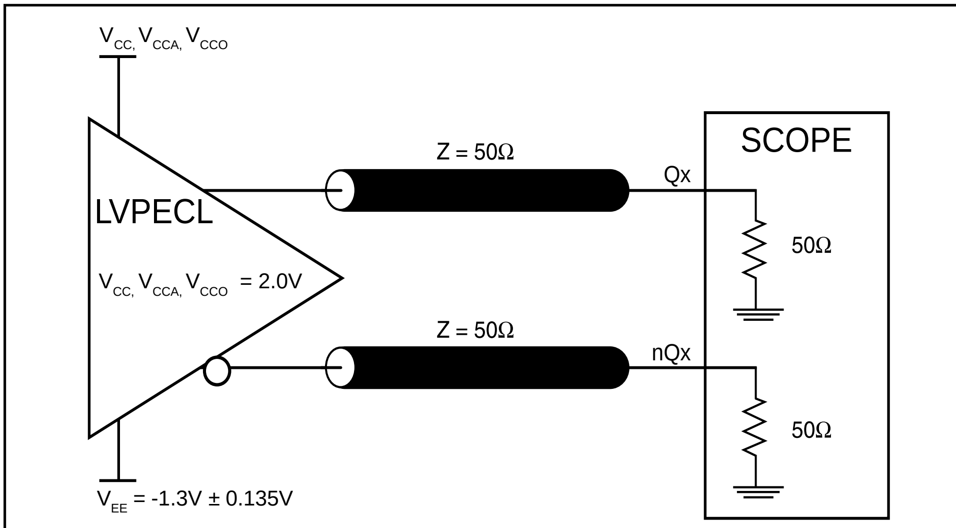


Figure 1 - 3.3V Output Load Test Circuit

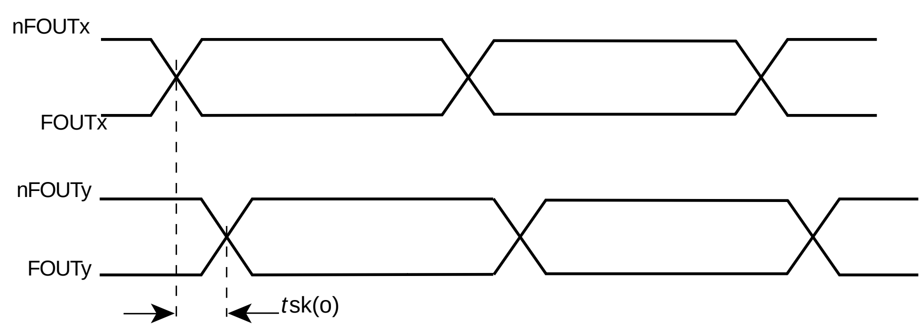
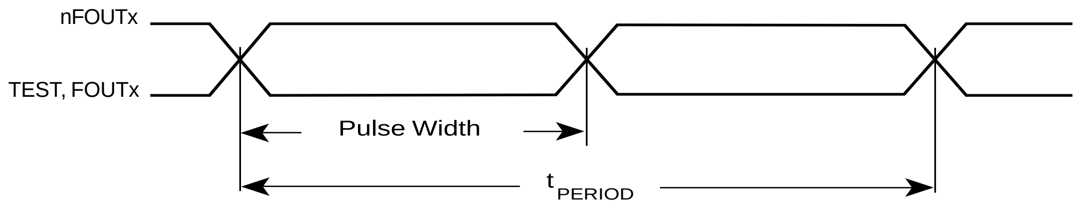


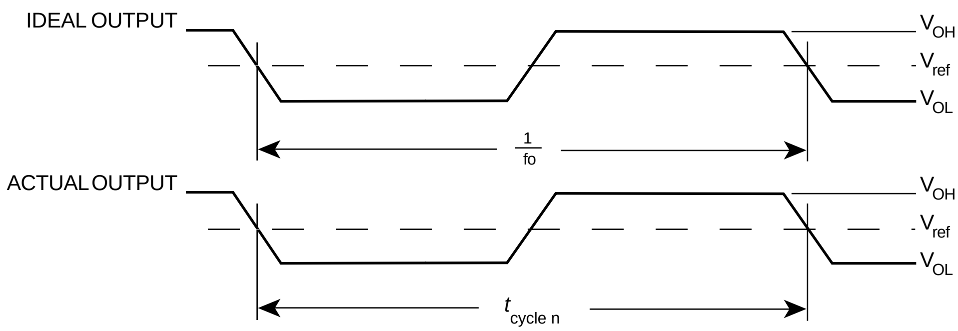
Figure 2 - Output Skew

Figure 3 - Input and Output Rise and Fall Time



$$\text{odc} = \frac{t_{PW}}{t_{PERIOD}}$$

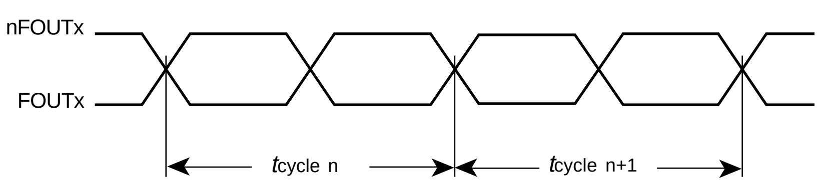
Figure 4 - odc & t_{PERIOD}



$$t\text{jit(per)} = \left| t_{cycle\ n} - \frac{1}{fo} \right|$$

where fo is the nominal output frequency and $t_{cycle\ n}$ is any cycle within the sample measured on controlled edges

Figure 5 - Period Jitter



$$t\text{jit(cc)} = t\text{cycle n} - t\text{cycle n+1}$$

Figure 6 - Cycle-to-Cycle Jitter

APPLICATIONS

STORAGE AREA NETWORKS

A variety of technologies are used for interconnection of the elements within a SAN. The tables below lists the common frequencies used as well as the settings for the ICS8432-51 to generate the appropriate frequency.

Table 9. Common SANs Applications Frequencies

Interconnect Technology	Clock Rate	Reference Freq. to SERDES (MHz)	Crystal Frequency (MHz)
Gigabit Ethernet	1.25 GHz	125, 250, 156.25	25, 25, 19.53
Fibre Channel	FC1 1.0625 GHz FC2 2.1250 GHz	106.25, 53.125, 132.81	16.6, 25, 26.563
Infiniband	2.5 GHz	125, 250	25, 25

Table 10. Configuration Details for SANs Applications

Interconnect Technology	Crystal Frequency (MHz)	ICS8432-01 Output Frequency to SERDES (MHz)	ICS8432-51 M & N Settings										
			M8	M7	M6	M5	M4	M3	M2	M1	M0	N1	N0
Gigabit Ethernet	25	125	0	0	0	0	0	1	0	1	0	1	0
	25	250	0	0	0	0	0	1	0	1	0	0	0
	19.53	156.25	0	0	0	0	1	0	0	0	0	1	0
Fiber Channel 1	25	53.125	0	0	0	0	1	0	0	0	1	1	1
	25	106.25	0	0	0	0	1	0	0	0	1	1	0
Fiber Channel 2	16.6	132.81	0	0	0	0	1	0	0	0	0	0	1
Infiniband	25	125	0	0	0	0	0	1	0	1	0	0	1
	25	250	0	0	0	0	0	1	0	1	0	0	0

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8432-51 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, better power supply isolation is required. *Figure 7* illustrates how a 10Ω along with a 10µF and a .01µF bypass capacitor should be connected to each power supply pin.

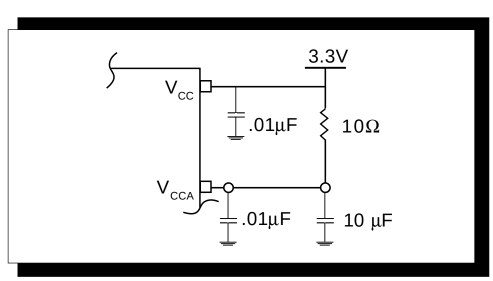


FIGURE 7. POWER SUPPLY FILTERING

Termination for LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. There are a few simple termination schemes. *Figures 8A and 8B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

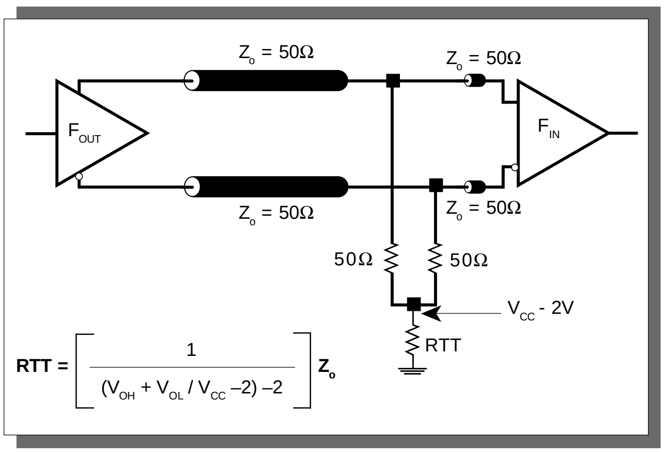


Figure 8A. LVPECL Output Termination

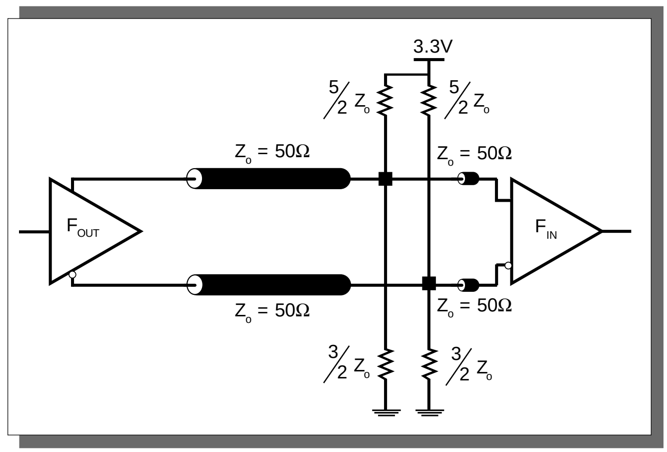


Figure 8B. LVPECL Output Termination

Layout Guideline

The schematic of the ICS8432-51 layout example used in this layout guideline is shown in *Figure 9A.* The ICS8432-51 recommended PCB board layout for this example is shown in *Figure 9B.* This layout example is used as a general guideline. The layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stacking of the P.C. board.

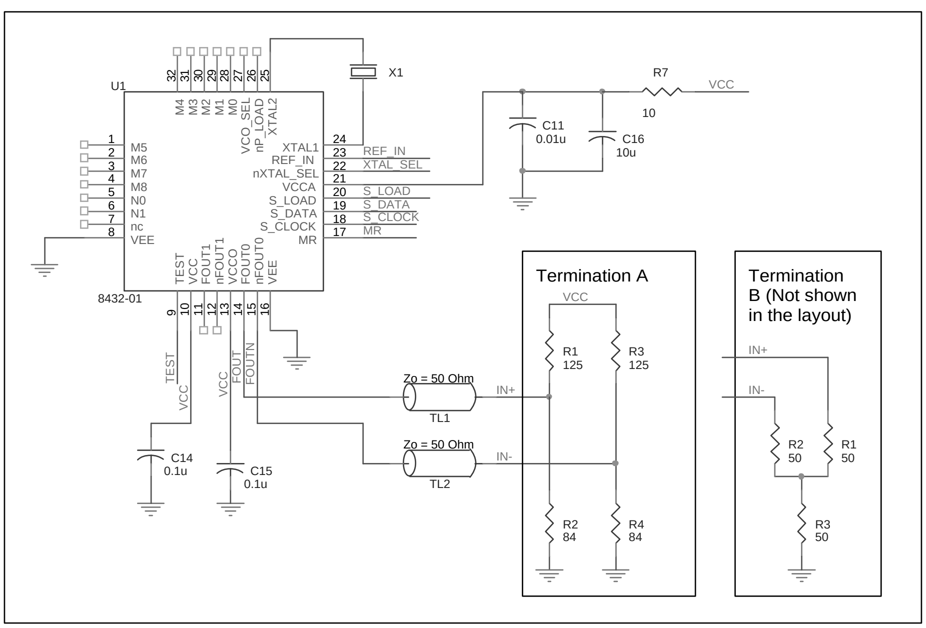


Figure 9A. Recommended Schematic Layout

The following component footprints are used in this layout example: All the resistors and capacitors are size 0603.

Power and Grounding

Place the decoupling capacitors C14 and C15 as close as possible to the power pins. If space allows, placing the decoupling capacitor at the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin generated by the via.

Maximize the pad size of the power (ground) at the decoupling capacitor. Maximize the number of vias between power (ground) and the pads. This can reduce the inductance between the power (ground) plane and the component power (ground) pins.

If V_{CCA} shares the same power supply with V_{CC}, insert the RC filter R7, C11, and C16 in between. Place this RC filter as close to the V_{CCA} as possible.

Clock Traces and Termination

The component placements, locations and orientations should be arranged to achieve the best clock signal quality. Poor clock signal quality can degrade the system performance or cause system failure. In the synchronous high-speed digital system, the clock signal is less tolerable to poor signal quality than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The trace shape and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signals traces.

- The traces with 50Ω transmission lines TL1 and TL2 at FOUT and nFOUT should have equal delay and run adjacent to each other. Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock trace on same layer. Whenever possible, avoid any vias on the clock traces. Any via on the trace can affect the trace characteristic impedance and hence degrade signal quality.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow more space between the clock trace and the other signal trace.
- Make sure no other signal trace is routed between the clock trace pair.

The matching termination resistors R1, R2, R3 and R4 should be located as close to the receiver input pins as possible. Other termination scheme can also be used but is not shown in this example.

Crystal

The crystal X1 should be located as close as possible to the pins 24 (XTAL1) and 25 (XTAL2). The trace length between the X1 and U1 should be kept to a minimum to avoid unwanted parasitic inductance and capacitance. Other signal traces should not be routed near the crystal traces.

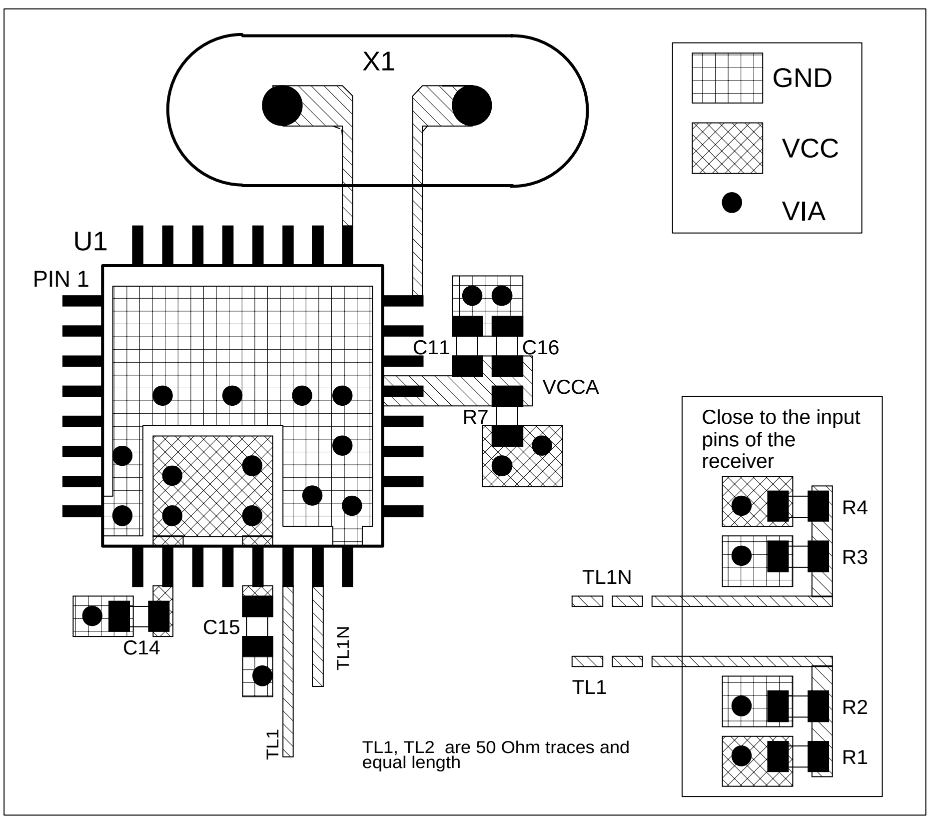


Figure 9B. PCB Board Layout for ICS8432-51

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8432-51.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8432-51 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 110mA = **381.2mW**
- Power (outputs)$_{MAX}$ = **30.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30.2mW = **60.4mW**

Total Power $_{\_MAX}$ (3.465V, with all outputs switching) = 381.2mW + 60.4mW = **441.6mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = junction-to-ambient thermal resistance

Pd_total = Total device power dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 11 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.441W * 42.1°C/W = 88.6°C. This is well below the limit of 125°C

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 11. Thermal Resistance θ_{JA} for 32-pin LQFP, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 10.*

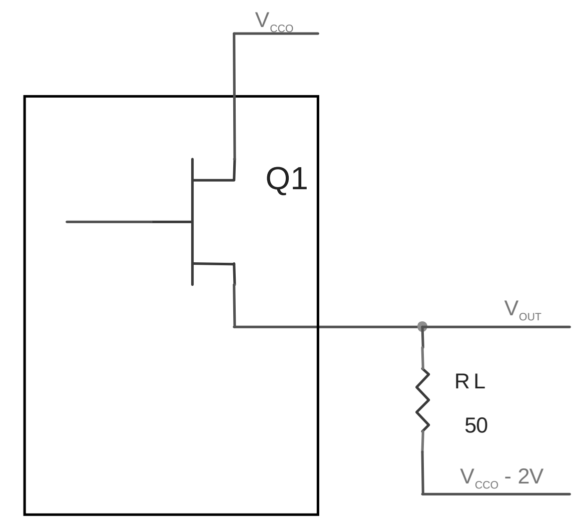


Figure 10 - LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX})$$

$$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX})$$

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} – 1.0V}$

  Using V_{CCO_MAX} = 3.465, this results in V_{OH_MAX} = **2.465V**

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} – 1.7V}$

  Using V_{CCO_MAX} = 3.465, this results in V_{OL_MAX} = **1.765V**

Pd_H =[(2.465V - (3.465V - 2V))/50Ω] * (3.465V - 2.465V) = **20mW**
Pd_L =[(1.765V - (3.465V - 2V))/50Ω] * (3.465V - 1.765V) = **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.2mW**

Reliability Information

Table 12. θ_{JA} vs. Air Flow Table

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for ICS8432-51 is: 3703

Package Outline - Y Suffix

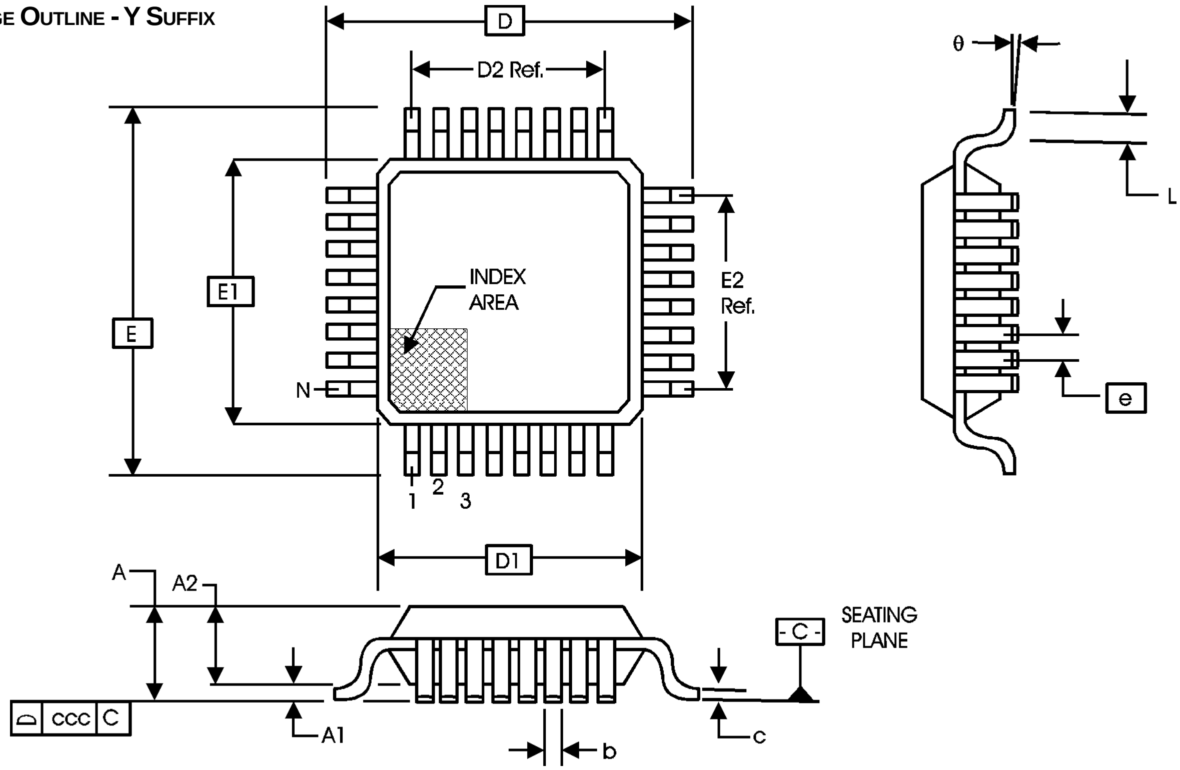


Table 13. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.60 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.60 Ref.		
e	0.80 BASIC		
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

Table 14. Ordering Information

Part/Order Number	Marking	Package	Count	Temperature
ICS8432AY-51	ICS8432AY-51	32 Lead LQFP	250 per tray	0°C to 70°C
ICS8432AY-51T	ICS8432AY-51	32 Lead LQFP on Tape and Reel	1000	0°C to 70°C