Integrated Circuit Systems, Inc.

ICS87974-01

LOW SKEW, 1-TO-15, DIFFERENTIAL-TO-LVCMOS CLOCK GENERATOR

GENERAL DESCRIPTION

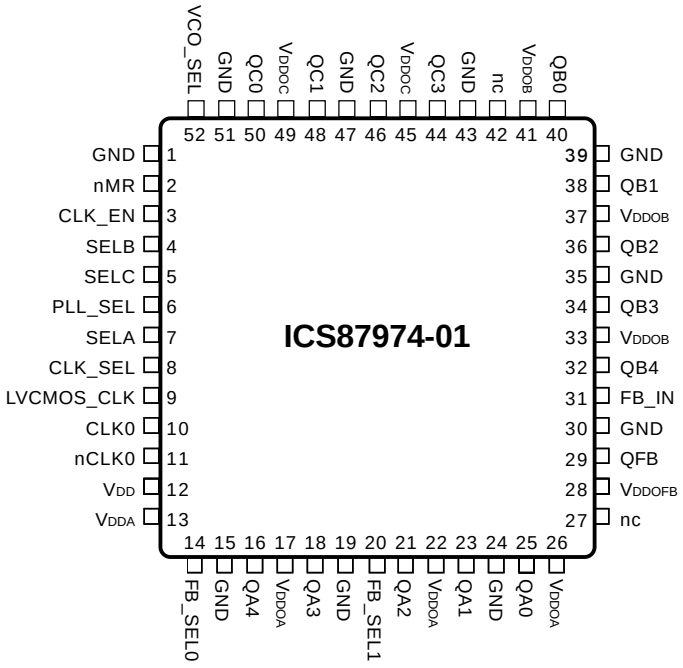
The ICS87974-01 is a low skew, low jitter 1-to-15 Differential-to-LVCMOS clock generator/zero delay buffer and is a member of the HiPerClockS family of High Performance Clock Solutions from ICS. The device has a fully integrated PLL and three banks whose divider ratios can be independently controlled, providing output frequency relationships of 1:1, 2:1, 3:1, 3:2, 3:2:1. In addition, the external feedback connection provides for a wide selection of output-to-input frequency ratios. The LVCMOS_CLK and CLK0, nCLK0 pins allow for redundant clocking on the input and dynamically switching the PLL between two clock sources.

Guaranteed low jitter and output skew characteristics make the ICS87974-01 ideal for those applications demanding well defined performance and repeatability.

FEATURES

- Fully integrated PLL
- 15 single ended 3.3V LVCMOS outputs
- Selectable LVCMOS_CLK or differential CLK0, nCLK0 inputs for redundant clock applications
- LVCMOS_CLK accepts LVCMOS or LVTTL input levels
- CLK0, nCLK0 pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency up to 125MHz
- External feedback for "zero delay" clock regeneration
- Cycle-to-cycle jitter: ±100ps (typical)
- Output skew: 350ps (maximum)
- Bank skew: ±50ps (typical)
- PLL reference zero delay: TBD
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

PIN ASSIGNMENT



52-Lead LQFP
10mm x 10mm x 1.4mm package body
Y package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

BLOCK DIAGRAM

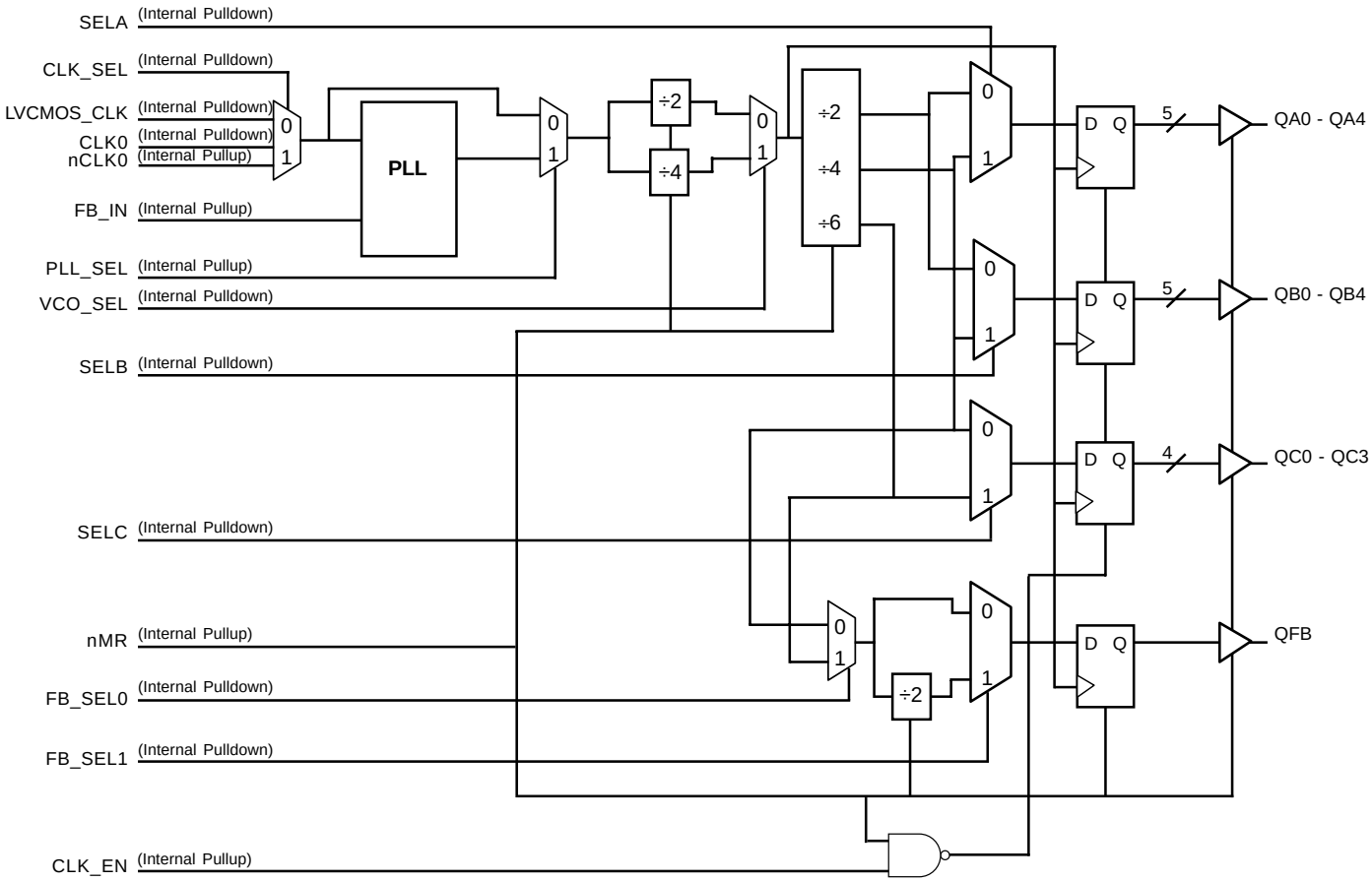


TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 15, 19, 24, 30, 35, 39, 43, 47, 51	GND	Power		Power supply ground. Connect to ground.
2	nMR	Input	Pullup	Master reset. When HIGH, outputs are enabled. When LOW, outputs are disabled and dividers are reset. LVCMOS / LVTTL interface levels.
3	CLK_EN	Input	Pullup	Clock enable. When LOW, all outputs except QFB are low.
4	SELB	Input	Pulldown	Selects divide value for Bank B output as described in Table 3. LVCMOS / LVTTL interface levels.
5	SELC	Input	Pulldown	Selects divide value for Bank C output as described in Table 3. LVCMOS / LVTTL interface levels.
6	PLL_SEL	Input	Pullup	Selects between the PLL and the reference clock as the input to the dividers. When HIGH, selects PLL. When LOW, selects the reference clock. LVCMOS / LVTTL interface levels.
7	SELA	Input	Pulldown	Selects divide value for Bank A output as described in Table 3. LVCMOS / LVTTL interface levels.
8	CLK_SEL	Input	Pulldown	Clock select input. LVCMOS / LVTTL interface levels.
9	LVCMOS_CLK	Input	Pulldown	Clock input. LVCMOS / LVTTL interface levels.
10	CLK0	Input	Pulldown	Non-inverting differential clock input.
11	nCLK0	Input	Pullup	Inverting differential clock input
27, 42	nc	Unused		No connect.
12	V_{DD}	Power		Positive supply pin. Connect to 3.3V.
13	V_{DDA}	Power		Analog supply pin. Connect to 3.3V.
14, 20	FB_SEL0, FB_SEL1	Input	Pulldown	Selects divide value for Bank feedback output as described in Table 3. LVCMOS / LVTTL interface levels.
16, 18, 21, 23, 25	QA4, QA3, QA2, QA1, QA0	Output		Bank A clock outputs. 7Ω typical output impedance. LVCMOS / LVTTL interface levels.
17, 22, 26	V_{DDOA}	Power		Output supply pins. Connect to 3.3V.
28	V_{DDOFB}	Power		Output supply pins. Connect to 3.3V.
29	QFB	Output		Clock output. LVCMOS / LVTTL interface levels.
31	FB_IN	Input	Pullup	Feedback input to phase detector for generating clocks with "zero delay". Connect to pin 29. LVCMOS / LVTTL interface levels.
32, 34, 36, 38, 40	QB4, QB3, QB2, QB1, QB0	Output		Bank B clock outputs. 7Ω typical output impedance. LVCMOS interface levels.
33, 37, 41	V_{DDOB}	Power		Output supply pins. Connect to 3.3V.
44, 46, 48, 50	QC3, QC2, QC1, QC0	Output		Bank C clock outputs. 7Ω typical output impedance. LVCMOS interface levels.
45, 49	V_{DDOC}	Power		Output supply pins. Connect to 3.3V.
52	VCO_SEL	Input	Pulldown	Selects VCO ÷ 4 when HIGH. Selects VCO ÷ 2 when LOW. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDA}, *V_{DDOx} = 3.465V			15	pF

*NOTE: V_{DDOx} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOFB}.

TABLE 3A. OUTPUT CONTROL PIN FUNCTION TABLE

Inputs		Outputs			
nMR	CLK_EN	QA0 - QA4	QB0 - QB4	QC0 - QC3	QFB
0	X	HiZ	HiZ	HiZ	HiZ
1	0	LOW	LOW	LOW	Enable
1	1	Enable	Enable	Enable	Enable

TABLE 3B. OPERATING MODE FUNCTION TABLE

Inputs	Operating Mode
PLL_SEL	
0	Bypass
1	PLL

TABLE 3C. PLL INPUT FUNCTION TABLE

Inputs	
CLK_SEL	PLL Input
0	LVCMOS_CLK
1	CLK0, nCLK0

TABLE 3D. SELECT PIN FUNCTION TABLE

SELA	QAx	SELB	QBx	SELC	QCx
0	÷ 2	0	÷ 2	0	÷ 4
1	÷ 4	1	÷ 4	1	÷ 6

TABLE 3E. FB SELECT FUNCTION TABLE

Inputs		Outputs
FB_SEL0	FB_SEL1	QFB
0	0	÷ 4
0	1	÷ 6
1	0	÷ 8
1	1	÷ 12

TABLE 3F. VCO SELECT FUNCTION TABLE

Inputs	
VCO_SEL	fVCO
0	VCO/2
1	VCO/4

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DDx}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	73.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDOx} = 3.3V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
*V_{DDOx}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			90		mA
I_{DDO}	Output Supply Current			10		mA
I_{DDA}	Analog Supply Current			290		mA

*NOTE: V_{DDOx} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOFB}.

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDOx} = 3.3V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	FB_SEL0, FB_SEL1, SELA, SELB, SELC, CLK_SEL, VCO_SEL LVCMOS_CLK	$V_{DD} = V_{IN} = 3.465V$			150	µA
		FB_IN, nMR, PLL_SEL, CLK_EN	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	FB_SEL0, FB_SEL1, SELA, SELB, SELC, CLK_SEL, VCO_SEL LVCMOS_CLK	V_{IN} = 0V, V_{DD} = 3.465V	-5			µA
		FB_IN, nMR, PLL_SEL, CLK_EN	V_{IN} = 0V, V_{DD} = 3.465V	-150			µA
V_{OH}	Output High Voltage; NOTE 1			2.4			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V
I_{OZL}	Output Tristate Current Low					TBD	µA
I_{OZH}	Output Tristate Current High					TBD	µA

NOTE 1: Outputs terminated with 50Ω to V_{DDOx}/2.

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDOx} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0	$V_{DD} = V_{IN} = 3.465V$			150	µA
		nCLK0	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	CLK0	$V_{IN} = 0V$, $V_{DD} = 3.465V$	-5			µA
		nCLK0	$V_{IN} = 0V$, $V_{DD} = 3.465V$	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} -0.85	V

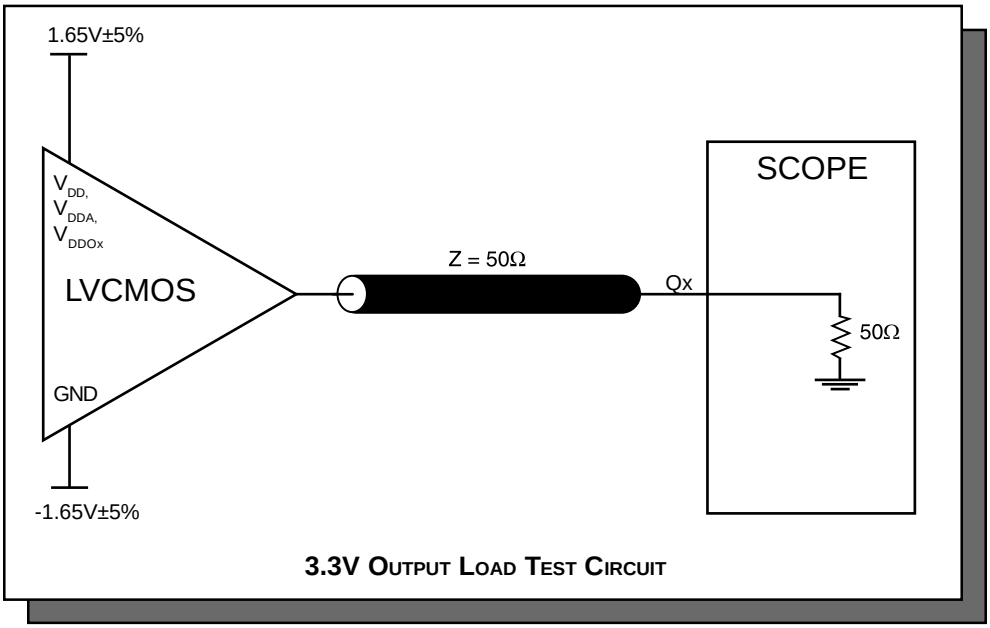
NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK0, nCLK0 is V_{DD} + 0.3V.

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDOx} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

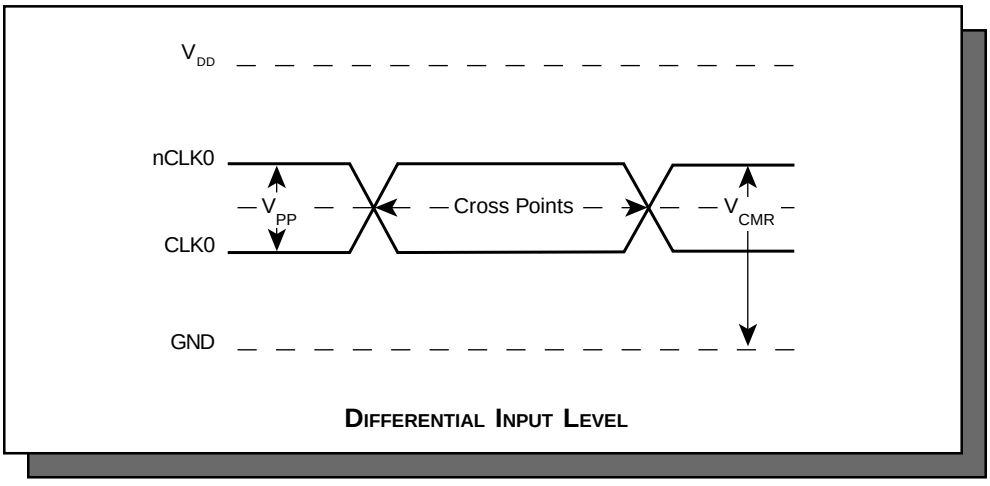
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		Qx ÷ 2, VCO ÷ 2			125	MHz
			Qx ÷ 4, VCO ÷ 2			63	MHz
			Qx ÷ 6, VCO ÷ 2			42	MHz
f_{VCO}	PLL VCO Lock Range; NOTE 5			200		700	MHz
tP_{LH}	Propagation Delay, Low to High; NOTE 1		PLL_SEL = 0V, 0MHz ≤ f ≤ MHz				ns
tP_{HL}	Propagation Delay, High to Low; NOTE 1		PLL_SEL = 0V, 0MHz ≤ f ≤ MHz				ns
t(Ø)	PLL Reference Zero Delay; NOTE 2, 5		PLL_SEL = 3.3V, fREF = TBD, f_{VCO} = TBD	X - 150ps	TBD X	X + 150ps	ps
tsk(b)	Bank Skew; NOTE 3, 5	Bank A	Measured on rising edge at $V_{DDO}/2$		±50		ps
		Bank B			±50		ps
		Bank C			±50		ps
*t*sk(o)	Output Skew; NOTE 4, 5		Measured on rising edge at $V_{DDO}/2$			350	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 5				±100		ps
t_L	PLL Lock Time					10	mS
t_R	Output Rise Time		20% to 80% @ 50MHz		450		ps
t_F	Output Fall Time		20% to 80% @ 50MHz		400		ps
t_{PW}	Output Pulse Width						ps
t_{EN}	Output Enable Time					10	ns
t_{DIS}	Output Disable Time					10	ns

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the $V_{DD}/2$ point of the input to the$V_{DDOx}/2$ of the output.
NOTE 2: Defined as the time difference between the input reference clock and the averaged feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 3: Defined as skew within a bank with equal load conditions.
NOTE 4: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOx}/2$.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

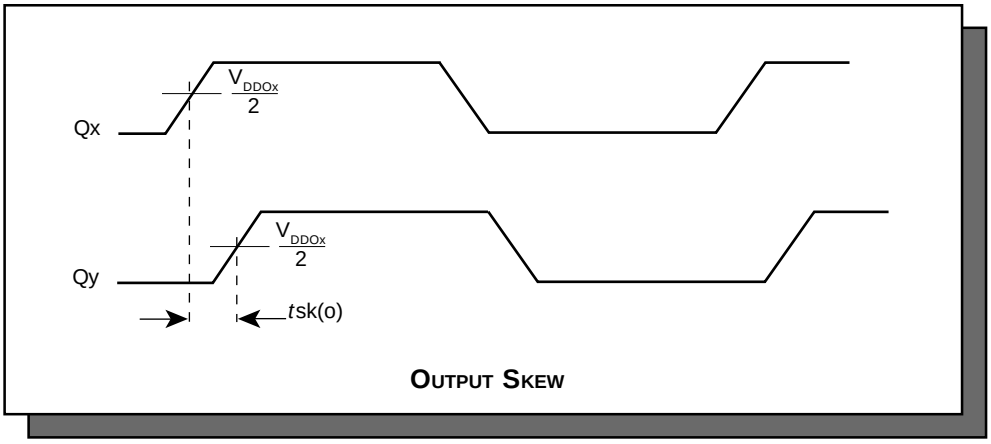
PARAMETER MEASUREMENT INFORMATION



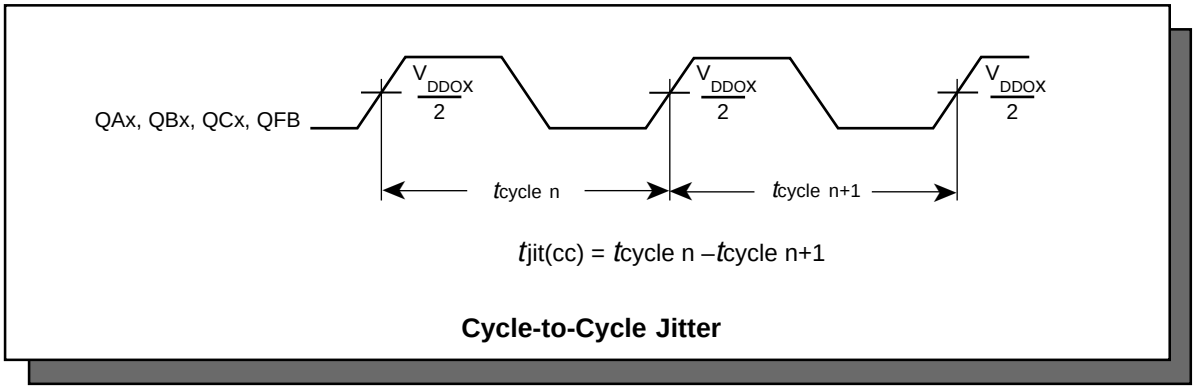
3.3V OUTPUT LOAD TEST CIRCUIT



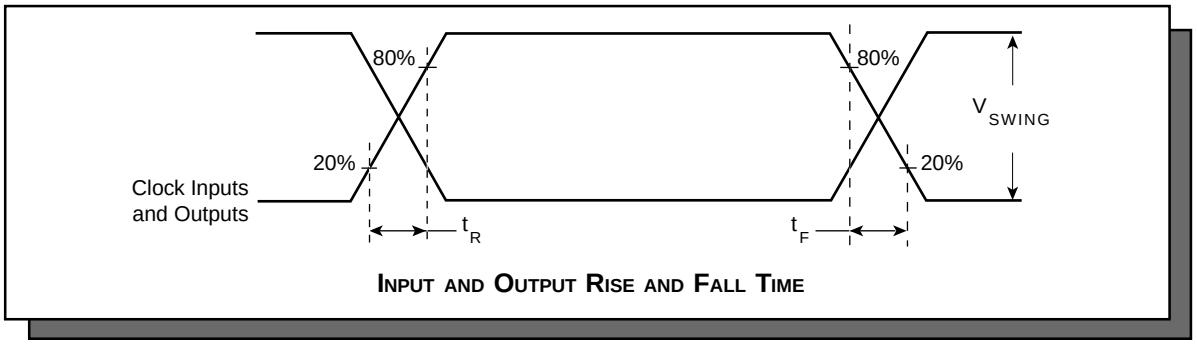
DIFFERENTIAL INPUT LEVEL



OUTPUT SKEW



Cycle-to-Cycle Jitter



INPUT AND OUTPUT RISE AND FALL TIME

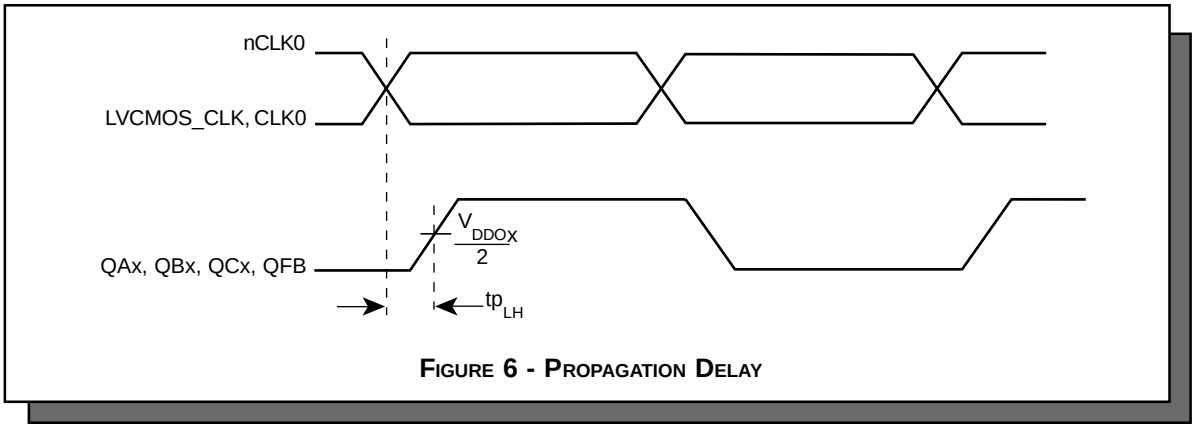


FIGURE 6 - PROPAGATION DELAY

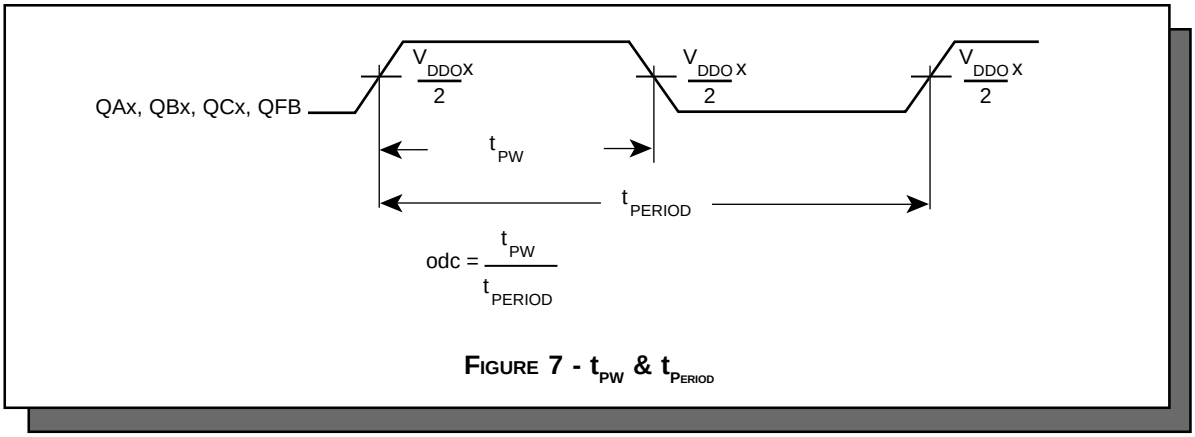


FIGURE 7 - t_{PW} & t_{PERIOD}

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

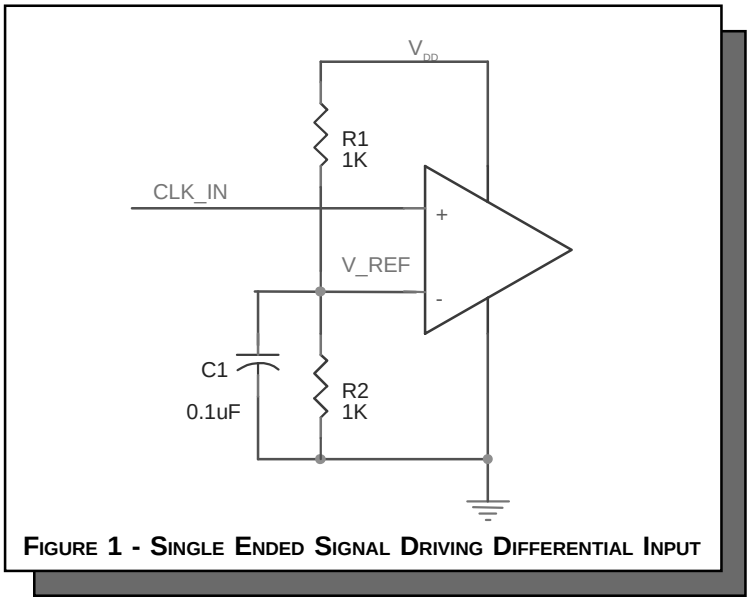


FIGURE 1 - SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS87974-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDOx} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.

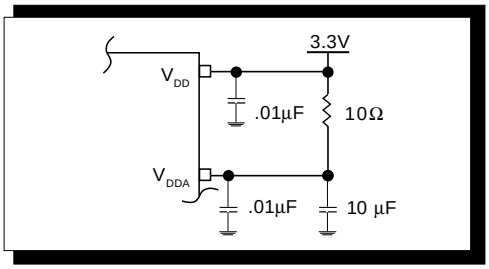


FIGURE 2 - POWER SUPPLY FILTERING

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	58.0°C/W	47.1°C/W	42.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	42.3°C/W	36.4°C/W	34.0°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87974-01 is: 4225

PACKAGE OUTLINE - Y SUFFIX

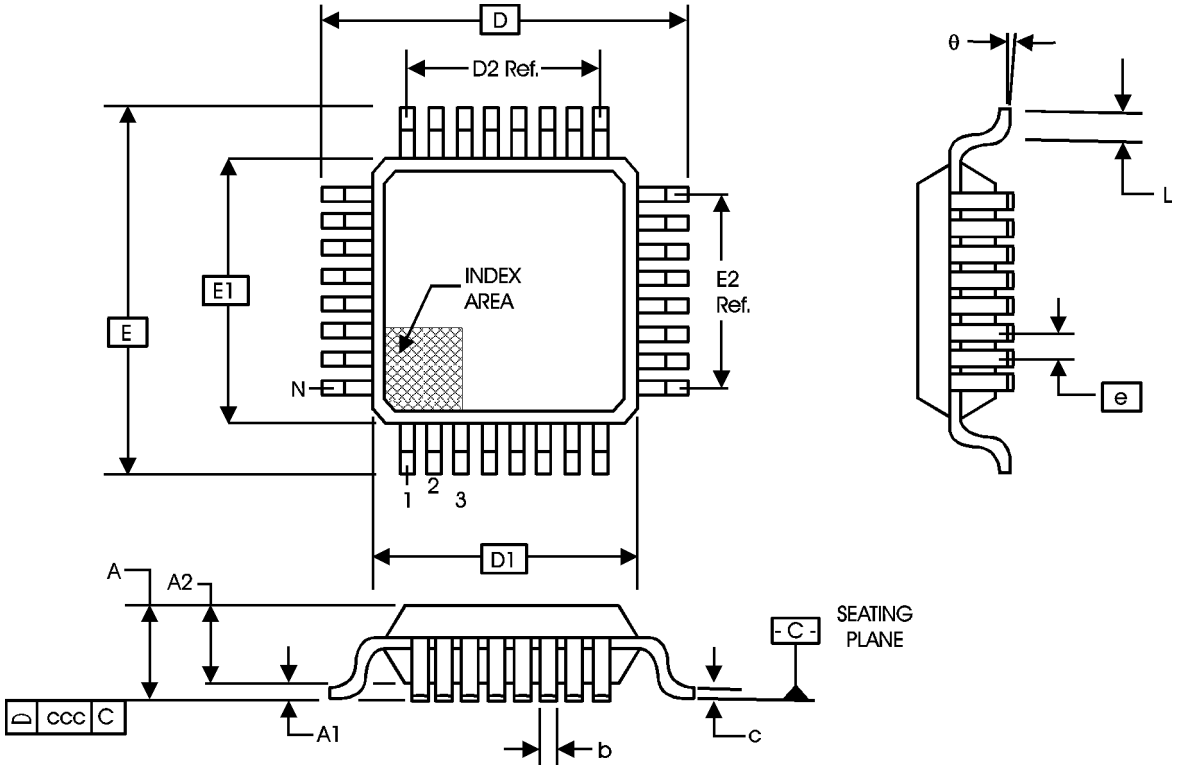


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BCC		
	MINIMUM	NOMINAL	MAXIMUM
N		52	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.22	0.32	0.38
b1	0.22	0.30	0.33
D		12.00 BASIC	
D1		10.00 BASIC	
E		12.00 BASIC	
E1		10.00 BASIC	
e		0.65 BASIC	
ccc	0.45	--	0.10
ddd	--	--	0.13

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS87974AY-01	ICS87974AY-01	52 Lead LQFP	160 per tray	0°C to 70°C
ICS87974AY-01T	ICS87974AY-01	52 Lead LQFP on Tape and Reel	500	0°C to 70°C