Integrated Circuit Systems, Inc.

ICS93v850

Preliminary Product Preview

DDR Phase Lock Loop Clock Driver

Recommended Application:

DDR Clock Driver

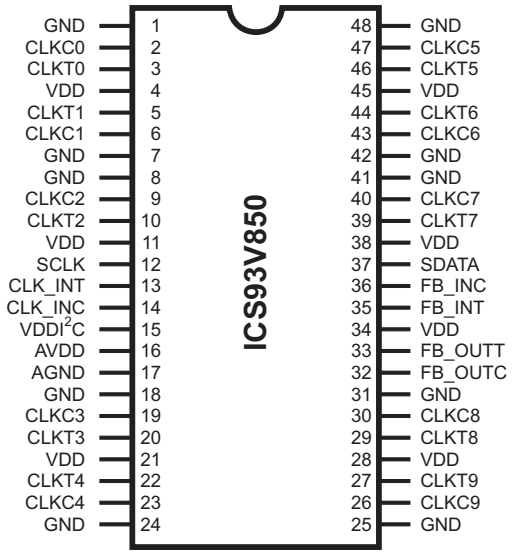
Product Description/Features:

- Low skew, low jitter PLL clock driver
- I^2C for functional and output control
- Feedback pins for input to output synchronization
- Spread Spectrum tolerant inputs
- With bypass mode mux
- Operating frequency 60 to 140 MHz

Switching Characteristics:

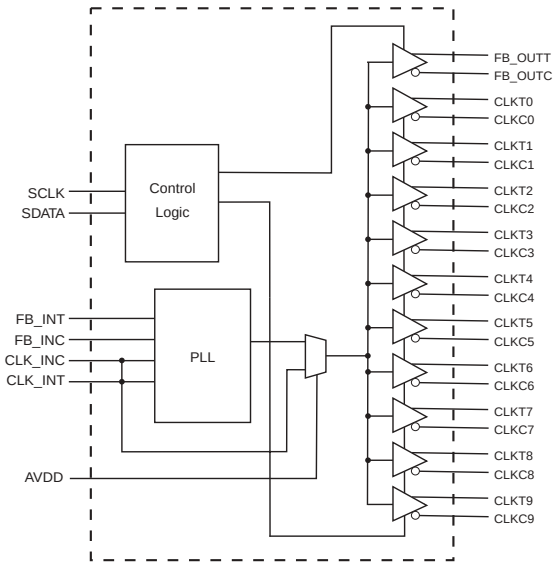
- PEAK - PEAK jitter (66MHz): <120ps
- PEAK - PEAK jitter (>100MHz): <75ps
- CYCLE - CYCLE jitter (66MHz):<120ps
- CYCLE - CYCLE jitter (>100MHz):<65ps
- OUTPUT - OUTPUT skew: <100ps
- Output Rise and Fall Time: 650ps - 950ps
- DUTY CYCLE: 49.5% - 50.5%

Pin Configuration



48-Pin TSSOP

Block Diagram



Functionality

INPUTS			OUTPUTS				PLL State
AVDD	CLK_INT	CLK_INC	CLKT	CLKC	FB_OUTT	FB_OUTC	
GND	L	H	L	H	L	H	Bypassed/Off
GND	H	L	H	L	H	L	Bypassed/Off
2.5V (nom)	L	H	L	H	L	H	On
2.5V (nom)	H	L	H	L	H	L	On
2.5V (nom)	<20 MHz	<20 MHz	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Off

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 7, 8, 18, 24, 25, 31, 41, 42, 48	GND	PWR	Ground
26, 30, 40, 43, 47, 23, 19, 9, 6, 2	CLKC(9:0)	OUT	"Complementory" clocks of differential pair outputs.
27, 29, 39, 44, 46, 22, 20, 10, 5, 3	CLKT(9:0)	OUT	"True" Clock of differential pair outputs.
4, 11, 21, 28, 34, 38, 45,	VDD	PWR	Power supply 2.5V
12	SCLK	IN	Clock input of I^2C input, 5V tolerant input
13	CLK_INT	IN	"True" reference clock input
14	CLK_INC	IN	"Complementory" reference clock input
15	VDDI^2C	PWR	3.3V power for I^2C
16	AVDD	PWR	Analog power supply, 2.5V
17	AGND	PWR	Analog ground.
32	FB_OUTC	OUT	"Complementory" Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INC.
33	FB_OUTT	OUT	"True" " Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INT.
35	FB_INT	IN	"True" Feedback input, provides feedback signal to the internal PLL for synchronization with CLK_INT to eliminate phase error.
36	FB_INC	IN	"Complementory" Feedback input, provides signal to the internal PLL for synchronization with CLK_INC to eliminate phase error.
37	SDATA	IN	Data input for I^2C serial input, 5V tolerant input

Byte 0: Output Control
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	3, 2	1	CLKT0, CLKC0
Bit 6	5, 6	1	CLKT1, CLKC1
Bit 5	10, 9	1	CLKT2, CLKC2
Bit 4	20, 19	1	CLKT3, CLKC3
Bit 3	22, 23	1	CLKT4, CLKC4
Bit 2	46, 47	1	CLKT5, CLKC5
Bit 1	44, 43	1	CLKT6, CLKC6
Bit 0	39, 40	1	CLKT7, CLKC7

Byte 1: Output Control
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	29, 30	1	CLKT8, CLKC8
Bit 6	27, 26	1	CLKT9, CLKC9
Bit 5	-	0	Reserved
Bit 4	-	0	Reserved*
Bit 3	-	0	Reserved*
Bit 2	-	0	Reserved
Bit 1	-	0	Reserved
Bit 0	-	0	Reserved

*** Note: Do not change this bit value.**

Byte 2: Reserved
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Byte 3: Reserved
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Byte 4: Reserved
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Byte 5: Reserved
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Reserved (Note)
Bit6	-	0	Reserved (Note)
Bit5	-	0	Reserved (Note)
Bit4	-	0	Reserved (Note)
Bit3	-	0	Reserved (Note)
Bit2	-	1	Reserved (Note)
Bit1	-	1	Reserved (Note)
Bit0	-	0	Reserved (Note)

Note: Don't write into this register, writing into this register can cause malfunction

Absolute Maximum Ratings

Supply Voltage: (VDD & AVDD) . . . . . -0.5V to 3.6V

(VDDI) . . . . . -0.5V to 4.6V

Logic Inputs: VI (except SCLK and SDATA) . . . . . –0.5 V to V_{DD} +0.5 V

VI (SCLK and SDATA) . . . . . –0.5 V to V_{DDI2C} +0.5 V

Logic Outputs: VO (except SDATA) . . . . . –0.5 V to V_{DD} +0.5 V

VO (SDATA) . . . . . –0.5 V to V_{DDI2C} +0.5 V

Input clamp current: IIK (VI < 0 or VI > VDD) . . . . . +/- 50mA

Output clamp current: IOK (VO < 0 or VO > VDD) . . . . . +/- 50mA

Continuous output current: IO (VO = 0 to VDD) . . . . . +/- 50mA

Package thermal impedance, theta JA: DGG package . . . +89°C/W

Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 85C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I_{IH}	VI = VDD or GND				µA
Input Low Current	I_{IL}	VI = VDD or GND				µA
Operating Supply Current	$I_{DD2.5}$	CL = 0pf				mA
	I_{DDPD}	CL = 0pf			100	µA
Output High Current	I_{OH}	VDD = 2.3V, V_{OUT} = 1V	-18			mA
Output Low Current	I_{OL}	VDD = 2.3V, V_{OUT} = 1.2V	26			mA
High Impedance Output Current	I_{OZ}	VDD=2.7V, Vout=VDD or GND			±10	µA
Input Clamp Voltage	V_{IK}	Iin = -18mA				V
High-level output voltage	V_{OH}	VDD = min to max, IOH = -1 mA				V
		VDD = 2.3V, IOH = -12 mA				V
Low-level output voltage	V_{OL}	VDD = min to max I_{OL}=1 mA			0.1	
		VDD = 2.3V IOH=12 mA			0.6	V
Input Capacitance[1]	C_{IN}	VI = GND or VDD				pF
Output Capacitance[1]	C_{OUT}	VOUT = GND or VDD		3		pF

[1]Guaranteed by design, not 100% tested in production.

Recommended Operating Condition

T_A = 0 - 85C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog/core supply voltage	V_{DD}, A_{VDD}		2.3	2.5	2.7	V
	V_{DDI2C}		2.3		3.6	V
Input voltage level	V_{IL}		-0.3		V_{DD}-0.4	V
	V_{IH}		0.4		V_{DD}+0.3	V
Input differential-pair voltage swing[1]	V_{ID}	DC - CLK_INT, FB_INT	0.36		V_{DDQ} +0.6	V
		AC - CLK_INT, FB_INT	0.5		V_{DDQ} +0.6	V
Input differential-pair crossing voltage	V_{IC}		0.45x(V_{IH}-V_{IL})		0.55x(V_{IH}-V_{IL})	V
Output differential-pair crossing voltage	V_{OC}					V

[1] Differential inputs signal voltages specifies the differential voltage [VTR - VCP] required for switching, where VT is the true input level and VCP is the complementary input level.

Timing Requirements

T_A = 0 - 85C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Operating clock frequency	$freq_{op}$		66	170	MHz
Input clock duty cycle	d_{tin}		40	60	%
CLK stabilization	T_{STAB}	from VDD = 3.3V to 1% target freq.		100	µs

Switching Characteristics

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Jitter; Absoulte Jitter	T_{jabs}	66MHz			120	ps
		100/125/133/167MHz			75	ps
Cycle to Cycle Jitter[1]	T_{cyc}-T_{cyc}	66MHz			110	ps
		100/125/133/167MHz			65	ps
Phase error	$t_{(phase\ error)}$		-150		150	ps
Output to Output Skew	T_{skew}				100	ps
Pulse skew	T_{skewp}				100	ps
Duty cycle	D_C[2]	66MHz to 100MHz	49.5		50.5	%
		101MHz to 167MHz	49		51	%
Rise Time, Fall Time	t_r, t_f	Load = 120Ω/16pF	650	800	950	ps
Typ: Propagation Delay Time		Bypass Mode CLK to any output		4		ns

Notes:

1. Refers to transition on noninverting output.
2. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle=t_{wH}/t_c, were the cycle (t_c) decreases as the frequency goes up.

General I^2C serial interface information

The information in this section assumes familiarity with I^2C programming.
For more information, contact ICS for an I^2C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

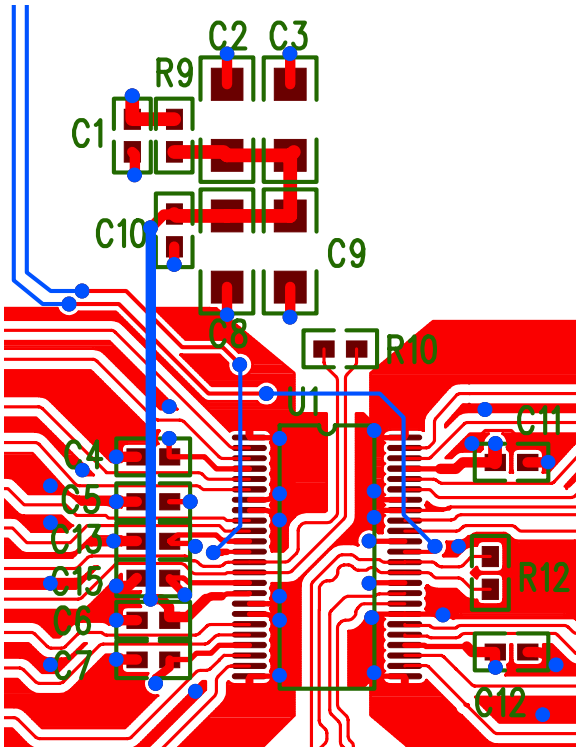
1. The ICS clock generator is a slave/receiver, I^2C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I^2C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

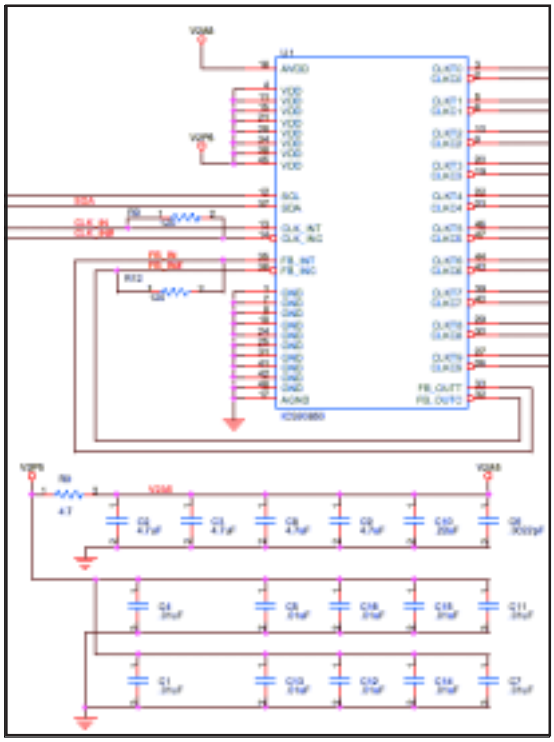
Recommended Layout for the ICS93v850

General Layout Precautions:

Use copper flooded ground on the top signal layer under the clock buffer The area under U1 on the right is an example. Flood over the ground vias.

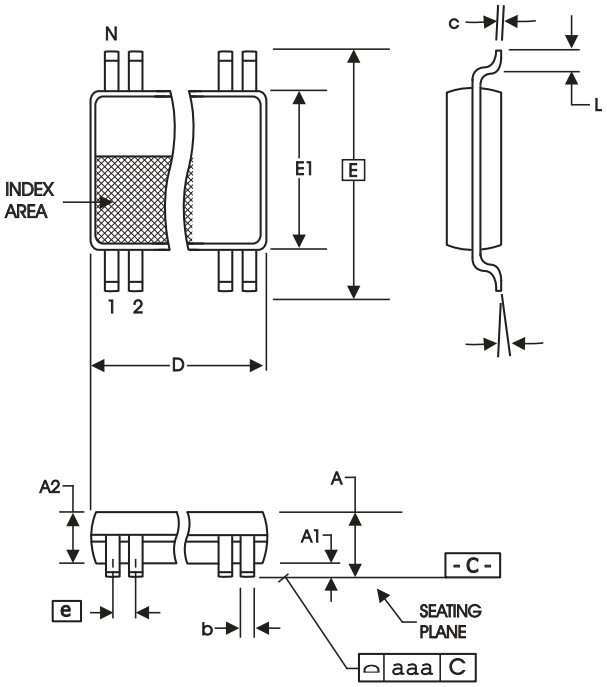
1) Use power vias for power and ground. Vias 20 mil or larger in diameter have lower high frequency impedance. Vias for signals may be minimum drill size.
2) Make all power and ground traces are as wide as the via pad for lower inductance.
3) VAA for pin 16 has a low pass RC filter to decouple the digital and analog supplies. The 4.7uF capacitors may be replaced with a single low ESR device with the same total capacitance. VAA is routed on a outside signal layer. Do not cut a power or ground plane and route in it.
4) Notice that ground vias are never shared.
5) When ever possible, VCC (net V2P5 in the schematic) pins have a decoupling capacitor. Power is always routed from the plane connection via to the capacitor pad to the VCC pin on the clock buffer. Moats or plane cuts are not used to isolate power.
6) Differential mode clock output traces are routed:
   a. With a ground trace between the pairs. Trace is grounded on both ends.
   b. Without a ground trace, clock pairs are routed with a separation of at least 5 times the thickness of the dielectric. If the dielectric thickness is 4.5 mil, the trace separation is at least 18 mils.
7) Terminate differential CLK_IN and FB_IN traces after routing to buffer pads.





Component Values:

Ref Desg.	Value	Description	Package
C1,C4,C5, C7,C11,C12	.01uF	CERAMIC MLC	0603
C2,C3,C8, C9	4.7uF	CERAMIC MLC	1206
C10	.22uF	CERAMIC MLC	0603
C6	2200pF	CERAMIC MLC	0603
R9,R12	120 Ω		0603
R9	4.7 Ω		0603
U1		ICS93701AG	TSSOP48



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

6.10 mm. Body, 0.50 mm. pitch TSSOP
(240 mil) (0.020 mil)

Ordering Information

ICS93v850yGT

Example:

ICS XXXX y G - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  G=TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS, AV = Standard Device