PRELIMINARY

Integrated Circuit Systems, Inc.

ICS87951

LOW SKEW, 1-TO-9 DIFFERENTIAL-TO-LVCMOS ZERO DELAY BUFFER

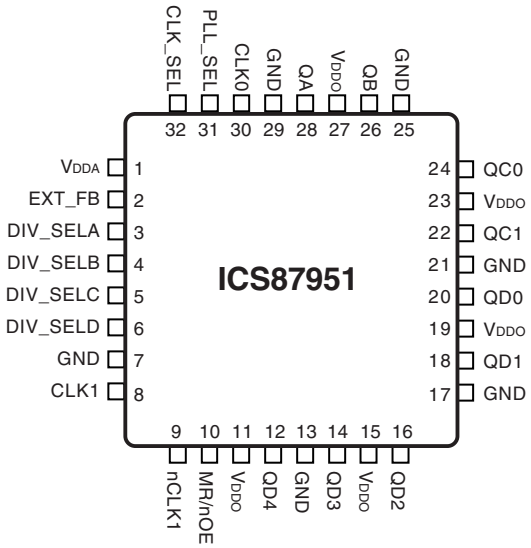
GENERAL DESCRIPTION

The ICS87951 is a low voltage, low skew 1-to-9 Differential-to-LVCMOS clock generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS87951 has two selectable clock inputs. The single ended clock input accepts LVCMOS or LVTTL input levels. The CLK1, nCLK1 pair can accept most standard differential input levels. With output frequencies up to 180MHz, the ICS87951 is targeted for high performance clock applications. Along with a fully integrated PLL, the ICS87951 contains frequency configurable outputs and an external feedback input for regenerating clocks with "zero delay".

FEATURES

- Fully integrated PLL
- 9 single ended 3.3V LVCMOS outputs
- Selectable single ended CLK0 or differential CLK1, nCLK1 inputs
- The single ended CLK0 input can accept the following input levels: LVCMOS or LVTTL input levels
- CLK1, nCLK1 supports the following input types: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency up to 180MHz
- VCO range: 200MHz to 480MHz
- External feedback for "zero delay" clock regeneration
- Cycle-to-cycle jitter: ±100ps (typical)
- Output skew: 375ps (maximum)
- PLL reference zero delay: 350ps window (maximum)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Pin compatible with the MPC951
- Industrial temperature information available upon request

PIN ASSIGNMENT



32-Lead LQFP

7mm x 7mm x 1.4mm package body

Y package

Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

BLOCK DIAGRAM

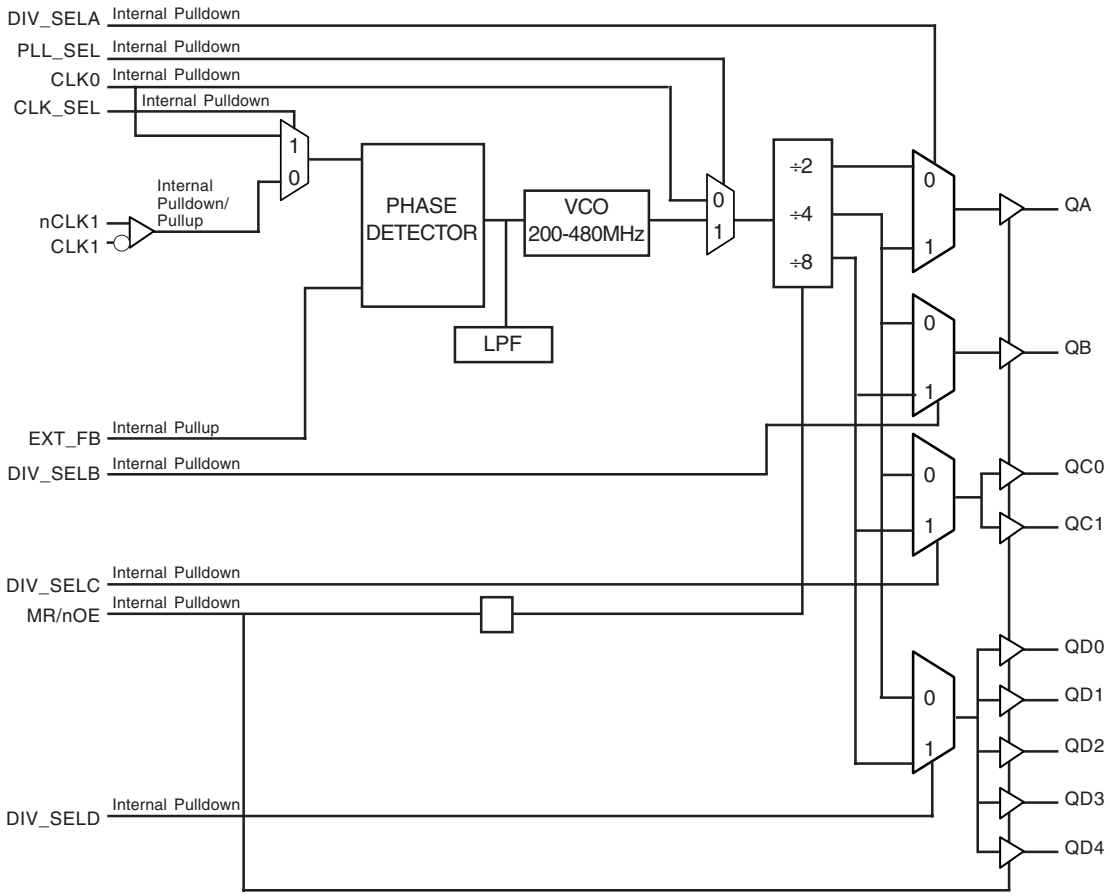


TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{DDA}	Power		Analog supply pin. Connect to 3.3V.
2	EXT_FB	Input	Pullup	Feedback input to phase detector for regenerating clocks with "zero delay". LVCMOS / LVTTL interface levels.
3	DIV_SELA	Input	Pulldown	Selects divide value for Bank A output as described in Table 3D. LVCMOS / LVTTL interface levels.
4	DIV_SELB	Input	Pulldown	Selects divide value for Bank B output as described in Table 3D. LVCMOS / LVTTL interface levels.
5	DIV_SELC	Input	Pulldown	Selects divide value for Bank C outputs as described in Table 3D. LVCMOS / LVTTL interface levels.
6	DIV_SELD	Input	Pulldown	Selects divide value for Bank D outputs as described in Table 3D. LVCMOS / LVTTL interface levels.
7, 13, 17, 21, 25, 29	GND	Power		Power supply ground. Connect to ground.
8	CLK1	Input	Pullup	Non-inverting differential clock input.
9	nCLK1	Input	Pulldown	Inverting differential clock input.
10	MR/nOE	Input	Pulldown	Master reset and output enable. When LOW, outputs are enabled. When HIGH, outputs are disabled and dividers are reset. LVCMOS / LVTTL interface levels.
11, 15, 19, 23, 27	V_{DDO}	Power		Output supply pins. Connect to 3.3V.
12, 14, 16, 18, 20	QD4, QD3, QD2, QD1, QD0	Output		Bank D clock outputs. 7Ω typical output impedance. LVCMOS interface levels.
22, 24	QC1, QC0	Output		Bank C clock outputs. 7Ω typical output impedance. LVCMOS interface levels.
26	QB	Output		Bank B clock output. 7Ω typical output impedance. LVCMOS interface levels.
28	QA	Output		Bank A clock output. 7Ω typical output impedance. LVCMOS interface levels.
30	CLK0	Input	Pulldown	LVCMOS / LVTTL phase detector reference clock input.
31	PLL_SEL	Input	Pulldown	Selects between the PLL and the reference clock as the input to the dividers. When HIGH, selects PLL. When LOW, selects the reference clock.
32	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK0. When LOW, selects CLK1, nCLK1. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DDA}, V_{DDO} = 3.47V		TBD		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

TABLE 3A. OUTPUT CONTROL PIN FUNCTION TABLE

Inputs	Outputs			
MR/nOE	QA	QB	QC0 - QC1	QD0 - QD4
1	HiZ	HiZ	HiZ	HiZ
0	Enabled	Enabled	Enabled	Enabled

TABLE 3B. OPERATING MODE FUNCTION TABLE

Inputs	Operating Mode
PLL_SEL	
0	Bypass
1	PLL

TABLE 3C. PLL INPUT FUNCTION TABLE

Inputs	
CLK_SEL	PLL Input
0	CLK1, nCLK1
1	CLK0

TABLE 3D. PROGRAMMABLE OUTPUT FREQUENCY FUNCTION TABLE

Inputs				Outputs			
DIV_SELA	DIV_SELB	DIV_SELC	DIV_SELD	QA	QB	QCx	QDx
0	0	0	0	VCO/2	VCO/4	VCO/4	VCO/4
0	0	0	1	VCO/2	VCO/4	VCO/4	VCO/8
0	0	1	0	VCO/2	VCO/4	VCO/8	VCO/4
0	0	1	1	VCO/2	VCO/4	VCO/8	VCO/8
0	1	0	0	VCO/2	VCO/8	VCO/4	VCO/4
0	1	0	1	VCO/2	VCO/8	VCO/4	VCO/8
0	1	1	0	VCO/2	VCO/8	VCO/8	VCO/4
0	1	1	1	VCO/2	VCO/8	VCO/8	VCO/8
1	0	0	0	VCO/4	VCO/4	VCO/4	VCO/4
1	0	0	1	VCO/4	VCO/4	VCO/4	VCO/8
1	0	1	0	VCO/4	VCO/4	VCO/8	VCO/4
1	0	1	1	VCO/4	VCO/4	VCO/8	VCO/8
1	1	0	0	VCO/4	VCO/8	VCO/4	VCO/4
1	1	0	1	VCO/4	VCO/8	VCO/4	VCO/8
1	1	1	0	VCO/4	VCO/8	VCO/8	VCO/4
1	1	1	1	VCO/4	VCO/8	VCO/8	VCO/8

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DDx}	4.6V
Inputs, V_I	-0.5V to V_{DDA} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	42.1°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DDA}	Analog Supply Current			10		mA
I_{DDO}	Output Supply Current			200		mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK0		2		V_{DD} + 0.3	V
		MR/nOE, DIV_SELx, PLL_SEL, CLK_SEL		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	CLK0		-0.3		1.3	V
		MR/nOE, DIV_SELx, PLL_SEL, CLK_SEL		-0.3		0.8	V
I_{IH}	Input High Current	MR/nOE, DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD	*V_{DDx} = V_{IN} = 3.465V			120	µA
		CLK0, PLL_SEL, CLK_SEL	*V_{DDx} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	MR/nOE, DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD	V_{IN} = 0V, *V_{DDx} = 3.465V	-5			µA
		CLK0, PLL_SEL, CLK_SEL	V_{IN} = 0V, *V_{DDx} = 3.465V	-120			µA
V_{OH}	Output High Voltage; NOTE 1			2.4			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$.
*NOTE: V_{DDx} denotes V_{DDA} and V_{DDO}.

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, V_{DDA} = V_{DDO} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK1	*V_{DDx} =V_{IN} = 3.465V			150	µA
		CLK1	*V_{DDx} =V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	nCLK1	V_{IN} = 0V, *V_{DDx} = 3.465V	-5			µA
		CLK1	V_{IN} = 0V, *V_{DDx} = 3.465V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK1 and nCLK1 is V_{DDA}+ 0.3V.
*NOTE: V_{DDx} denotes V_{DDA} and V_{DDO}.

TABLE 5. PLL INPUT REFERENCE CHARACTERISTICS, V_{DDA} = V_{DDO} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Reference Frequency				100	MHz

TABLE 6. AC CHARACTERISTICS, V_{DDA} = V_{DDO} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		QA ÷2			180	MHz
			QA/QB ÷4			120	MHz
			QB ÷8			60	MHz
f_{VCO}	PLL VCO Lock Range			200		480	MHz
tp_{LH}	Propagation Delay, Low to High	CLK0; NOTE 1A	PLL_SEL = 0V		4.6		ns
		CLK1, nCLK1; NOTE 1B			4.8		ns
t(Ø)	Static Phase Offset; NOTE 2, 5		PLL_SEL = 3.3V, fREF = TBD, f_{VCO} = TBD	TBD - 175	TBD	TBD + 175	ps
*t*sk(o)	Output Skew; NOTE 4, 5					375	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 5				± 100		ps
t_L	PLL Lock Time; NOTE 5						mS
t_R	Output Rise Time		0.8 to 2V	0.1		1.0	ns
t_F	Output Fall Time		0.8 to 2V	0.1		1.0	ns
t_{PW}	Output Pulse Width			tcycle/2 - 100		tcycle/2 + 100	ps
t_{EN}	Output Enable Time					6	ns
t_{DIS}	Output Disable Time					7	ns

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1A: Measured from theV_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 1B: Measured from the differential input crossing point toV_{DDO}/2 of the output.
NOTE 2: Defined as the time difference between the input reference clock and the averaged feedback input signal, when the PLL is locked and the input reference frequency is stable.
NOTE 3: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
NOTE 4: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

PARAMETER MEASUREMENT INFORMATION

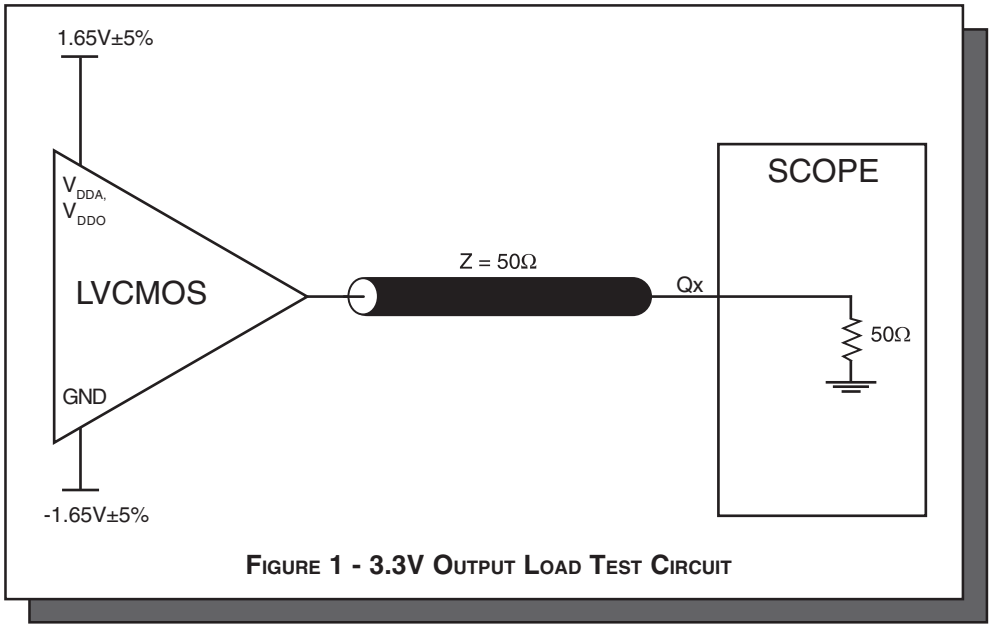


FIGURE 1 - 3.3V OUTPUT LOAD TEST CIRCUIT

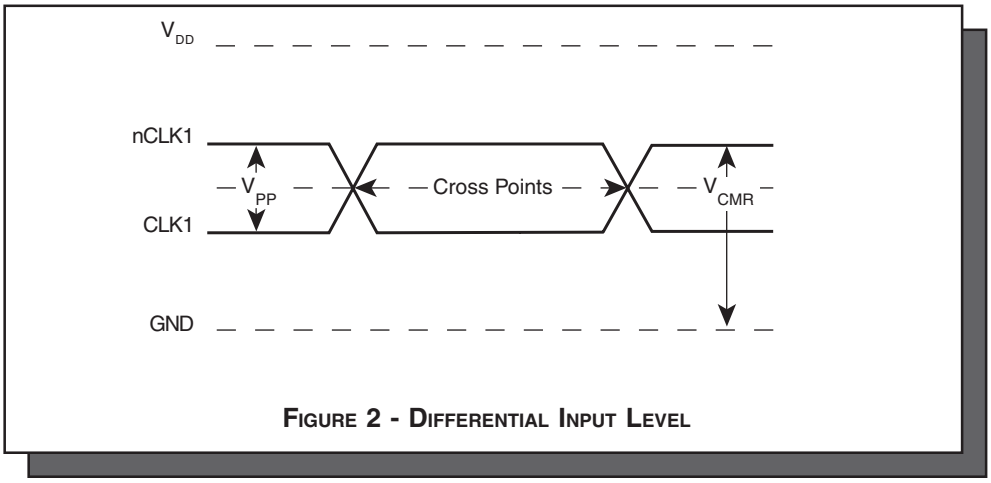
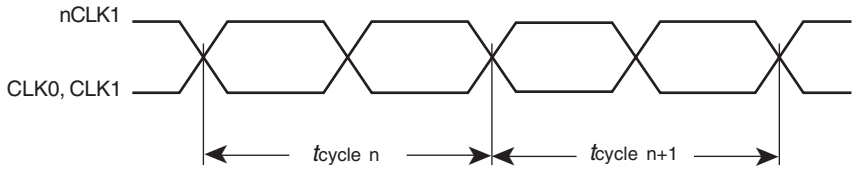
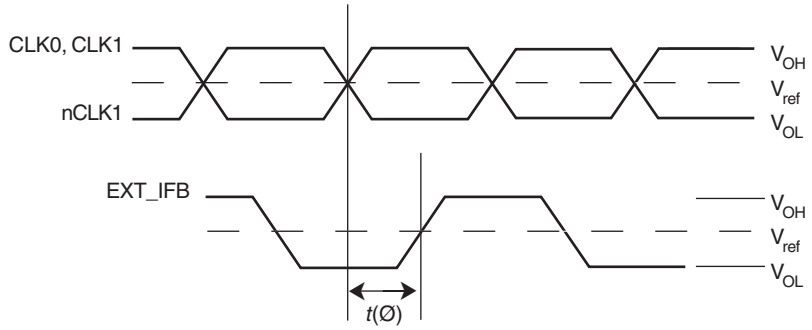


FIGURE 2 - DIFFERENTIAL INPUT LEVEL



$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$
1000 Cycles

FIGURE 3 - Cycle-to-Cycle Jitter



$t_{jit(Ø)} = \left| t(Ø) - t(Ø)_{mean} \right|$ = Phase Jitter $t(Ø)_{mean}$ = Static Phase Offset

(where $t(Ø)$ is any random sample, and $t(Ø)_{mean}$ is the average of the sampled cycles measured on controlled edges)

FIGURE 4 - PHASE JITTER AND STATIC PHASE OFFSET

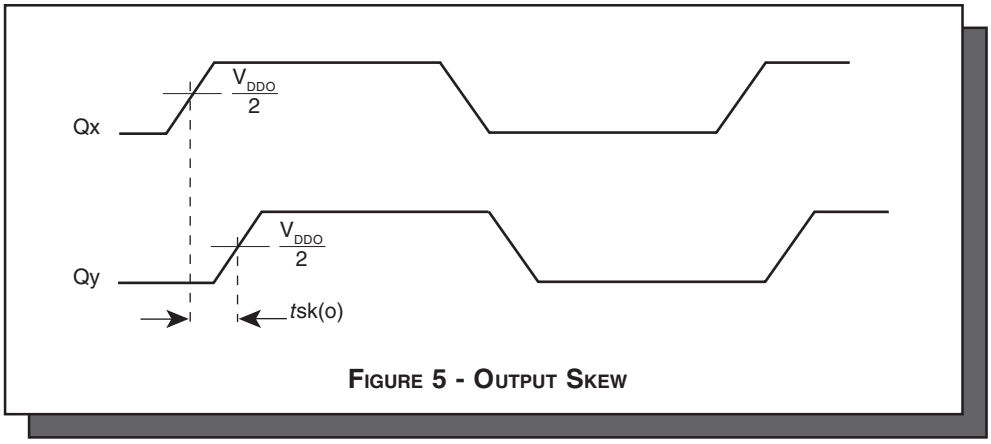


FIGURE 5 - OUTPUT SKEW

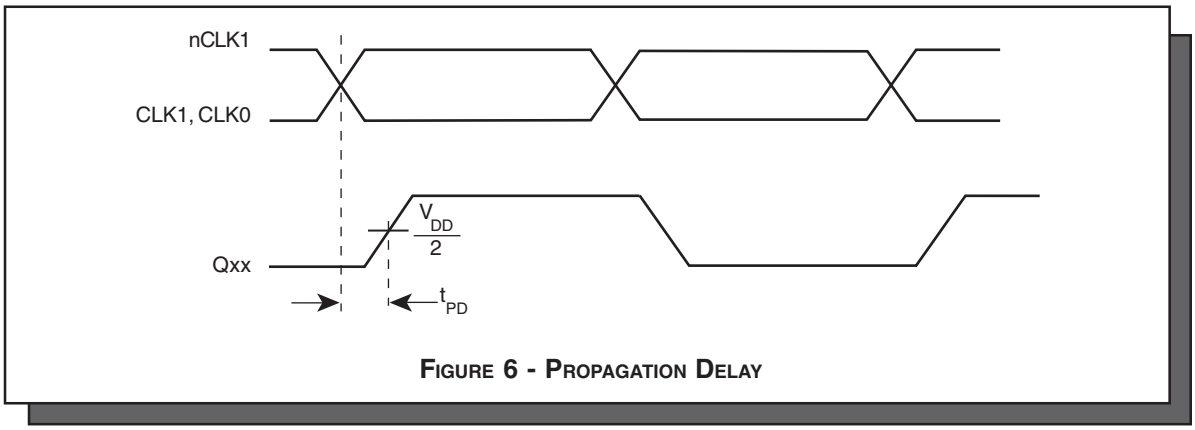


FIGURE 6 - PROPAGATION DELAY

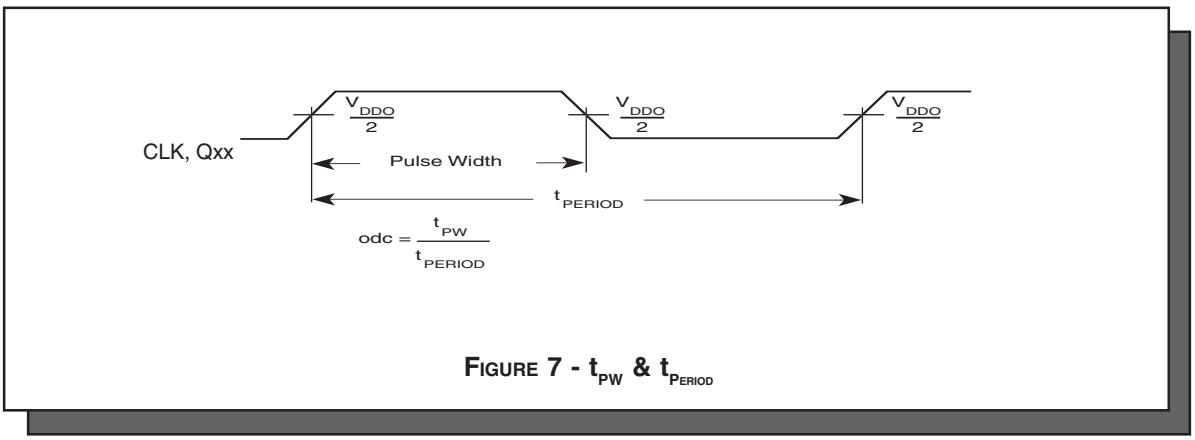


FIGURE 7 - t_{PW} & t_{PERIOD}

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 8 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF ~ V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

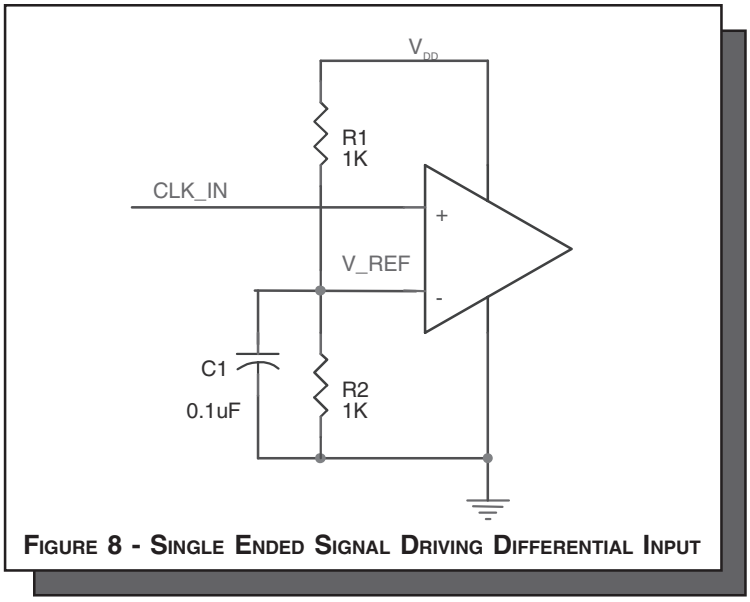


FIGURE 8 - SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

TABLE 7. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87951 is: 2674

PACKAGE OUTLINE - Y SUFFIX

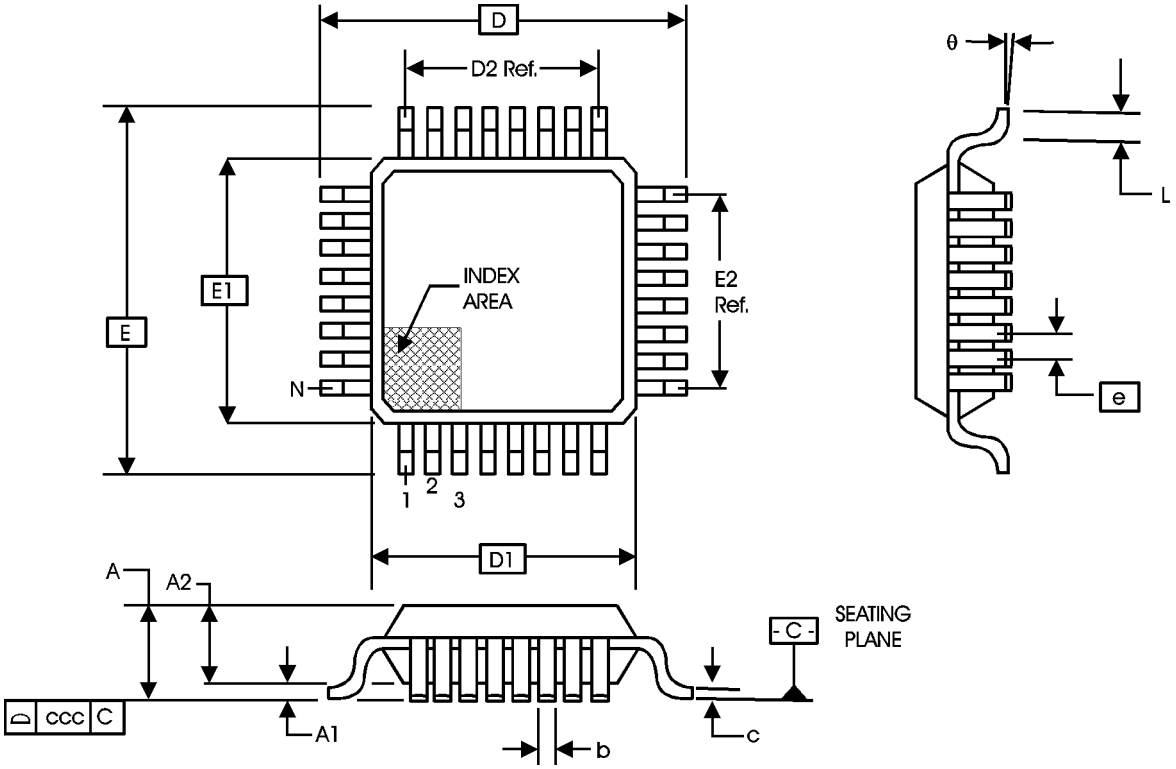


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS87951AY	ICS87951AY	32 Lead LQFP	250 per tray	0°C to 70°C
ICS87951AY-T	ICS87951AY	32 Lead LQFP on Tape and Reel	1000	0°C to 70°C