Integrated Circuit Systems, Inc.

ICS8745-21
DIFFERENTIAL-TO-LVDS ZERO DELAY CLOCK GENERATOR

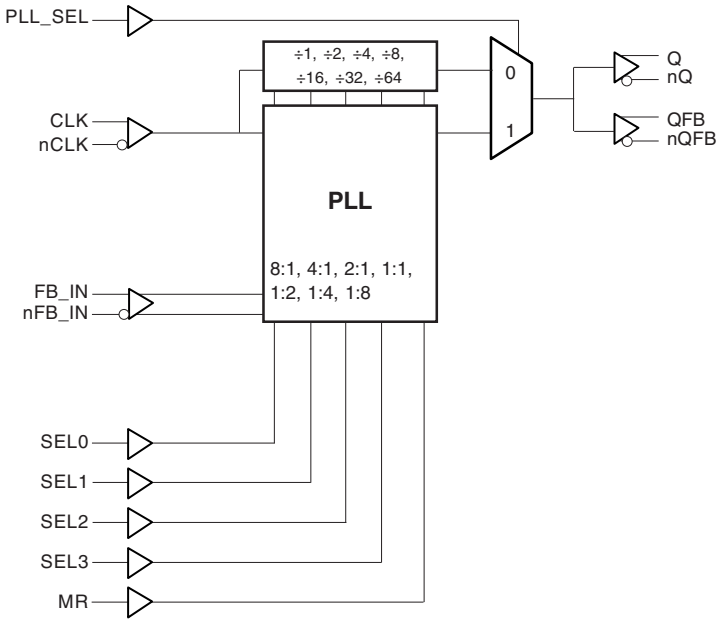
GENERAL DESCRIPTION

The ICS8745-21 is a highly versatile 1:1 LVDS clock generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8745-21 has a fully integrated PLL and can be configured as zero delay buffer, multiplier or divider, and has an output frequency range of 31.25MHz to 700MHz. The Reference Divider, Feedback Divider and Output Divider are each programmable, thereby allowing for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8. The external feedback allows the device to achieve "zero delay" between the input clock and the output clocks. The PLL_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output dividers.

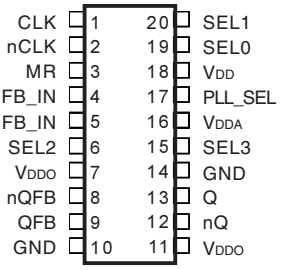
FEATURES

- 1 differential 3.3V LVDS output pair designed to meet or exceed the requirements of ANSI TIA/EIA-644
  1 differential feedback output pair
- Differential CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Output frequency range: 31.25MHz - 700MHz
- Input frequency range: 31.25MHz - 700MHz
- VCO range: 250MHz - 700MHz
- External feedback for "zero delay" clock regeneration with configurable frequencies.
- Programmable dividers allow for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8
- Cycle-to-cycle jitter: 25ps (maximum)
- Static phase offset: 50ps ± 150ps
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS8745-21

20-Lead, 300-MIL SOIC
7.5mm x 12.8mm x 2.3mm body package
M Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	CLK	Input	Pulldown	Non-inverting differential clock input.
2	nCLK	Input	Pullup	Inverting differential clock input.
3	MR	Input	Pulldown	Master reset. Resets the output divider. LVCMOS interface levels.
4	nFB_IN	Input	Pullup	Feedback input to phase detector for regenerating clocks with "zero delay".
5	FB_IN	Input	Pulldown	Feedback input to phase detector for regenerating clocks with "zero delay".
6	SEL2	Input	Pulldown	Determines output divider values in Table 3. LVCMOS interface levels.
7, 11	V_{DDO}	Power		Output supply pins. Connect to 3.3V.
8, 9	nQFB, QFB	Output		Differential feedback outputs. LVDS interface levels.
10, 14	GND	Power		Power supply ground. Connect to ground.
12, 13	nQ, Q	Output		Differential clock outputs. LVDS interface levels.
15	SEL3	Input	Pulldown	Determines output divider values in Table 3. LVCMOS interface levels.
16	V_{DDA}	Power		Analog supply pin. Connect to 3.3V.
17	PLL_SEL	Input	Pullup	Selects between the PLL and reference clock as the input to the dividers. When HIGH, selects PLL. When LOW, selects the reference clock. LVCMOS interface levels.
18	V_{DD}	Power		Positive supply pin. Connect to 3.3V.
19	SEL0	Input	Pulldown	Determines output divider values in Table 3. LVCMOS interface levels.
20	SEL1	Input	Pulldown	Determines output divider values in Table 3. LVCMOS interface levels.

NOTE: *Pullup* and *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs					Outputs PLL_SEL = 1 PLL Enable Mode
SEL3	SEL2	SEL1	SEL0	Reference Frequency Range (MHz)*	Q0 - Q4, nQ0 - nQ4
0	0	0	0	250 - 700	÷ 1
0	0	0	1	125 - 350	÷ 1
0	0	1	0	62.5 - 175	÷ 1
0	0	1	1	31.25 - 87.5	÷ 1
0	1	0	0	250 - 700	÷ 2
0	1	0	1	125 - 350	÷ 2
0	1	1	0	62.5 - 175	÷ 2
0	1	1	1	250 -700	÷ 4
1	0	0	0	125 - 350	÷ 4
1	0	0	1	250 - 700	÷ 8
1	0	1	0	125 - 350	x 2
1	0	1	1	62.5 - 175	x 2
1	1	0	0	31.25 - 87.5	x 2
1	1	0	1	62.5 - 175	x 4
1	1	1	0	31.25 - 87.5	x 4
1	1	1	1	31.25 - 87.5	x 8

*NOTE: VCO frequency range for all configurations above is 250 to 700MHz.

TABLE 3B. PLL BYPASS FUNCTION TABLE

Inputs				Outputs PLL_SEL = 0 PLL Bypass Mode
SEL3	SEL2	SEL1	SEL0	Q0 - Q4, nQ0 - nQ4
0	0	0	0	÷ 4
0	0	0	1	÷ 4
0	0	1	0	÷ 4
0	0	1	1	÷ 8
0	1	0	0	÷ 8
0	1	0	1	÷ 8
0	1	1	0	÷ 16
0	1	1	1	÷ 16
1	0	0	0	÷ 32
1	0	0	1	÷ 64
1	0	1	0	÷ 2
1	0	1	1	÷ 2
1	1	0	0	÷ 4
1	1	0	1	÷ 1
1	1	1	0	÷ 2
1	1	1	1	÷ 1

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DDx}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Positive Supply Current				80	mA
I_{DDA}	Analog Supply Current				15	mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	MR, SEL0, SEL1, SEL2, SEL3	*V_{DDx} = V_{IN} = 3.465V			150	µA
		PLL_SEL	*V_{DDx} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	MR, SEL0, SEL1, SEL2, SEL3	*V_{DDx} = 3.465V, V_{IN} = 0V	-5			µA
		PLL_SEL	*V_{DDx} = 3.465V, V_{IN} = 0V	-150			µA

*NOTE: V_{DDx} denotes V_{DD}, V_{DDA}, and V_{DDO}.

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, FB_IN	*V_{DDx} = V_{IN} = 3.465V			150	µA
		nCLK, nFB_IN	*V_{DDx} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	CLK, FB_IN	*V_{DDx} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK, nFB_IN	*V_{DDx} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.
*NOTE: V_{DDx} denotes V_{DD}, V_{DDA}, and V_{DDO}.

TABLE 4D. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		230	350	460	mV
ΔV_{OD}	V_{OD} Magnitude Change			0	40	mV
V_{OS}	Offset Voltage		1.125	1.25	1.375	V
ΔV_{OS}	V_{OS} Magnitude Change			5	25	mV
I_{OSD}	Differential Output Short Circuit Current			-3.5		mA
I_{Os}	Output Short Circuit Current	CLK = V_{DD}, Q = 0V or CLK = 0V, nQ = 0V		-3.5		mA
I_{OFF}	Power Off Leakage	V_{OUT} = 0V or 3.465V, V_{DD} = 0V	-20	±1	+20	µA
V_{OH}	Output Voltage High			1.34	1.6	V
V_{OL}	Output Voltage Low		0.9	1.06		V

TABLE 5. INPUT FREQUENCY CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	CLK, nCLK	PLL_SEL = 1	31.25		700	MHz
			PLL_SEL = 0			700	MHz

TABLE 6. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency				700	MHz
t_{PD}	Propagation Delay; NOTE 1	PLL_SEL = 0V f ≤ 700MHz	4.5	5	5.5	ns
*t*sk(o)	Output Skew; NOTE 4, 5	PLL_SEL = 0V			15	ps
t(Ø)	Static Phase Offset; NOTE 2, 5, 6	PLL_SEL = 3.3V	-100	50	200	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 5, 6				25	ps
*t*jit(θ)	Phase Jitter; NOTE 3, 5				±50	ps
t_{PW}	Output Pulse Width		tcycle/2 - 85	tcycle/2	tcycle/2 + 85	ps
t_L	PLL Lock Time				1	ms
t_R	Output Rise Time	20% to 80% @ 50MHz	150		450	ps
t_F	Output Fall Time	20% to 80% @ 50MHz	150		450	ps

All parameters measured at f_{MAX} unless noted otherwise. All outputs terminated with 50Ω to $V_{DDO}/2$.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as the time difference between the input reference clock and the averaged feedback input signal across all conditions, when the PLL is locked and the input reference frequency is stable.
NOTE 3: Phase jitter is dependent on the input source used.
NOTE 4: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 6: Characterized at VCO frequency of 622MHz.

PARAMETER MEASUREMENT INFORMATION

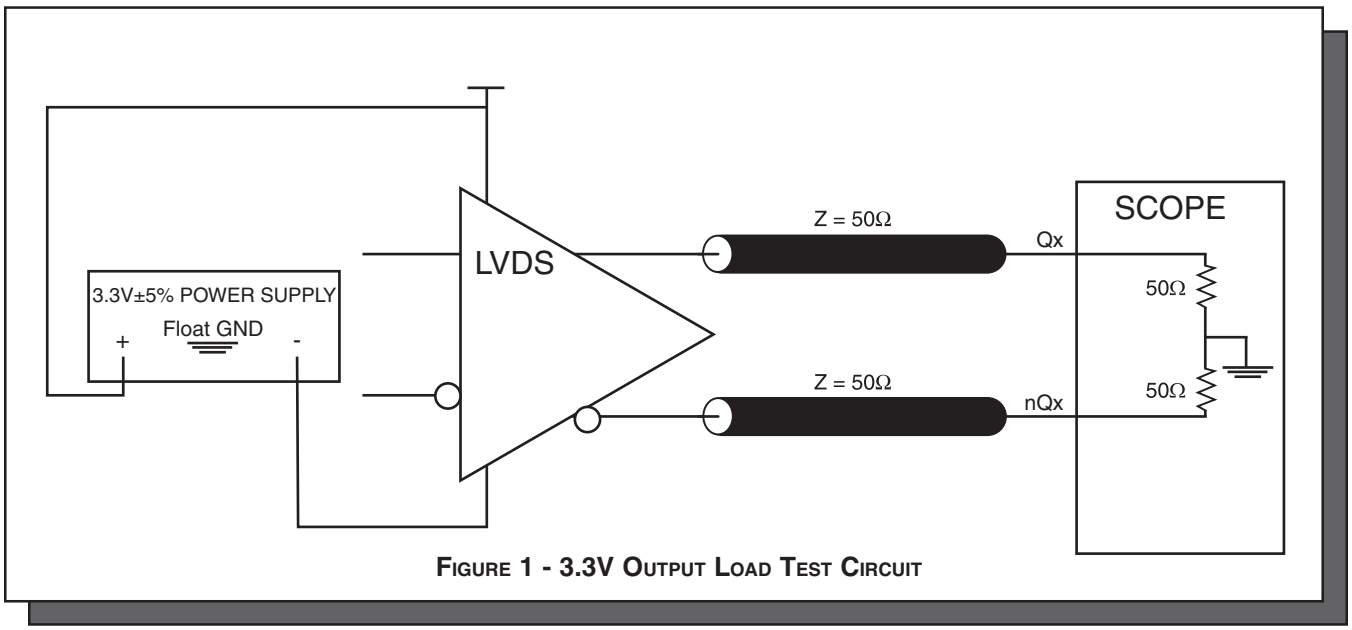


FIGURE 1 - 3.3V OUTPUT LOAD TEST CIRCUIT

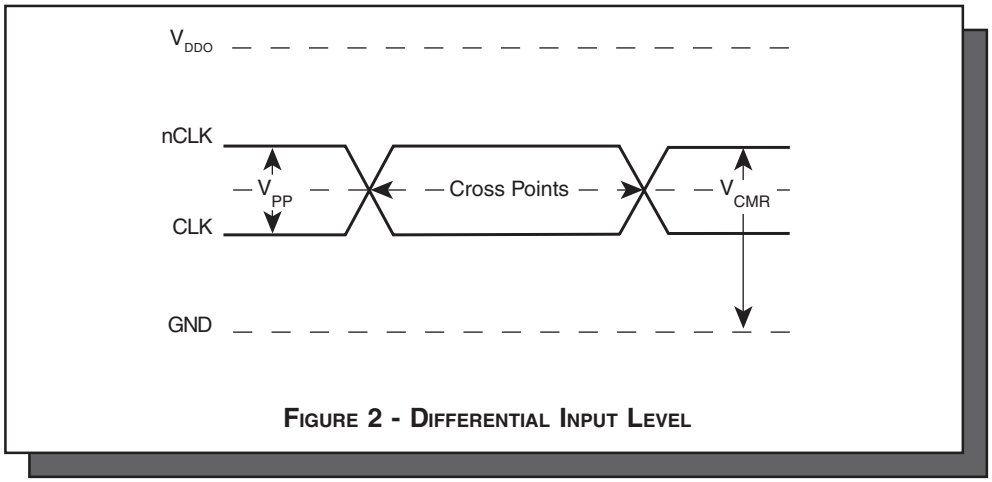


FIGURE 2 - DIFFERENTIAL INPUT LEVEL

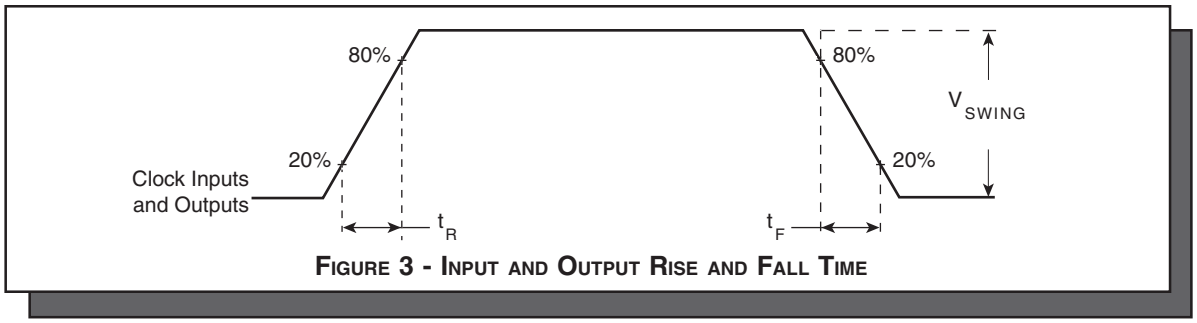


FIGURE 3 - INPUT AND OUTPUT RISE AND FALL TIME

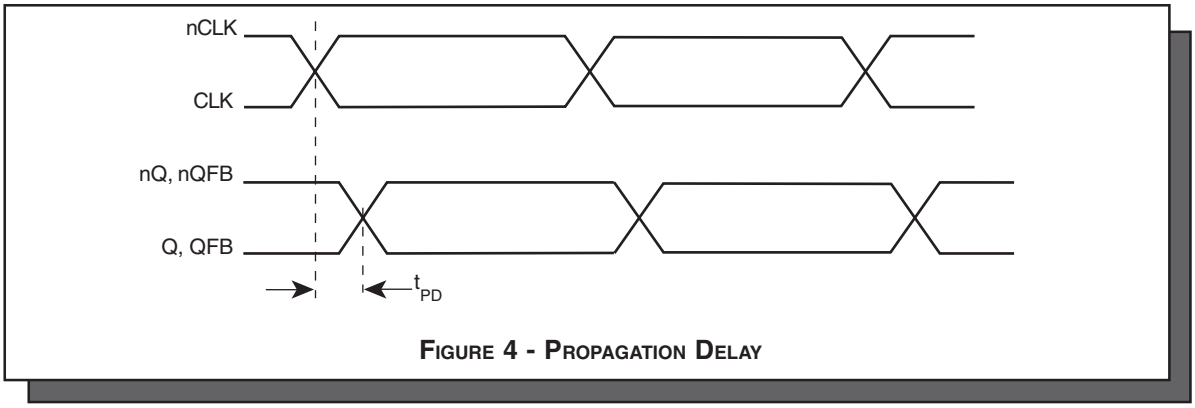


FIGURE 4 - PROPAGATION DELAY

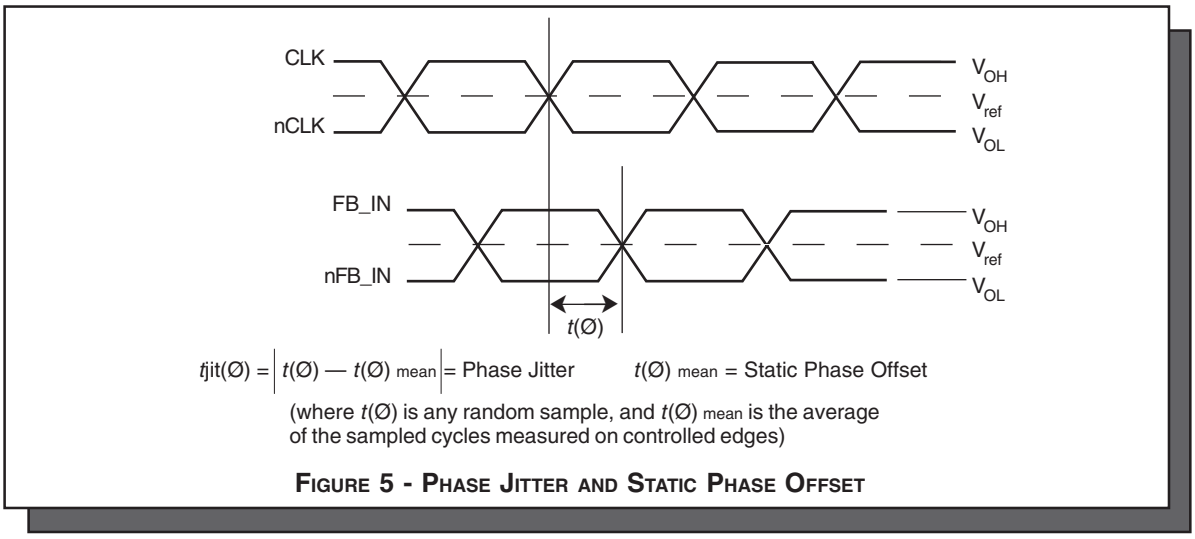


FIGURE 5 - PHASE JITTER AND STATIC PHASE OFFSET

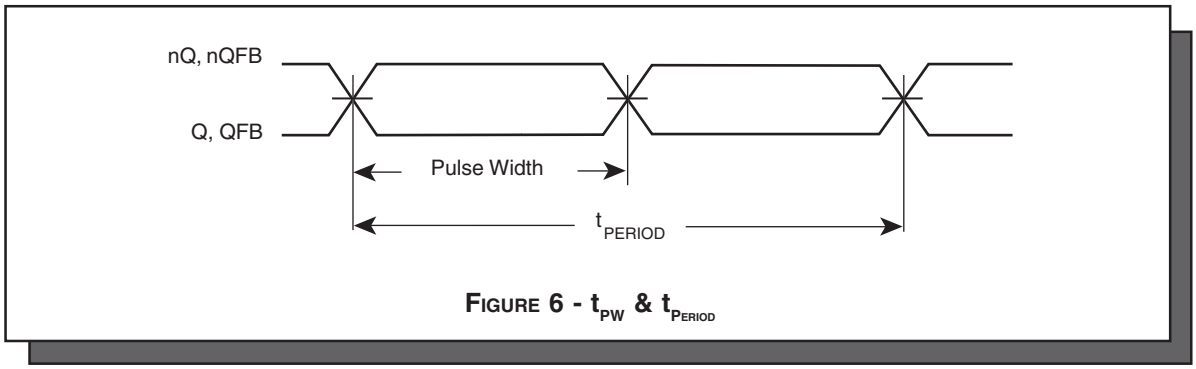
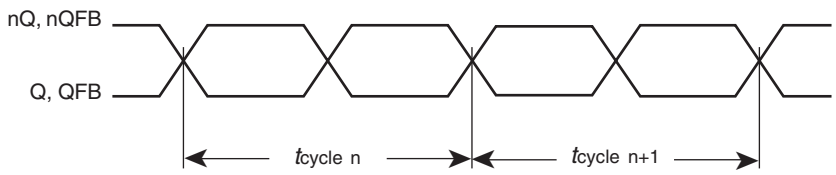


FIGURE 6 - t_{PW} & t_{PERIOD}



$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$
1000 Cycles

FIGURE 7 - Cycle-to-Cycle Jitter

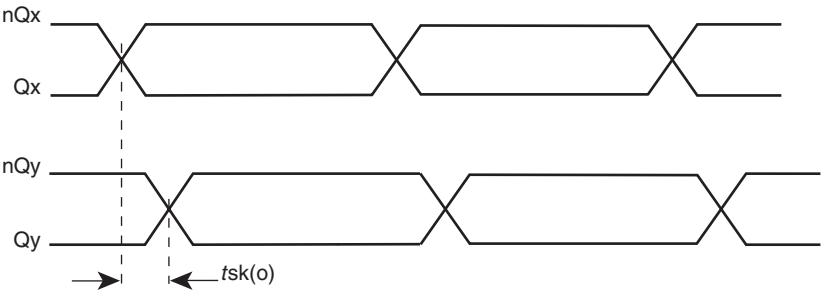


FIGURE 8 - OUTPUT SKEW

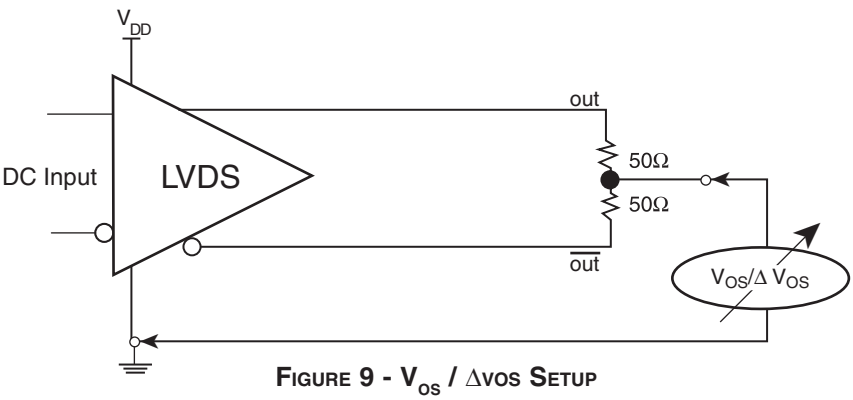


FIGURE 9 - V_{OS} / ΔV_{OS} SETUP

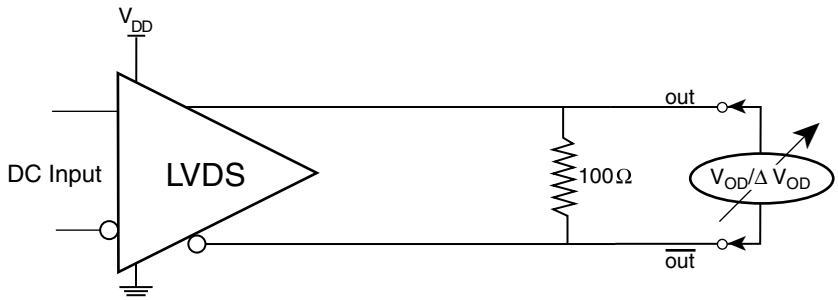


FIGURE 10 - VOD / ΔVOD SETUP

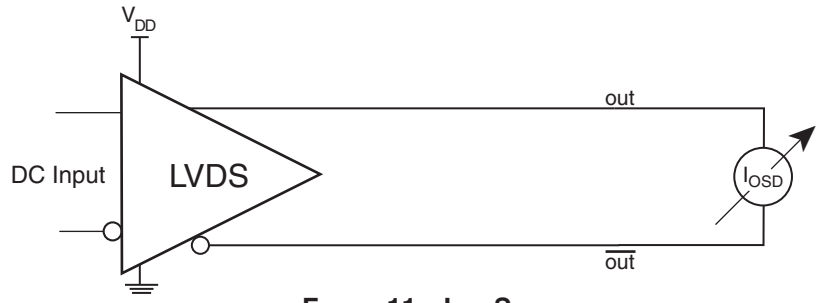


FIGURE 11 - I_{OSD} SETUP

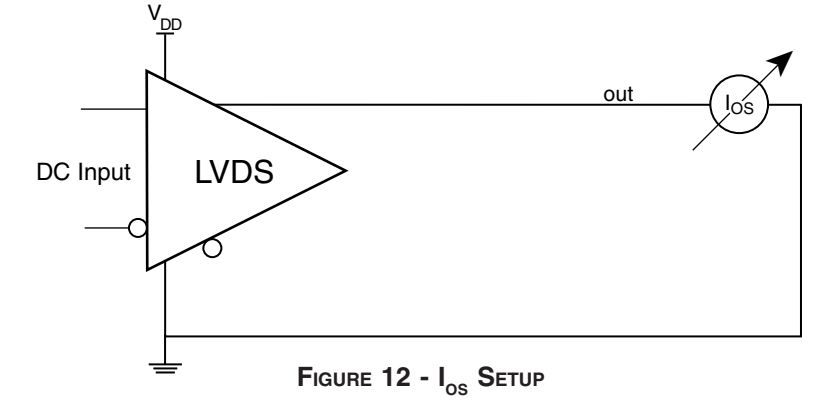


FIGURE 12 - I_{OS} SETUP

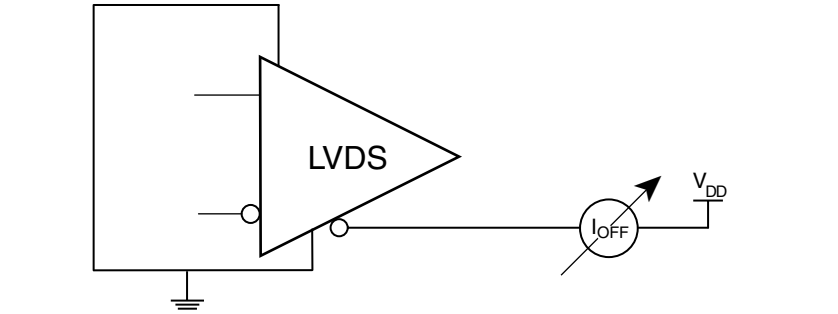


FIGURE 13 - I_{OFF} SETUP

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 14 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

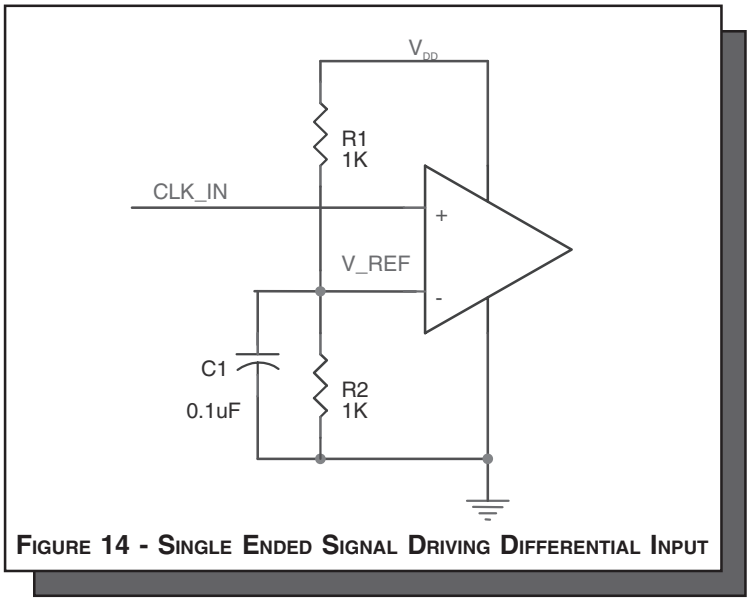


FIGURE 14 - SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

LAYOUT GUIDELINE

The schematic of the ICS8745-21 layout example is shown in *Figure 15.* The ICS8745-21 recommended PCB board layout for this example is shown in *Figure 16.* This layout example is used as a general guideline. The layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stacking of the P.C. board.

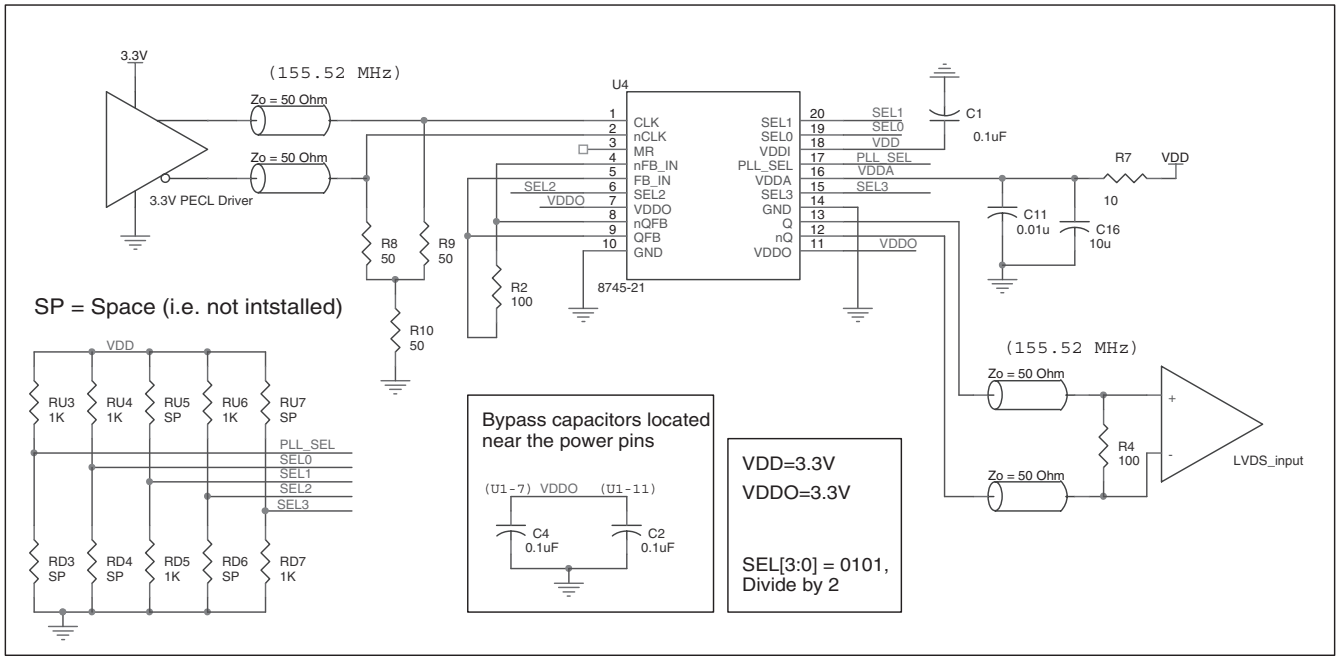


FIGURE 15 - ICS8745-21 LVDS ZERO DELAY BUFFER SCHEMATIC EXAMPLE

The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.

POWER AND GROUNDING

Place the decoupling capacitors C1, C2, and C4, as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the V_{DDA} pin as possible.

CLOCK TRACES AND TERMINATION

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a spearation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The matching termination resistors should be located as close to the receiver input pins as possible.

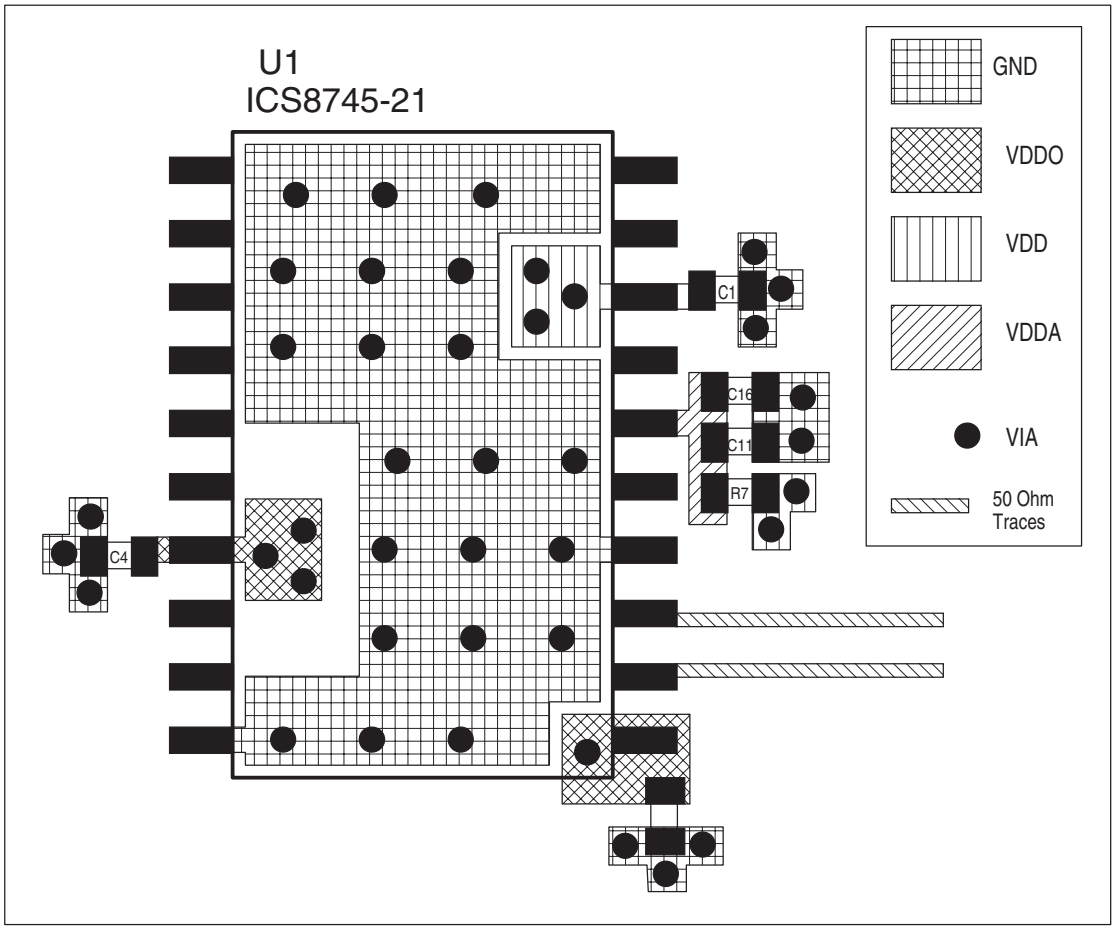


FIGURE 16 - PCB BOARD LAYOUT FOR ICS8745-21

TABLE 7. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8745-21 is: 3050

PACKAGE OUTLINE - M SUFFIX

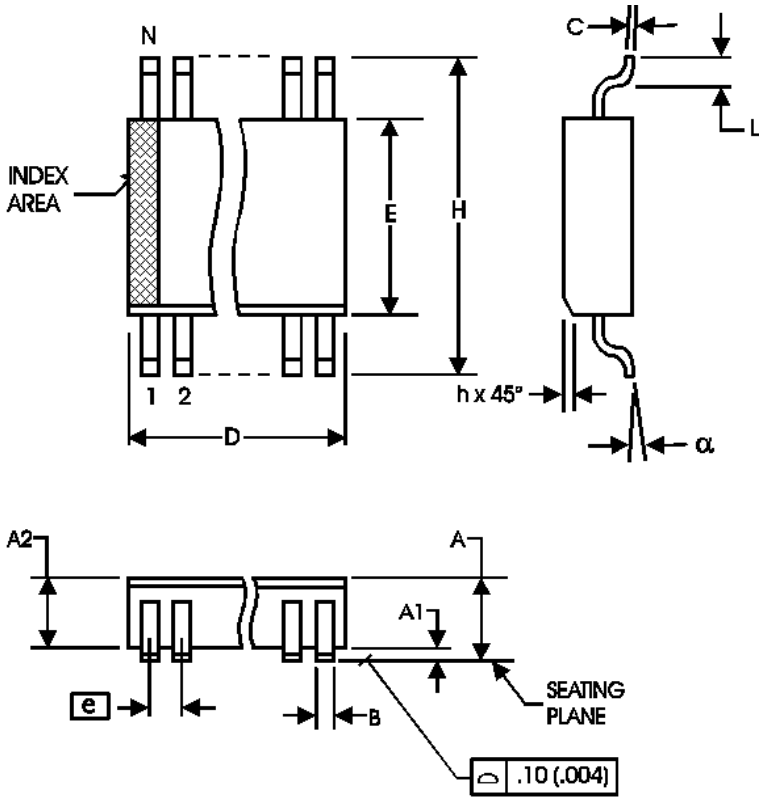


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	20	
A	--	2.65
A1	0.10	--
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	12.60	13.00
E	7.40	7.60
e	1.27 BASIC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-013, MO-119

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8745AM-21	ICS8745AM-21	20 Lead SOIC	38 per Tube	0°C to 70°C
ICS8745AM-21T	ICS8745AM-21	20 Lead SOIC on Tape and Reel	1000	0°C to 70°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	6	1 5 7	Revised Block Diagram. Added Output Skew row at 15ps Max. Added Output Skew Diagram.	10/31/01
B	3A 6	3 5	Added note at bottom of table. Added Note 6.	11/19/01
B	1	2	Changed inputs from LVDS interface levels to LVCMOS interface levels.	11/29/01
C	4C	4	Revised V_{CMR} row from "V_{DD} + 0.5" Minimum to "GND + 0.5" Minimum	11/30/01