Integrated Circuit Systems, Inc.

Preliminary Product Preview **ICS1524**

High-Performance Phase Controlled Clock Generator

General Description

The **ICS1524** is a user programmable high performance phase locked loop (PLL) frequency synthesizer capable of generating single ended (SSTL) and differential (PECL) outputs up to 250 MHz from a variety of timing sources. A second set of outputs (DPACLK) may be phase offset from the main set (CLK) providing for dynamic adjustment in 5.6^o to 22.5^o steps through the full 360^o. Phase adjustment is derived from a locked loop and therefore the delayed clock is phase stable relative to the main clock.

The **ICS1524** is a low-cost but very high-performance frequency generator. It is perfectly suited to general purpose phase controlled clock synthesis as well as line-locked and genlocked high-resolution video applications. Using ICS's advanced low-voltage CMOS mixed-mode technology, the **ICS1524** is an effective phase controlled clock synthesizer and also supports video projectors and displays at resolutions from VGA to beyond UXGA.

The advanced PLL uses either its internal programmable feedback divider or an external divider. The device available in a 24-pin wide small-outline integrated circuit (SOIC) package.

Through use of the serial I^{2}C bus, the **ICS1524** may be user programmed into a wide range of timing generation applications. Programmed configuration as well as certain operating status can be monitored through the same I^{2}C bus, making the device suitable for intelligent system designs.

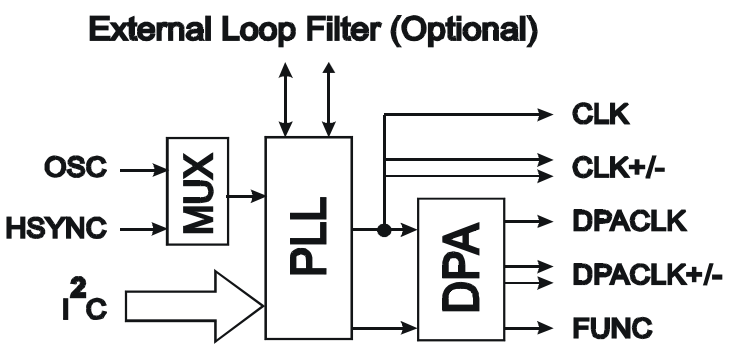
Features

- 250 MHz balanced PECL differential outputs
- 150 MHz single-ended SSTL_3 clock outputs
- Dynamic Phase Adjust (DPA) for DPACLK outputs
  - Software phase adjustment up to 160 MHz
  - 360^o Adjustment at up to 1/64 clock increments
- Wide input frequency range
  - 8 kHz to 100 MHz
- External or internal loop filter selection
- Uses 3.3 VDC
  - Inputs are 5 volt tolerant.
- I^{2}C-bus serial interface runs at either low speed (100 kHz) or high speed (400 kHz).
- Hardware and Software PLL Lock detection

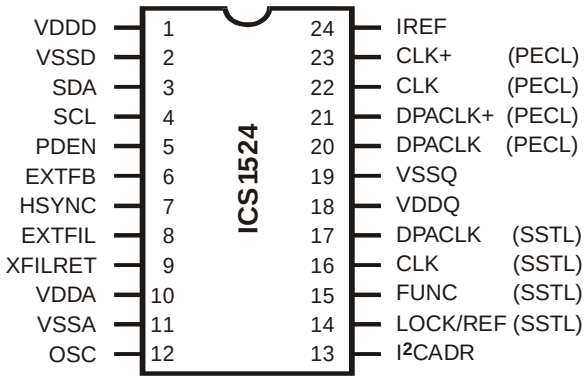
Applications

- General Purpose Frequency Synthesis
- LCD Monitors and Video Projectors
- Genlocking Multiple Video Subsystems
- Communications Clock Generation
- High Frequency Clock Genmeration

Block Diagram



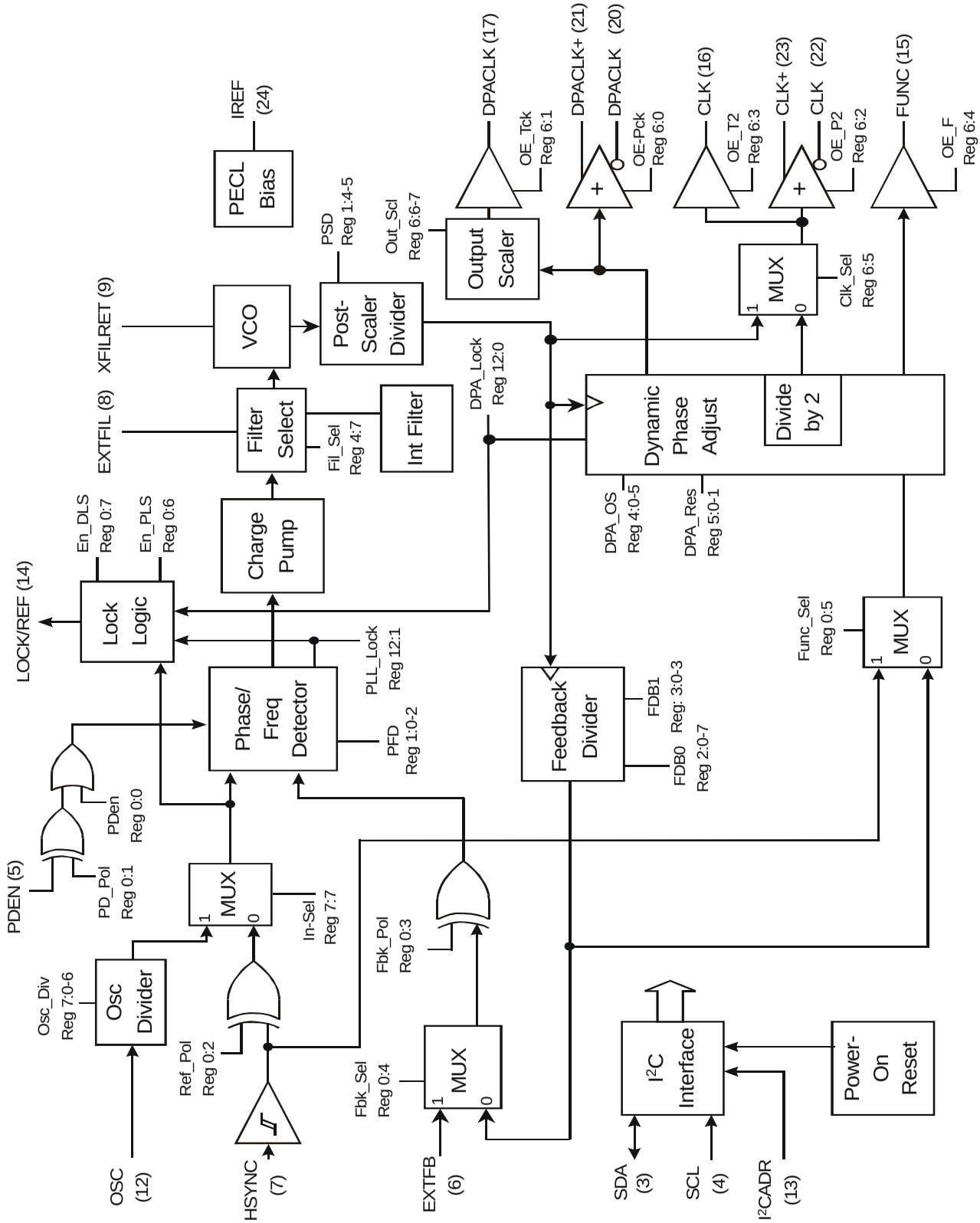
Pin Configuration



24 Pin 300-mil SOIC

I^{2}C-bus is a trademark of Philips Corporation.

Block Diagram



ICS Company Confidential

September 25, 2001

ICS1524 Block Diagram

Pin Descriptions

PIN NO.	PIN NAME	TYPE	DESCRIPTION	COMMENTS
1	VDDD	POWER	Digital supply	3.3V Power to digital circuitry
2	VSSD	POWER	Digital ground	Ground for digital circuitry
3	SDA	IN/OUT	Serial data	I²C-bus[1]
4	SCL	IN	Serial clock	I²C-bus[1]
5	PDEN	IN	PFD enable	Enables charge pump operation[1]
6	EXTFB	IN	External feedback	External divider input toPFD[1]
7	REF	IN	Phase Detector MUX Input	External Phase/Frequency Reference input to PLL[1]
8	EXTFIL	IN	External filter	External PLL loop filter
9	XFILRET	IN	External filter return	External PLL loop filter return
10	VDDA	POWER	Analog supply	3.3V for analog circuitry
11	VSSA	POWER	Analog ground	Ground for analog circuitry
12	OSC	IN	Phase Detector MUX Input	Divideable External Phase/Frequency Reference input to PLL[1, 2]
13	I²CADR	IN	I²C address	Chip I²C address select Low = 4Dh read, 4Ch write High = 4Fh read, 4Eh write
14	LOCK/REF	SSTL	Lock indicator/reference	Indicates PLL lock, DPA lock or REF input
15	FUNC	SSTL	Function output	Selectable Feedback Divider output
16	CLK	SSTL	Pixel clock	Non-Delayed Clock
17	DPACLK	SSTL	DPA Delayed Clock	Phase Delayed Clock
18	VDDQ	POWER	Output driver supply	3.3V VDD for output drivers
19	VSSQ	POWER	Output driver ground	Ground for output drivers
20	DPACLK–	PECL Open Drain	Phase Delayed PECL clock -	DPA Delayed Inverted PECL Clock 45/55%up to 135 MHz
21	DPACLK+	PECL Open Drain	Phase Delayed PECL clock +	DPA Delayed PECL Clock 45/55%up to 135 MHz
22	CLK–	PECL Open Drain	PECL clock -	Non-Delayed Inverted PECL Clock 45/55%up to 200 MHz 40/50%up to 250 MHz
23	CLK+	PECL Open Drain	PECL clock +	Non-Delayed PECL Clock 45/55%up to 200 MHz 40/50%up to 250 MHz
24	IREF	IN	Reference current	Reference current for PECL outputs

Notes:

1. These LVTTL inputs are 5V-tolerant.
2. Connect to ground if unused.

I²C Register Map Summary

Register Index	Name	Access	Bit Name	Bit #	Reset Value	Description
0h	Input Control	R / W	PDen	0	1	Phase Detector Enable (0=Disable 1=Enable)
			PD_Pol	1	0	Phase Detector Input Select
			Ref_Pol	2	0	External Reference Polarity (0=Positive Edge, 1=Negative Edge)
			Fbk_Pol	3	0	External Feedback Polarity (0=Positive Edge, 1=Negative Edge)
			Fbk_Sel	4	0	External Feedback Select (0=Internal Feedback, 1=External)
			Func_Sel	5	0	Function Output Select (0=Recovered FEEDBACK, 1=INPUT)
			EnPLS	6	1	Enable PLL Lock/Ref Status Output (0=Disable 1=Enable)
			EnDLS	7	0	Enable DPA Lock/Ref Status Output (0=Disable 1=Enable)
1h	Loop Control	R / W *	PFD0-2	0-2	0	Phase Detector Gain (000=1ua, 001=2ua, 010=4ua...111=128ua)
			Reserved	3	0	Reserved
			PSD0-1	4-5	0	Post-Scaler Divider (0 = 2, 1 = 4, 2 = 8, 3 = 16)
			Reserved	6-7	0	Reserved
2h	FdBk Div 0	R / W *	FBD0-7	0-7	FF	PLL FeedBack Divider LSBs (bits 0-7) * (Actual add 8)
3h	FdBk Div 1	R / W *	FBD8-11	0-3	F	PLL Feedback Divider MSBs (bits 8-11) *
			Reserved	4-7	0	Reserved
4h	DPA Offset	R / W	DPA_OS0-5	0-5	0	Dynamic Phase Aligner Offset
			Reserved	6	0	Reserved
			Fil_Sel	7	1	Loop Filter Select (0=External, 1=Internal)
5h	DPA Control	R / W **	DPA_Res0-1	0-1	3	DPA Resolution (0=16 elements, 1=32, 2=Reserved, 3=64)
			Metal_Rev	2-7	0	Metal Mask Revision Number
6h	Output Enables	R / W	OE_Pck	0	1	Output Enable for PECL DPACLK (0=High Z, 1=Enabled)
			OE_Tck	1	1	Output Enable for STTL_3 DPACLK (0=High Z, 1=Enabled)
			OE_P2	2	1	Output Enable for PECL CLK (0=High Z, 1=Enabled)
			OE_T2	3	1	Output Enable for STTL_3 CLK (0=High Z, 1=Enabled)
			OE_F	4	1	Output Enable for STTL_3 FEEDBACK (0=High Z, 1=Enabled)
			Clk_Sel	5	1	Select CLK Output (0=DPACLK/2, 1=CLK)
			Out_Scl	6-7	0	SSTL DPACLK (Pin 17) Scaler (0 = 1, 1 = 2, 2 = 4, 3 = 8)
7h	Osc_Div	R / W	Osc_Div 0-6	0-6	0	Osc Divider Modulus
			In-Sel	7	1	Phase Detector Input MUX Selector (0=HSYNC, 1=OSC)
8h	Reset	Write	DPA	0-3	x	Writing xAh resets DPA and loads working register 5
			PLL	4-7	x	Writing 5xh resets PLL and loads working registers 1-3
10h	Chip Ver	Read	Chip Ver	0-7	17	Chip Version
11h	Chip Rev	Read	Chip Rev	0-7	C2	Value Increments with each all-layer change.
12h	Rd_Reg	Read	DPA_Lock	0	N/A	DPA Lock Status (0=Unlocked, 1=Locked)
			PLL_Lock	1	N/A	PLL Lock Status (0=Unlocked, 1=Locked)
			Reserved	2-7	0	Reserved

* Identifies double-buffered registers. Working registers are loaded during software PLL reset.

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Absolute Maximum Ratings

VDD, VDDA, VDDQ (to VSS) 4.3V
Digital Inputs . . . . . VSS – 0.3V to 5.5V
Analog Outputs . . . . . VSSA – 0.3V to VDDA +0.3V
Digital Outputs . . . . . VSSQ – 0.3V to VDDQ +0.3V
Storage Temperature . . . . . – 65°C to +150°C
Junction Temperature . . . . . 175°C
Soldering Temperature . . . . . 260°C
ESD Susceptibility . . . . . > 2 KV

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (VCC)	3.14	3.3	3.46	V
Ambient Operating Temperature	0	25	85 . °C	

DC Supply Current

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Supply Current, Digital	IDDD	VDDD = 3.6V	—	25	mA
Supply Current, Output Drivers	IDDQ	VDDQ = 3.6V, no output drivers enabled.	—	6	mA
Supply Current, Analog	IDDA	VDDA = 3.6V	—	5	mA

Digital Inputs (SDA, SCL, PDEN, EXTFB, HSYNC, OSC, I^2CADR)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	VIH		2	5.5	V
Input Low Voltage	VIL		VSS-0.3	0.8	V
Input Hysteresis			0.2	0.6	V
Input High Current	IIH	V_{IH} = VDD	—	±10	µA
Input Low Current	IIL	V_{IL} = 0	—	±200	µA
Input Capacitance	Cin		—	10	pF

SDA (In Output Mode: SDA is Bidirectional)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output Low Voltage	VOL	IOUT = 3 mA. VOH = 6.0V maximum as determined by the external pull-up resistor.		0.4	V

PECL Outputs (DPACLK+, DPACLK–, CLK+, CLK -)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output High Voltage	VOH	IOUT = 0	—	VDD	V
Maximum Output Frequency	Fp MAX	VDDD = 3.3V	—	250	MHz
Output Low Voltage (Note: VOL must not fall below the level given so that the correct value for IOUT can be maintained.)	VOL	IOUT = programmed value	1.0	—	V

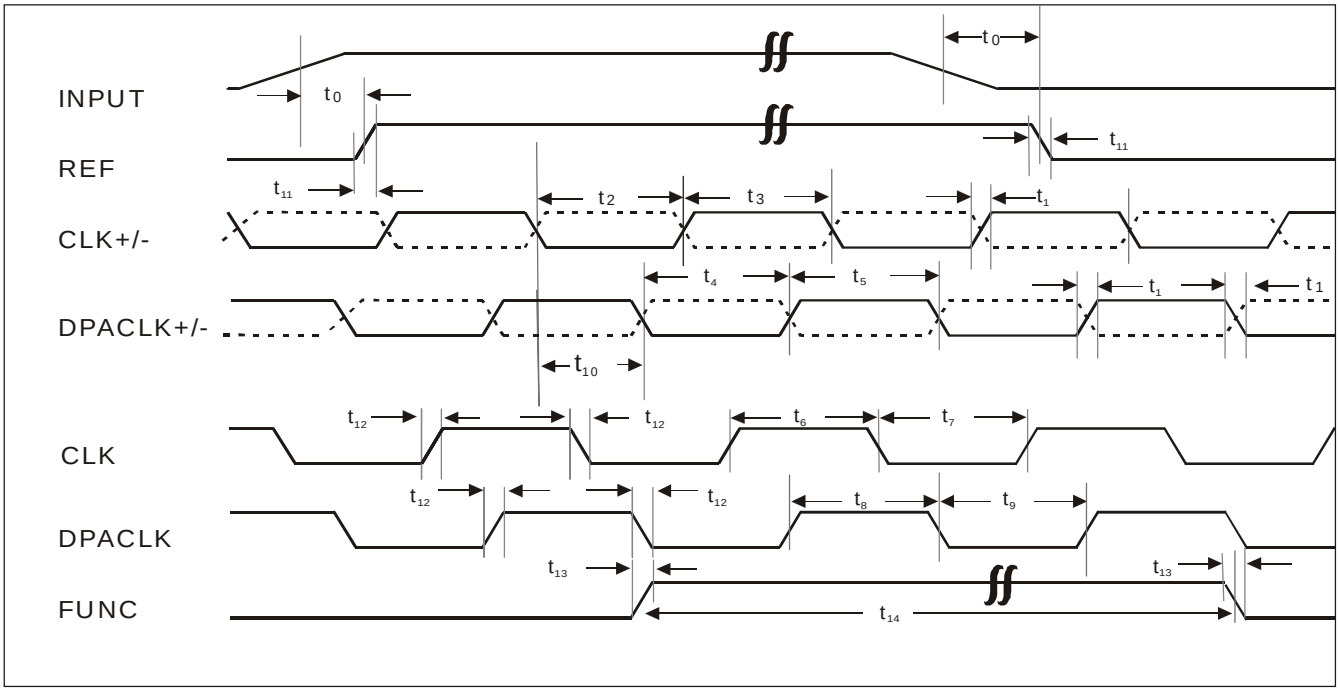
SSTL-3 Outputs (DPACLK, CLK, FUNC, LOCK/REF)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output Resistance	R_O	1 <V_O<2V	—	80	Ω
Maximum Output Frequency	Fs MAX	VDDD = 3.3V	—	150	MHz

AC Input Characteristics

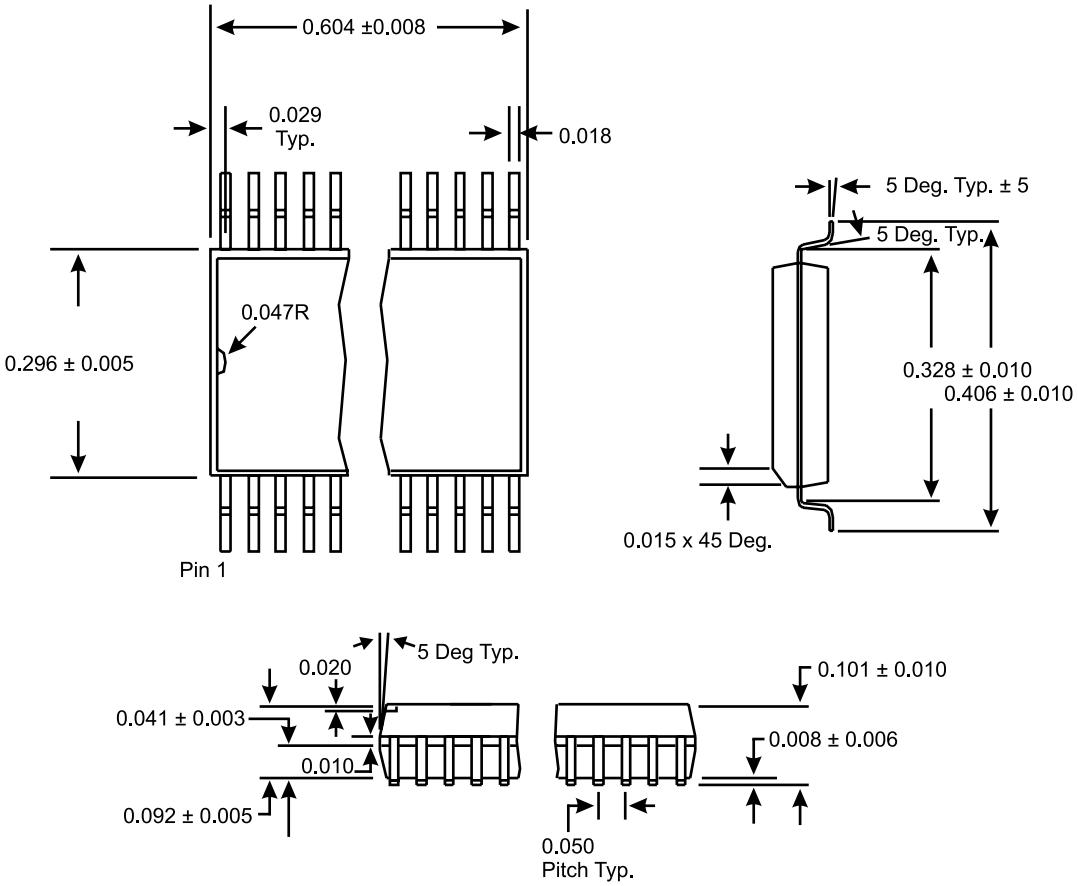
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
HSYNC Input Frequency	f_{HSYNC}		.008	10	MHz
OSC Input Frequency	f_{OSC}		.02	100	MHz

Output Timing Diagram



Output Timing Table

Symbol	Timing Description	Min	Typ	Max	Units	Notes
t_0	HSYNC Input to REF output delay	-	5.0	-	ns	1M Ohm, < 2 pf load
t_1	PECL outputs transition time	-	2	-	ns	75 Ohm Termination, < 1 pf load
t_2, t_3	PECL CLK duty cycle	45	50	55	%	T_{CLK} < 200 MHz
t_2, t_3	PECL CLK duty cycle	40	50	60	%	T_{CLK} < 240 MHz
t_4, t_5	PECL DPACLK duty cycle	40	50	60	%	T_{CLK} < 200 MHz
t_6, t_7	SSTL CLK duty cycle	45	50	55	%	T_{CLK} < 200 MHz
t_8, t_9	SSTL DPACLK duty cycle	45	50	55	%	T_{CLK} < 135 MHz
t_{10}	DPA Offset Delay	-	3ns+T_{DPA}	-	ns	T_{DPA} = DPA Offset (Reg4) * T_{CLK} / [DPA Resolution (Reg5)]
t_{11}	REF output transition time	-	2	-	ns	1M Ohm, < 2 pf load
t_{12}	SSTL clock output transition time	-	2		ns	1M Ohm, < 2 pf load
t_{13}	FUNC output transition time	-	2	-	ns	1M Ohm, < 2 pf load
t_{14}	FUNC Pulse Width	-	4	-	T_{CLK}	1M Ohm, < 2 pf load



24-Pin SOIC (wide body)

Ordering Information			
Part/Order Number	**Marking**	**Package**	**Shipping**
ICS1524AM	ICS1524AM	SIOC-24	Tubes
ICS1524AMT	ICS1524AM	SIOC-24	Tape and Reel

NOTES

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