PRELIMINARY

Integrated Circuit Systems, Inc.

ICS8312
LOW SKEW, 1-TO-12 LVCMOS FANOUT BUFFER

GENERAL DESCRIPTION

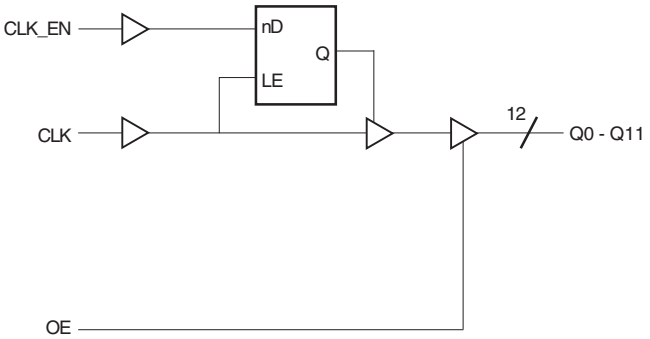
The ICS8312 is a low skew, 1-to-12 LVCMOS Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8312 single ended clock input accepts LVCMOS or LVTTL input levels. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 12 to 24 by utilizing the ability of the outputs to drive two series terminated lines.

The ICS8312 is characterized at full 3.3V, 2.5V, and 1.8V output operating supply modes. Guaranteed output and part-to-part skew characteristics along with the 1.8V output capabilities makes the ICS8312 ideal for high performance, single ended applications that also required a limited output voltage.

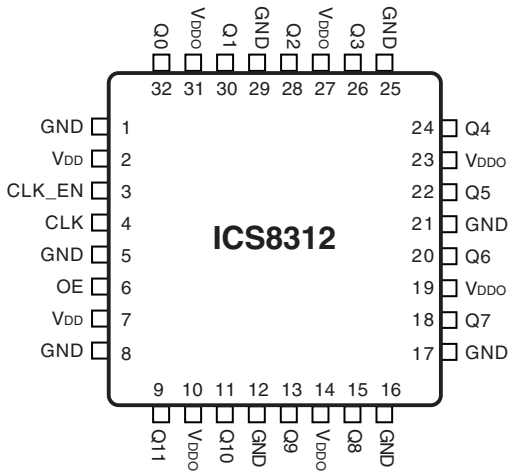
FEATURES

- 12 LVCMOS outputs
- LVCMOS clock input
- Maximum output frequency up to 250MHz
- Output skew: 80ps (typical)
- Part-to-part skew: TBD
- Full 3.3V, 2.5V, and 1.8V operating supply modes
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
7mm x 7mm x 1.4mm
Y Pacakge
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 5, 8, 12, 16, 17, 21, 25, 29	GND	Power		Power supply ground. Connect to ground.
2, 7	V_{DD}	Power		Positive supply pins. Connect 3.3, 2.5V, or 1.8V.
3	CLK_EN	Input	Pullup	Synchronous control for enabling and disabling clock outputs. LVCMOS / LVTTL interface levels.
4	CLK	Input	Pulldown	Clock input. LVCMOS interface level.
6	OE	Input	Pullup	Output enable. Controls enabling and disabling of outputs Q0 thru Q11.
9, 11, 13, 15, 18, 20, 22, 24, 26, 28, 30, 32	Q11, Q10, Q9, Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Q0 thru Q11 outputs. 10Ω typical output impedance.
10, 14, 19, 23, 27, 31	V_{DDO}	Power		Output supply pins. Connect 3.3V, 2.5V, 1.8V.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
R_{OUT}	Output Impedance			10		Ω

TABLE 3A. OUTPUT ENABLE AND CLOCK ENABLE FUNCTION TABLE

Control Inputs		Output
OE	CLK_EN	Q0 thru Q11
0	X	Hi-Z
1	0	LOW
1	1	Follows CLK input

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs			Outputs
OE	CLK_EN	CLK	Q0 thru Q11
1	1	0	LOW
1	1	1	HIGH

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DDx}	4.6V
Input Voltage, V_I	-0.5V to V_{DD}+0.5V
Outputs Voltage, V_O	-0.5V to V_{DDO}+0.5V
Package Thermal Impedance, θJA	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			0		mA
I_{DDO}	Output Supply Current			0		mA

TABLE 4B. LVCMOS DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK		2		V_{DD} + 0.3	V
		CLK_EN, OE		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	CLK		-0.3		1.3	V
		CLK_EN, OE		-0.3		0.8	V
I_{IH}	Input High Current	CLK_EN, OE	$V_{DD} = V_{IN} = 3.465V$			5	µA
		CLK_SEL	$V_{DD} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	CLK_EN, OE	$V_{DD} = 3.465$, $V_{IN} = 0V$	-150			µA
		CLK_SEL	$V_{DD} = 3.465$, $V_{IN} = 0V$	-5			µA
V_{OH}	Output High Voltage; NOTE 1			2.6			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See page 7, Figure 1A, 3.3V Load Test Circuit.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay Low to High; NOTE 1	f ≤ 250MHz		2.2		ns
tp_{HL}	Propagation Delay High to Low; NOTE 1	f ≤ 250MHz				ns
*t*sk(o)	Output Skew; NOTE 2, 5			80		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5			TBD		ps
t_R	Output Rise Time; NOTE 4	30% to 70%		300		ps
t_F	Output Fall Time; NOTE 4	30% to 70%		300		ps
odc	Output Duty Cycle			50		%
t_{EN}	Output Enable Time; NOTE 4			TBD		ns
t_{DIS}	Output Disable TIme; NOTE 4			TBD		ns

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as the skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 4C. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			0		mA
I_{DDO}	Output Supply Current			0		mA

TABLE 4D. LVCMOS DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK		2		V_{DD} + 0.3	V
		CLK_EN, OE		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	CLK		-0.3		1.3	V
		CLK_EN, OE		-0.3		0.8	V
I_{IH}	Input High Current	CLK_EN, OE	$V_{DD} = V_{IN} = 2.625V$			5	µA
		CLK_SEL	$V_{DD} = V_{IN} = 2.625V$			150	µA
I_{IL}	Input Low Current	CLK_EN, OE	$V_{DD} = 2.625V$, $V_{IN} = 0V$	-150			µA
		CLK_SEL	$V_{DD} = 2.625V$, $V_{IN} = 0V$	-5			µA
V_{OH}	Output High Voltage; NOTE 1			1.8			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See page 7, Figure 1B, 2V Load Test Circuit.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay Low to High; NOTE 1	f ≤ 250MHz		2.2		ns
tp_{HL}	Propagation Delay High to Low; NOTE 1	f ≤ 250MHz				ns
*t*sk(o)	Output Skew; NOTE 2, 5			80		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5			TBD		ps
t_R	Output Rise Time; NOTE 4	30% to 70%		330		ps
t_F	Output Fall Time; NOTE 4	30% to 70%		330		ps
odc	Output Duty Cycle			50		%
t_{EN}	Output Enable Time; NOTE 4			TBD		ns
t_{DIS}	Output Disable TIme; NOTE 4			TBD		ns

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as the skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 4E. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 1.8V \pm 0.2V$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		1.6	1.8	2.0	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current			0		mA
I_{DDO}	Output Supply Current			0		mA

TABLE 4F. LVCMOS DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 1.8V \pm 0.2V$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK		2		V_{DD} + 0.3	V
		CLK_EN, OE		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	CLK		-0.3		1.3	V
		CLK_EN, OE		-0.3		0.8	V
I_{IH}	Input High Current	CLK_EN, OE	$V_{DD} = V_{IN} = 2.625V$			5	µA
		CLK_SEL	$V_{DD} = V_{IN} = 2.625V$			150	µA
I_{IL}	Input Low Current	CLK_EN, OE	$V_{DD} = 2.625V$, $V_{IN} = 0V$	-150			µA
		CLK_SEL	$V_{DD} = 2.625V$, $V_{IN} = 0V$	-5			µA
V_{OH}	Output High Voltage; NOTE 1			1.15			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See page 8, Figure 1C, 1.8V Load Test Circuit.

TABLE 5C. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 1.8V \pm 0.2V$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					MHz
tp_{LH}	Propagation Delay Low to High; NOTE 1	f ≤ MHz		3.3		ns
tp_{HL}	Propagation Delay High to Low; NOTE 1	f ≤ MHz				ns
*t*sk(o)	Output Skew; NOTE 2, 5			80		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5			TBD		ps
t_R	Output Rise Time; NOTE 4	30% to 70%		280		ps
t_F	Output Fall Time; NOTE 4	30% to 70%		280		ps
odc	Output Duty Cycle			50		%
t_{EN}	Output Enable Time; NOTE 4			TBD		ns
t_{DIS}	Output Disable TIme; NOTE 4			TBD		ns

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as the skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

PARAMETER MEASUREMENT INFORMATION

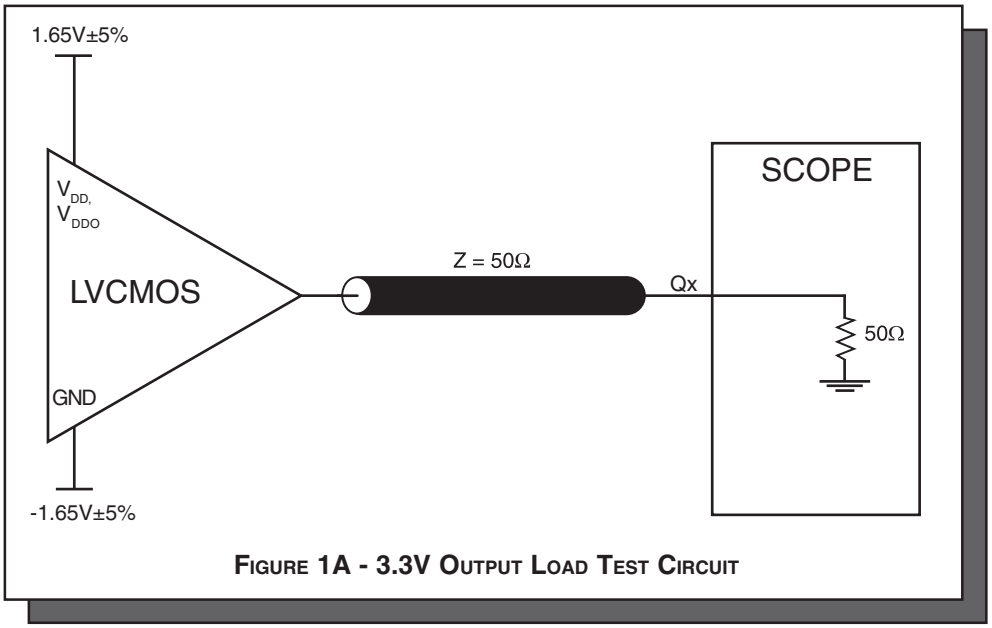


FIGURE 1A - 3.3V OUTPUT LOAD TEST CIRCUIT

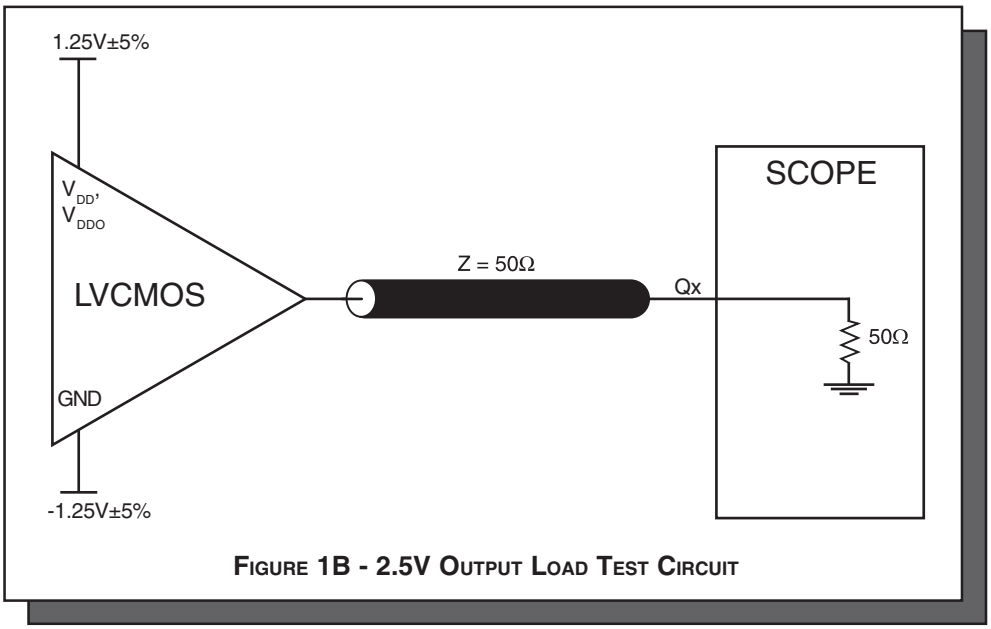


FIGURE 1B - 2.5V OUTPUT LOAD TEST CIRCUIT

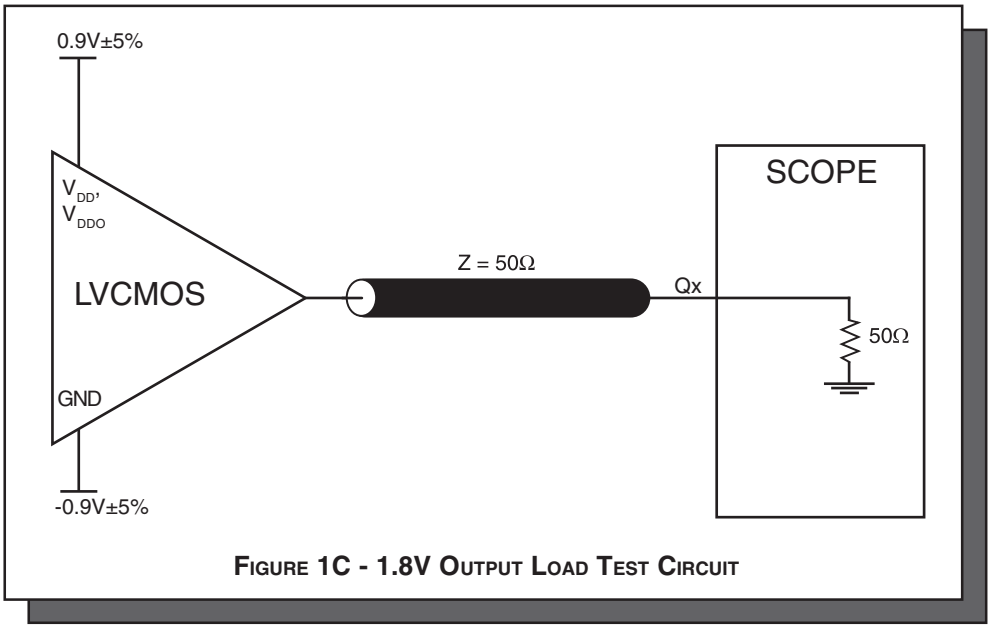


FIGURE 1C - 1.8V OUTPUT LOAD TEST CIRCUIT

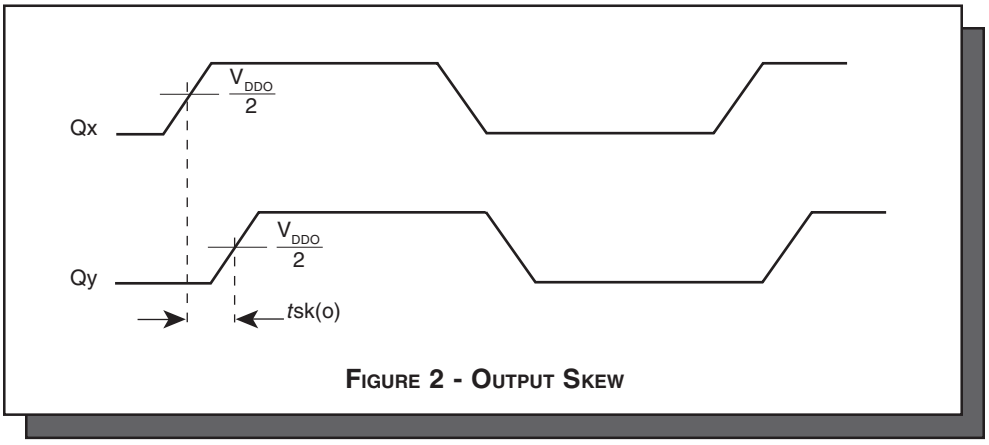


FIGURE 2 - OUTPUT SKEW

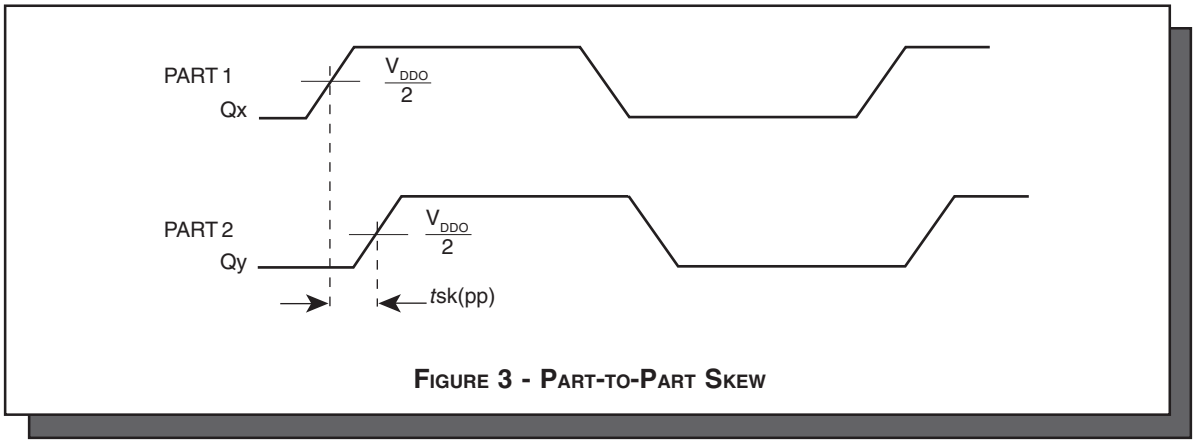


FIGURE 3 - PART-TO-PART SKEW

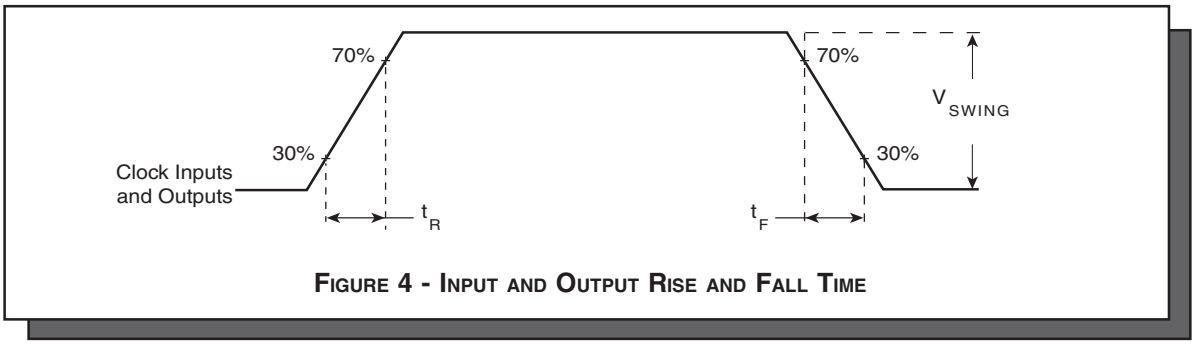


FIGURE 4 - INPUT AND OUTPUT RISE AND FALL TIME

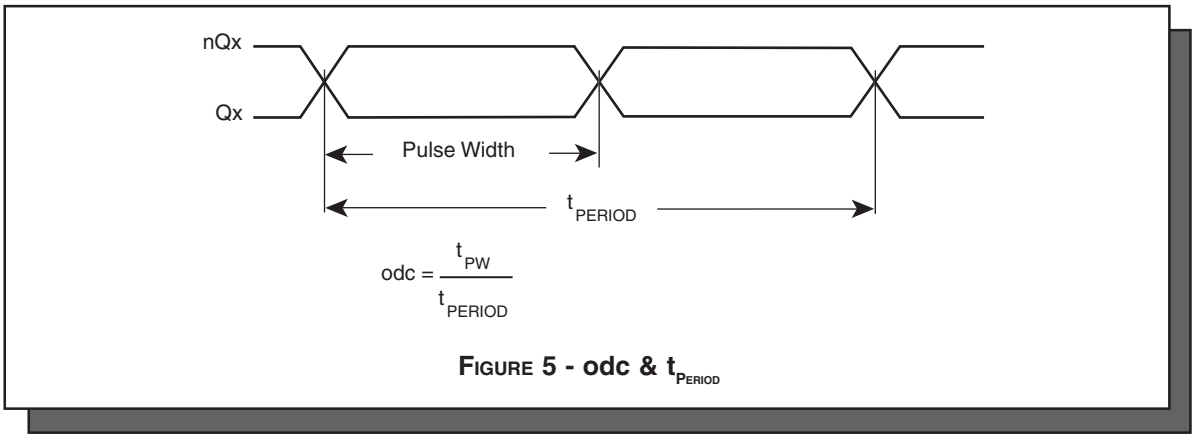


FIGURE 5 - odc & t_{PERIOD}

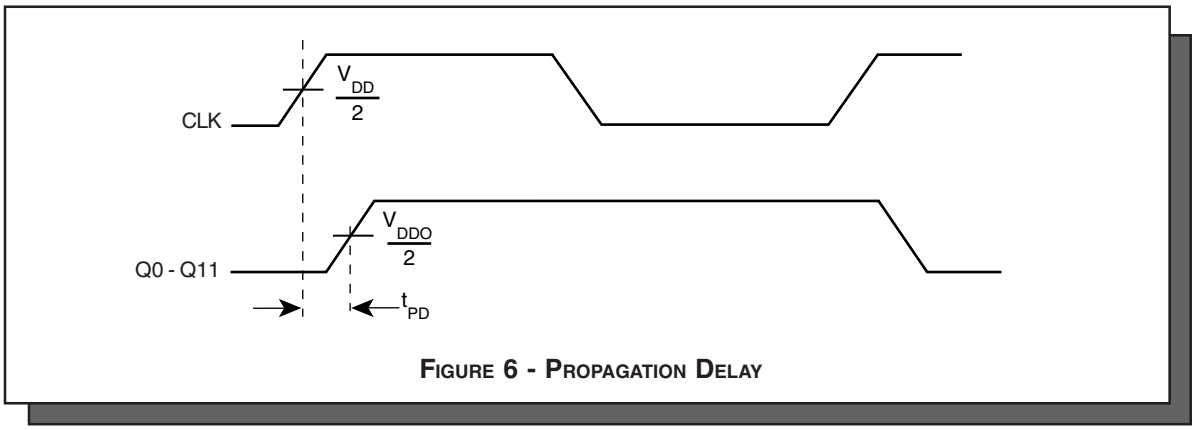


FIGURE 6 - PROPAGATION DELAY

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8312 is: 339

PACKAGE OUTLINE - Y SUFFIX

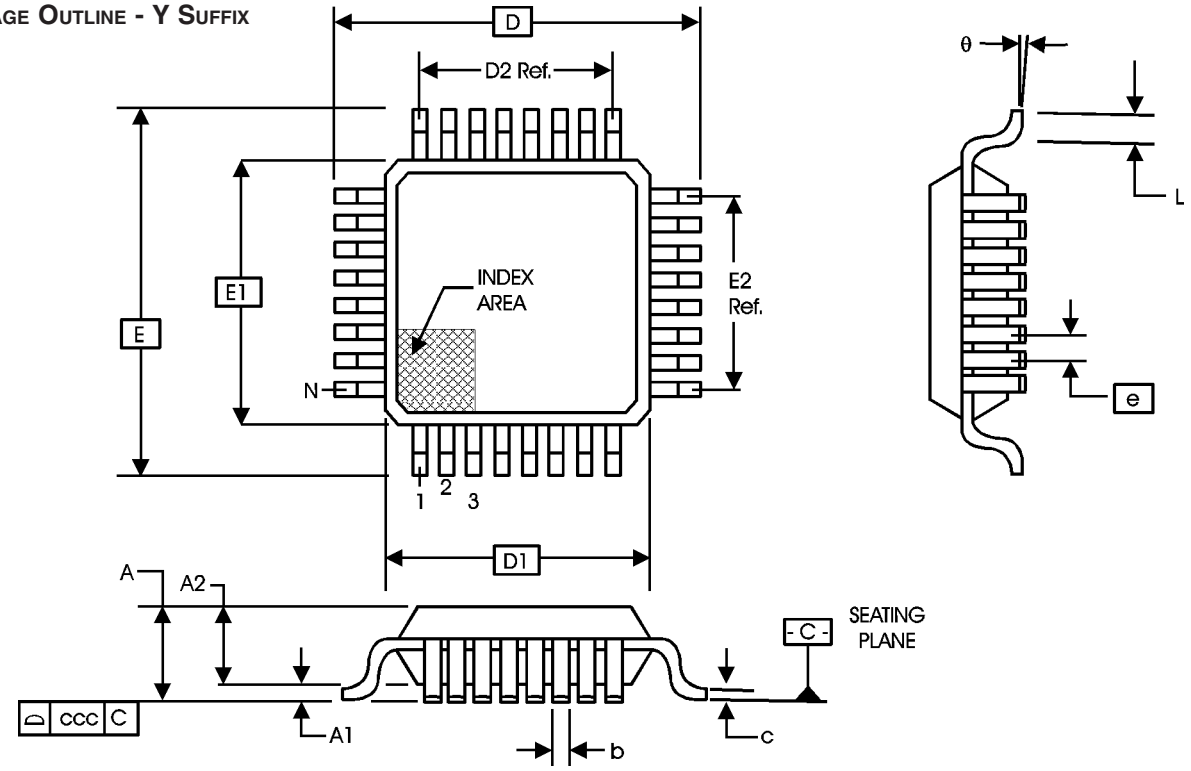


TABLE 6. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8312AY	ICS8312AY	32 Lead LQFP	250 per tray	0°C to 70°C
ICS8312AYT	ICS8312AY	32 Lead LQFP on Tape and Reel	1000	0°C to 70°C