# PRELIMINARY

**Integrated Circuit Systems, Inc.**

# ICS8432-111
## 700MHz/350MHz
### DIFFERENTIAL-TO-3.3V LVPECL FREQUENCY SYNTHESIZER

## GENERAL DESCRIPTION

The ICS8432-111 is a general purpose, dual output Differential-to-3.3V LVPECL High Frequency Synthesizer and a member of the HiPerClockS™ family of High Performance Clocks Solutions from ICS. The ICS8432-111 has a selectable differential CLK, nCLK pair or LVCMOS TEST_CLK. The TEST_CLK input accepts LVCMOS or LVTTL input levels and translates them to 3.3V LVPECL levels. The CLK, nCLK pair can accept most standard differential input levels.The VCO operates at a frequency range of 200MHz to 700MHz. The VCO frequency is programmed in steps equal to the value of the input differential or single ended reference frequency. Output frequencies up to 700MHz for FOUT and 350MHz for FOUT/2 can be programmed using the serial or parallel interfaces to the configuration logic. The low phase noise characteristics and the multiple frequency outputs of the ICS8432-111 makes it an ideal clock source for Fiber Channel 1 and 2, and Infiniband applications.

## FEATURES

- Dual differential 3.3V LVPECL outputs

- Selectable differential CLK, nCLK pair or LVCMOS TEST_CLK

- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVHSTL, LVDS, SSTL, HCSL

- TEST_CLK can accept the following input types: LVCMOS or LVTTL

- Maximum FOUT frequency up to 700MHz
  Maximum FOUT/2 frequency up to 350MHz

- 14MHz to 25MHz differential input or TEST_CLK input frequency

- VCO range: 200MHz - 700MHz

- Parallel or serial interface for programming counter and VCO frequency multiplier and dividers

- RMS period jitter: TBD

- Cycle-to-cycle jitter: 25ps (maximum)

- 3.3V supply voltage

- 0°C to 70°C ambient operating temperature

## BLOCK DIAGRAM
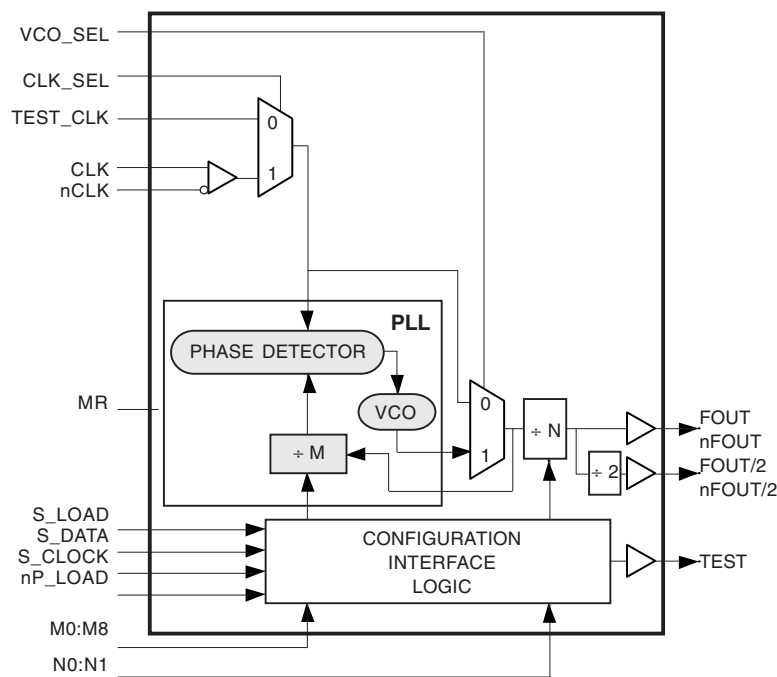


## PIN ASSIGNMENT
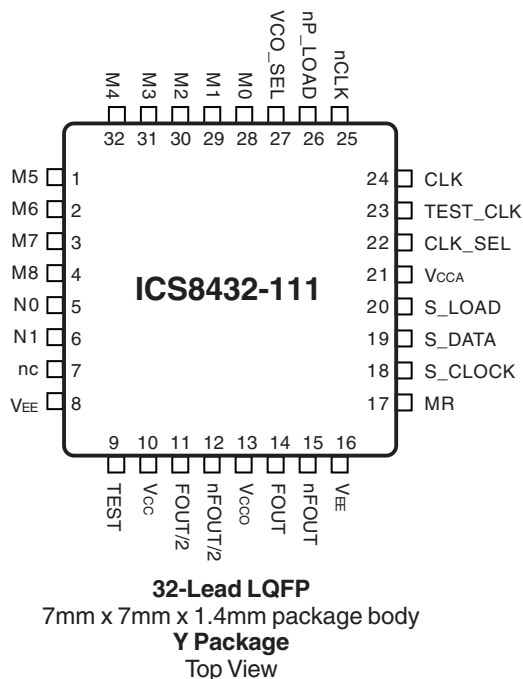


**32-Lead LQFP**
7mm x 7mm x 1.4mm package body
**Y Package**
Top View

**FUNCTIONAL DESCRIPTION**

*NOTE: The functional description that follows describes operation using a 25MHz clock input. Valid PLL loop divider values for different input frequencies are defined in the Input Frequency Characteristics, Table 5, NOTE 1.*

The ICS8432-111 features a fully integrated PLL and therefore requires no external components for setting the loop band-width. A differential clock input is used as the input to the ICS8432-111. This input is fed into the phase detector. A 25MHz clock input provides a 25MHz phase detector reference frequency. The VCO of the PLL operates over a range of 200MHz to 700MHz. The output of the loop divider is also applied to the phase detector.

The phase detector and the loop filter divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVPECL output buffers. The divider provides a 50% output duty cycle.

The programmable features of the ICS8432-111 support two input modes and programmable PLL loop divider and output divider. The two input operational modes are parallel and serial. *Figure1* shows the timing diagram for each mode. In parallel mode the nP_LOAD input is initially LOW. The data on inputs M0 through M8 and N0 and N1 is passed directly to the ripple counter. On the LOW-to-HIGH transition of the nP_LOAD input, the data is latched and the ripple counter remains loaded until the next LOW transition on nP_LOAD or until a serial event occurs. As a result, the M and N bits can be hardwired to set the ripple counter to a specific default state that will automatically occur during power-up. The TEST output is LOW when operating in the parallel input mode. The relationship between the VCO frequency, the input frequency and the loop divider is defined as follows:

$$fVCO = f_{IN} \times M$$

The M count and the required values of M0 through M8 are shown in Table 3B, Programmable VCO Frequency Function. Valid M values for which the PLL will achieve lock are defined as $8 \leq M \leq 28$. The frequency out is defined as follows:

$$fOUT = \frac{fVCO}{N} = f_{IN} \times \frac{M}{N}$$

Serial operation occurs when nP_LOAD is HIGH and S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the ripple counter when S_LOAD transitions from LOW-to-HIGH. The ripple counter divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH, data at the S_DATA input is passed directly to the ripple counter on each rising edge of S_CLOCK. The serial mode can be used to program the M and N bits and test bits T1 and T0. The internal registers T0 and T1 determine the state of the TEST output as follows:

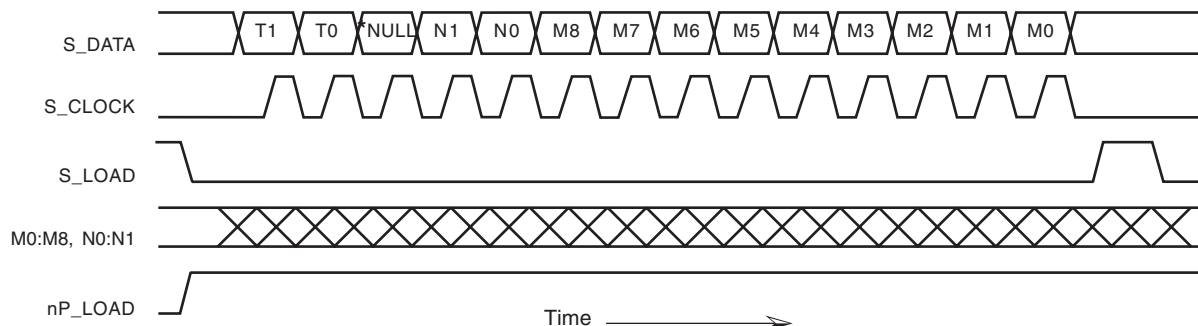| T1 | T0 | TEST Output |
|----|----|-------------|
| 0 | 0 | LOW |
| 0 | 1 | S_Data |
| 1 | 0 | Output of M divider |
| 1 | 1 | CMOS Fout/2 |



**FIGURE 1. PARALLEL & SERIAL LOAD OPERATIONS**

*NOTE: The NULL timing slot must be observed.

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### TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1 | M5 | Input | Pullup | M counter/divider inputs. Data latched on LOW-to-HIGH transistion of nP_LOAD input. LVCMOS / LVTTL interface levels. |
| 2, 3, 4, 28, 29, 30, 31, 32 | M6, M7, M8, M0, M1, M2, M3, M4 | Input | Pulldown | |
| 5, 6 | N0, N1 | Input | Pulldown | Determines output divider value as defined in Table 3C Function Table. LVCMOS / LVTTL interface levels. |
| 7 | nc | Unused | | No connect. |
| 8, 16 | $V_{EE}$ | Power | | Negative supply pins. Connect to ground. |
| 9 | TEST | Output | | Test output which is ACTIVE in the serial mode of operation. Output driven LOW in parallel mode. LVCMOS interface levels. |
| 10 | $V_{CC}$ | Power | | Positive supply pin. |
| 11, 12 | FOUT/2, nFOUT/2 | Output | | Half frequency differential output for the synthesizer. 3.3V LVPECL interface levels. |
| 13 | $V_{CCO}$ | Power | | Output supply pin. Connect to 3.3V. |
| 14, 15 | FOUT, nFOUT | Output | | Differential output for the synthesizer. 3.3V LVPECL interface levels. |
| 17 | MR | Input | Pulldown | Master reset. Forces outputs LOW, but does not effect loaded M, N, and T values. LVCMOS / LVTTL interface levels. |
| 18 | S_CLOCK | Input | Pulldown | Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. |
| 19 | S_DATA | Input | Pulldown | Shift register serial input. Data sampled on the rising edge of S_CLOCK. |
| 20 | S_LOAD | Input | Pulldown | Controls transition of data from shift register into the ripple counter. LVCMOS / LVTTL interface levels. |
| 21 | $V_{CCA}$ | Power | | Analog supply pin. Connect to 3.3V. |
| 22 | CLK_SEL | Input | Pullup | Selects between differential clock input or test input as the PLL reference source. LVCMOS / LVTTL interface levels. Selects CLK, nCLK inputs when HIGH. Selects TEST_CLK when LOW. |
| 23 | TEST_CLK | Input | Pulldown | Test clock input. LVCMOS / LVTTL interface levels. |
| 24 | CLK | Input | Pulldown | Non-inverting differential clock input. |
| 25 | nCLK | Input | Pullup | Inverting differential clock input. |
| 26 | nP_LOAD | Input | Pulldown | Parallel load input. Determines when data present at M8:M0 is loaded into ripple counter, and when data present at N1:N0 sets the output divider value. LVCMOS / LVTTL interface levels. |
| 27 | VCO_SEL | Input | Pullup | Determines whether synthesizer is in PLL or bypass mode. LVCMOS / LVTTL interface levels. |

NOTE: *Pullup* and *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

### TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | | 4 | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | KΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | KΩ |

**TABLE 3A. PARALLEL AND SERIAL MODE FUNCTION TABLE**

| MR | nP_LOAD | M | N | S_LOAD | S_CLOCK | S_DATA | Conditions |
|----|---------|---|---|--------|---------|--------|------------|
| | | Inputs | | | | | Conditions |
| H | X | X | X | X | X | X | Reset. M and N counters reset. |
| L | L | Data | Data | X | X | X | Data on M and N inputs passed directly to the ripple counter and output divider. TEST output forced LOW. |
| L | ↑ | Data | Data | L | X | X | Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs. |
| L | H | X | X | L | ↑ | Data | Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK. |
| L | H | X | X | ↑ | L | Data | Contents of the shift register are passed to the ripple counter and output divider. |
| L | H | X | X | ↓ | L | Data | Ripple counter and output divider values are latched. |
| L | H | X | X | L | X | X | Parallel or serial input do not affect shift registers. |
| L | H | X | X | H | ↑ | Data | S_DATA passed directly to ripple counter as it is clocked. |

NOTE:  L = LOW
　　　 H = HIGH
　　　 X = Don't care
　　　 ↑ = Rising edge transition
　　　 ↓ = Falling edge transition

**TABLE 3B. PROGRAMMABLE VCO FREQUENCY FUNCTION TABLE**

| VCO Frequency (MHz) | M Count | 256 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
|---------------------|---------|-----|-----|----|----|----|----|----|----|----|
| | | M8 | M7 | M6 | M5 | M4 | M3 | M2 | M1 | M0 |
| 200 | 8 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 225 | 9 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 250 | 10 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 275 | 11 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| • | • | • | • | • | • | • | • | • | • | • |
| • | • | • | • | • | • | • | • | • | • | • |
| 650 | 26 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 675 | 27 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 700 | 28 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |

NOTE 1: These M count values and the resulting frequencies correspond to differential input or TEST_CLK input frequency of 25MHz.

**TABLE 3C. PROGRAMMABLE OUTPUT DIVIDER FUNCTION TABLE**

| Inputs | | N Divider Value | Output Frequency (MHz) | | | |
|--------|--------|-----------------|-------------------------|---------|---------|---------|
| | | | FOUT | | FOUT/2 | |
| N1 | N0 | | Minimum | Maximum | Minimum | Maximum |
| 0 | 0 | 1 | 200 | 700 | 125 | 350 |
| 0 | 1 | 2 | 100 | 350 | 62.5 | 175 |
| 1 | 0 | 4 | 50 | 175 | 31.25 | 87.5 |
| 1 | 1 | 8 | 25 | 87.5 | 15.625 | 43.75 |

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## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, $V_{CCx}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{CC}$ + 0.5V |
| Outputs, $V_O$ | -0.5V to $V_{CC}$ + 0.5V |
| Package Thermal Impedance, $\theta_{JA}$ | 47.9°C/W (0 lfpm) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these condition or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,** $V_{CC} = V_{CCA} = V_{CCO} = 3.3V\pm5\%$, $T_A = 0°C$ TO 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Positive Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCA}$ | Analog Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCO}$ | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{EE}$ | Power Supply Current | | | | 110 | mA |
| $I_{CCA}$ | Analog Supply Current | | | | 15 | mA |

**TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS,** $V_{CC} = V_{CCA} = V_{CCO} = 3.3V\pm5\%$, $T_A = 0°C$ TO 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | VCO_SEL, CLK_SEL, S_LOAD, S_DATA, S_CLOCK, nP_LOAD, N0:N1, M0:M8, MR | | 2 | | $V_{CC}$ + 0.3 | V |
| | | TEST_CLK | | 2 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | VCO_SEL, CLK_SEL, S_LOAD, S_DATA, S_CLOCK, nP_LOAD, N0:N1, M0:M8, MR | | -0.3 | | 0.8 | V |
| | | TEST_CLK | | | | 1.3 | V |
| $I_{IH}$ | Input High Current | M0-M4, M6-M8, N0, N1, S_CLOCK, S_DATA, S_LOAD, TEST_CLK, nP_LOAD, MR | *$V_{CCx} = V_{IN} = 3.465V$ | | | 150 | µA |
| | | M5, CLK_SEL, VCO_SEL | *$V_{CCx} = V_{IN} = 3.465V$ | | | 5 | µA |
| $I_{IL}$ | Input Low Current | M0-M4, M6-M8, N0, N1, S_CLOCK, S_DATA, S_LOAD, TEST_CLK, nP_LOAD, MR | *$V_{CCx} = 3.465V$, $V_{IN} = 0V$ | -5 | | | µA |
| | | M5, CLK_SEL, VCO_SEL | *$V_{CCx} = 3.465V$, $V_{IN} = 0V$ | -150 | | | µA |
| $V_{OH}$ | Output High Voltage | TEST; NOTE 1 | | 2.6 | | | V |
| $V_{OL}$ | Output Low Voltage | TEST; NOTE 1 | | | | 0.5 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CCO}$/2. See page 8, Figure 2, 3.3V Output Load Test Circuit.
*NOTE: $V_{CCx}$ denotes $V_{CC}$, $V_{CCA}$, and $V_{CCO}$.

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**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,** $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | CLK | $*V_{CCx} = V_{IN} = 3.465V$ | | | 150 | μA |
| | | nCLK | $*V_{CCx} = V_{IN} = 3.465V$ | | | 5 | μA |
| $I_{IL}$ | Input Low Current | CLK | $*V_{CCx} = 3.465V, V_{IN} = 0V$ | -5 | | | μA |
| | | nCLK | $*V_{CCx} = 3.465V, V_{IN} = 0V$ | -150 | | | μA |
| $V_{PP}$ | Peak-to-Peak Input Voltage | | | 0.15 | | 1.3 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 | | | $V_{EE} + 0.5$ | | $V_{CC} - 0.85$ | V |

NOTE 1: Common mode voltage is defined as $V_{IH}$.
NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is $V_{CC} + 0.3V$.
NOTE: $*V_{CCx}$ denotes $V_{CC}$, $V_{CCA}$, and $V_{CCO}$.

**TABLE 4D. LVPECL DC CHARACTERISTICS,** $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{CCO} - 1.4$ | | $V_{CCO} - 1.0$ | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | $V_{CCO} - 2.0$ | | $V_{CCO} - 1.7$ | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.6 | | 0.85 | V |

NOTE 1:  Outputs terminated with 50 Ω to $V_{CCO}$ - 2V.

**TABLE 5. INPUT FREQUENCY CHARACTERISTICS,** $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{IN}$ | Input Frequency | TEST_CLK; NOTE 1 | | 12 | | 25 | MHz |
| | | CLK, nCLK; NOTE 1 | | 12 | | 25 | MHz |
| | | S_CLOCK | | | | 50 | MHz |

NOTE 1: For the input frequency range, the M value must be set for the VCO to operate within the 200MHz to 700MHz range. Using the minimum input frequency of 12MHz, valid values of M are $17 \leq M \leq 58$. Using the maximum frequency of 25MHz, valid values of M are $8 \leq M \leq 28$.

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**TABLE 6. AC CHARACTERISTICS,** $V_{CC} = V_{CCA} = V_{CCO} = 3.3V\pm5\%$, $T_A = 0°C$ TO $70°C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $F_{OUT}$ | Output Frequency | | | 25 | | 700 | MHz |
| $t$jit(cc) | Cycle-to-Cycle Jitter; NOTE 2 | | | | | 25 | ps |
| $t$jit(per) | Period Jitter, RMS; NOTE 2 | | | | | TBD | ps |
| $t$sk(o) | Output Skew; NOTE 1, 2 | | | | | 10 | ps |
| $t_R$ | Output Rise Time | | 20% to 80% @ 50MHz | 300 | | 700 | ps |
| $t_F$ | Output Fall Time | | 20% to 80% @ 50MHz | 300 | | 700 | ps |
| $t_S$ | Setup Time | M, N to nP_LOAD | | | | 5 | ns |
| | | S_DATA to S_CLOCK | | | | 5 | ns |
| | | S_CLOCK to S_LOAD | | | | 5 | ns |
| $t_H$ | Hold Time | M, N to nP_LOAD | | | | 5 | ns |
| | | S_DATA to S_CLOCK | | | | 5 | ns |
| | | S_CLOCK to S_LOAD | | | | 5 | ns |
| odc | Output Duty Cycle | | | 47 | | 53 | % |
| $t_{LOCK}$ | PLL Lock Time | | | | | 10 | ms |

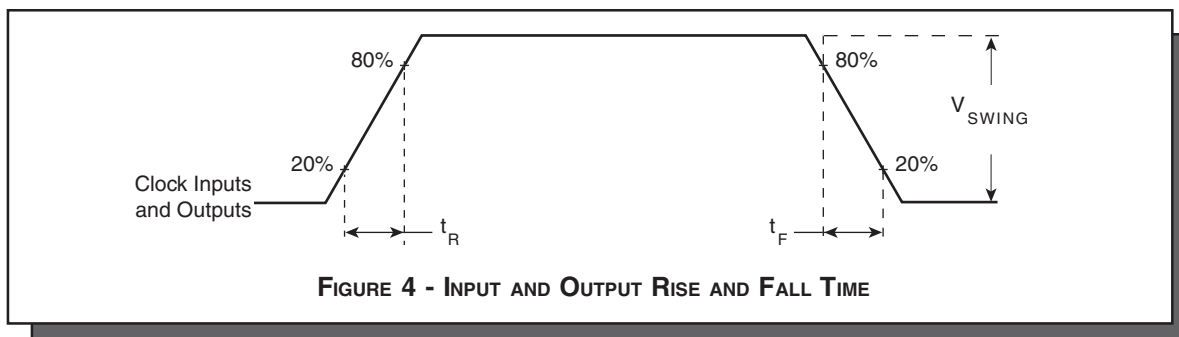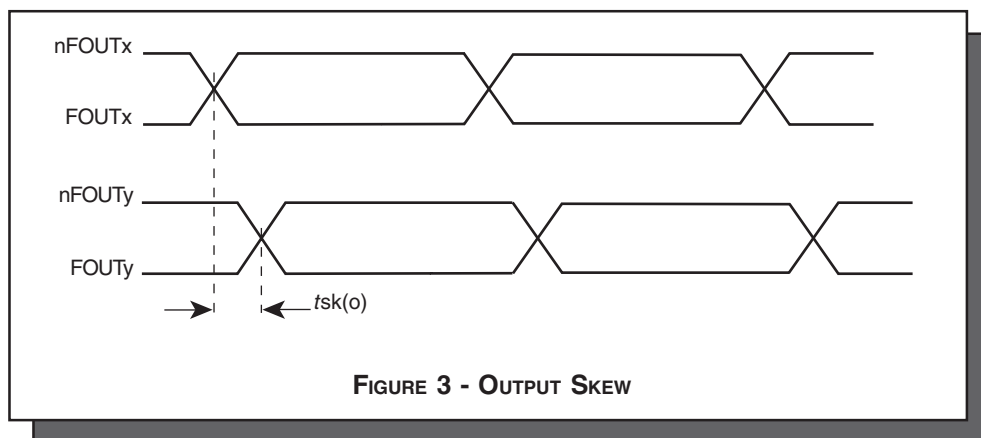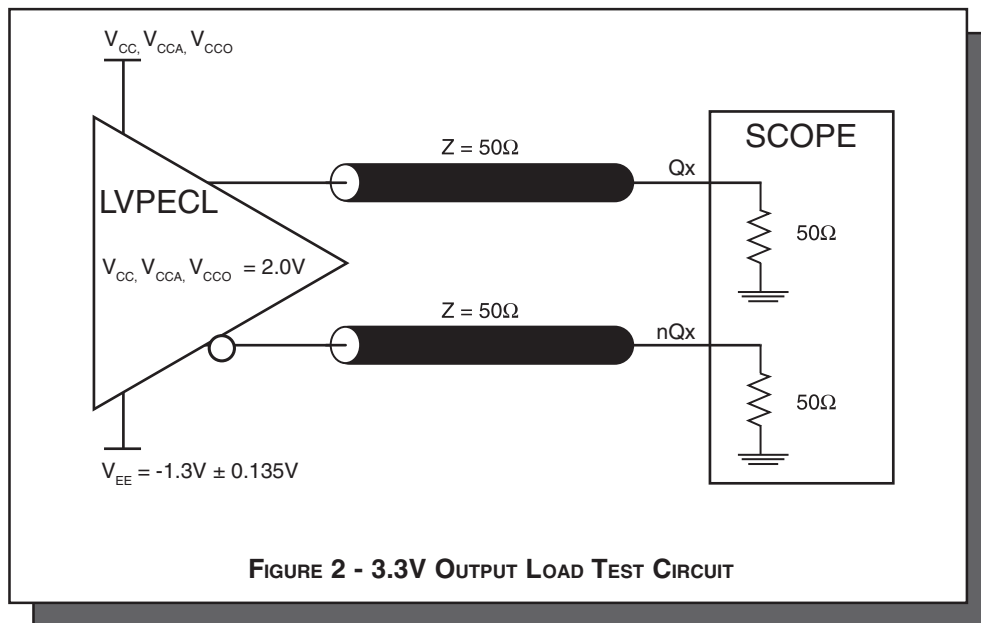All parameters measured at 500MHz unless noted otherwise.
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

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## PARAMETER MEASUREMENT INFORMATION

$V_{CC}, V_{CCA}, V_{CCO}$

SCOPE

$Z = 50\Omega$

Qx

LVPECL

$V_{CC}, V_{CCA}, V_{CCO} = 2.0V$

$50\Omega$

$Z = 50\Omega$

nQx

$50\Omega$

$V_{EE} = -1.3V \pm 0.135V$

**FIGURE 2 - 3.3V OUTPUT LOAD TEST CIRCUIT**

nFOUTx

FOUTx

nFOUTy

FOUTy

$t$sk(o)

**FIGURE 3 - OUTPUT SKEW**

80%          80%

$V_{SWING}$

20%          20%

Clock Inputs
and Outputs

$t_R$          $t_F$

**FIGURE 4 - INPUT AND OUTPUT RISE AND FALL TIME**

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nFOUT, n FOUT/2

TEST, FOUT, FOUT/2

Pulse Width

$t_{PERIOD}$

$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

**FIGURE 5 - odc & $t_{PERIOD}$**

IDEAL OUTPUT

$\frac{1}{fo}$

ACTUAL OUTPUT

$t$cycle n

$$t\text{jit(per)} = \left| t_{cycle\ n} - \frac{1}{fo} \right|$$ where fo is the nominal output frequency and $t_{cycle\ n}$ is any cycle within the sample measured on controlled edges

**FIGURE 6 - Period Jitter**

nFOUT, n FOUT/2

FOUT, FOUT/2

$t$cycle n

$t$cycle n+1

$$t\text{jit(cc)} = t\text{cycle n} - t\text{cycle n+1}$$
1000 Cycles

**FIGURE 7 - Cycle-to-Cycle Jitter**

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## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

*Figure 8* shows how the differential input can be wired to accept single ended levels. The reference voltage $V\_REF \sim V_{CC}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{CC} = 3.3V$, V_REF should be 1.25V and R2/R1 = 0.609.



**FIGURE 8 - SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT**
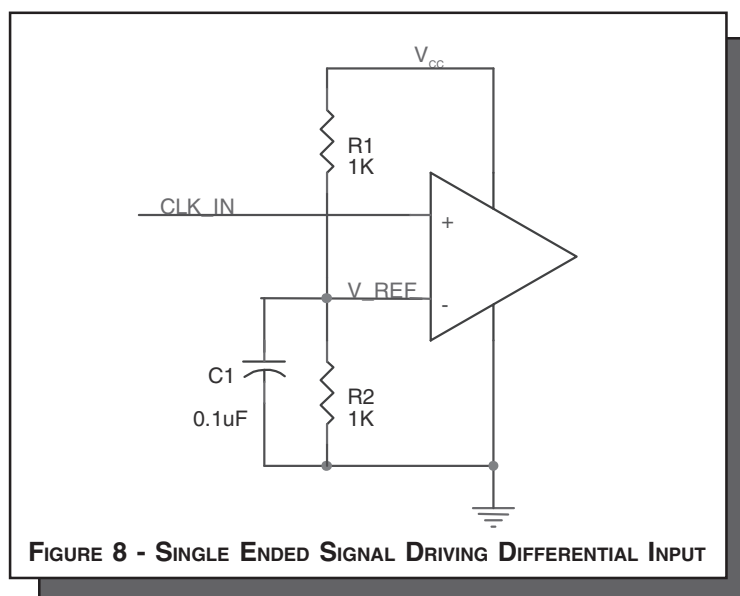
### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8432-111 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. $V_{CC}$, $V_{CCA}$, and $V_{CCO}$ should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 9* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each $V_{CCA}$ pin.
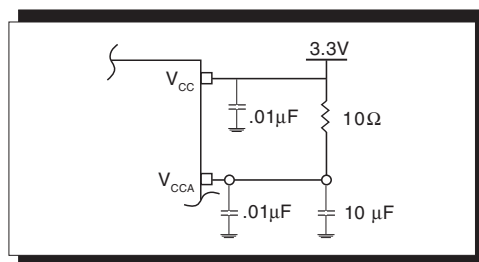


**FIGURE 9. POWER SUPPLY FILTERING**

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## TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. There are a few simple termination schemes. *Figures 10A and 10B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.
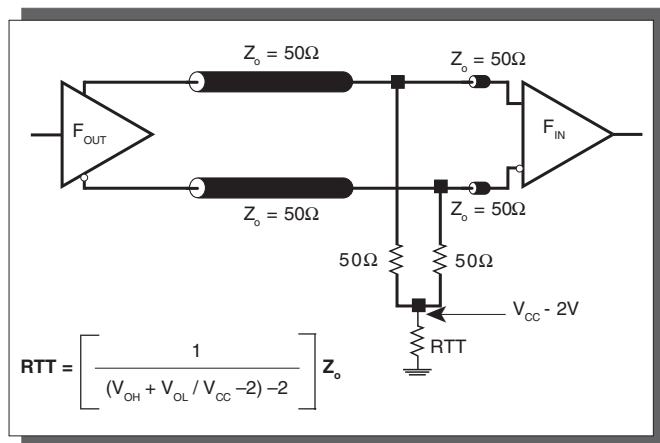


$$RTT = \left[ \frac{1}{(V_{OH} + V_{OL} / V_{CC} - 2) - 2} \right] Z_o$$

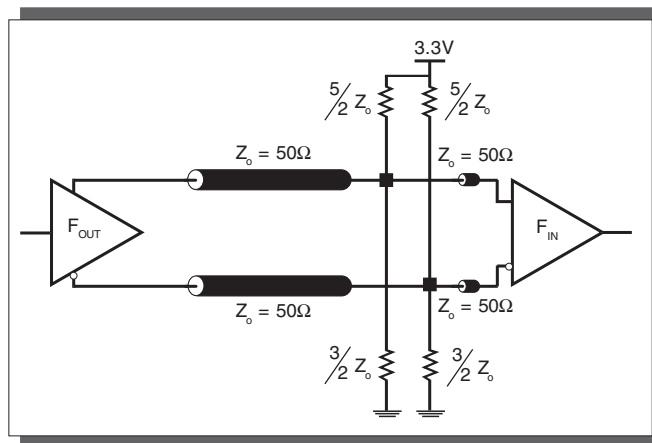**FIGURE 10A. LVPECL OUTPUT TERMINATION**



**FIGURE 10B. LVPECL OUTPUT TERMINATION**

## LAYOUT GUIDELINE

The schematic of the ICS8432-111 layout example used in this layout guideline is shown in *Figure 11A.* The ICS8432-111 recommended PCB board layout for this example is shown in *Figure 11B.* This layout example is used as a general guideline. The layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stacking of the P.C. board.

**FIGURE 11A. SCHEMATIC OF RECOMMENDED LAYOUT**

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The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.

### POWER AND GROUNDING

Place the decoupling capacitors C1, C6, C2, C4, and C5, as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the $V_{CCA}$ pin as possible.

### CLOCK TRACES AND TERMINATION

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signals traces.

- The differential 50Ω output traces should have same length.

- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.

- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.

- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a spearation of at least three trace widths between the differential clock trace and the other signal trace.

- Make sure no other signal traces are routed between the clock trace pair.

- The matching termination resistors should be located as close to the receiver input pins as possible.

FIGURE 11B. PCB BOARD LAYOUT FOR ICS8432-111

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## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8432-111. Equations and example calculations are also provided.

*1. Power Dissipation.*
The total power dissipation for the ICS8432-111 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC}$ = 3.3V + 5% = 3.465V, which gives worst case results.
**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 110mA = **381.2mW**

- Power $(outputs)_{MAX}$ = **30.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30.2mW = **60.4mW**

  **Total Power $_{MAX}$** (3.465V, with all outputs switching) = 381.2mW + 60.4mW = **441.6mW**

*2. Junction Temperature.*
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

$Tj$ = Junction Temperature

$\theta_{JA}$ = junction-to-ambient thermal resistance

$Pd\_total$ = Total device power dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.441W * 42.1°C/W = 88.6°C. This is well below the limit of 125°C

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**Table 7. Thermal Resistance $\theta_{JA}$ for 32-pin LQFP, Forced Convection**

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) | | |
|---|---|---|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 47.9°C/W | 42.1°C/W | 39.4°C/W |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

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*3. Calculations and Equations.*

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 12.*



**FIGURE 12 - LVPECL DRIVER CIRCUIT AND TERMINATION**
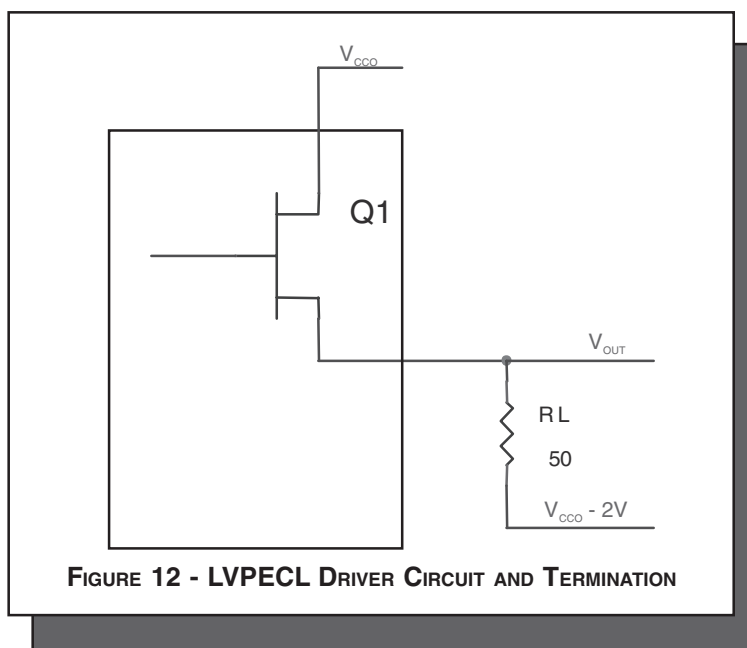
To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO}$ - 2V.

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX})$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX})$$

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 1.0V}$

    Using $V_{CCO\_MAX} = 3.465$, this results in $V_{OH\_MAX} = \mathbf{2.465V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

    Using $V_{CCO\_MAX} = 3.465$, this results in $V_{OL\_MAX} = \mathbf{1.765V}$

Pd_H =[(2.465V - (3.465V - 2V))/50Ω] * (3.465V - 2.465V) = **20mW**
Pd_L =[(1.765V - (3.465V - 2V))/50Ω] * (3.465V - 1.765V) = **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.2mW**

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# RELIABILITY INFORMATION

TABLE 8. $\theta_{JA}$ VS. AIR FLOW TABLE

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) | | | |
|---|---|---|---|
| | **0** | **200** | **500** |
| Single-Layer PCB, JEDEC Standard Test Boards | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 47.9°C/W | 42.1°C/W | 39.4°C/W |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8432-111 is: 3765

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**PACKAGE OUTLINE - Y SUFFIX**
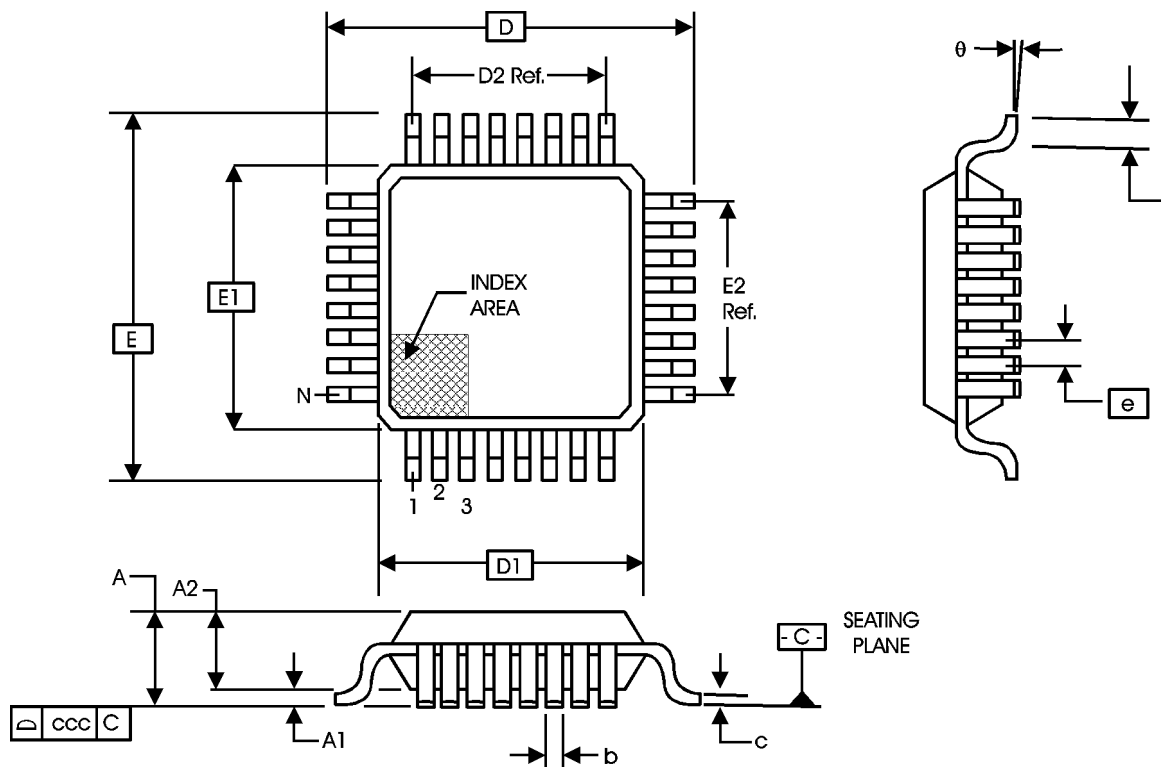


**TABLE 9. PACKAGE DIMENSIONS**

| SYMBOL | JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS | | |
|---|---|---|---|
| | BBA | | |
| | MINIMUM | NOMINAL | MAXIMUM |
| N | 32 | | |
| A | -- | -- | 1.60 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.30 | 0.37 | 0.45 |
| c | 0.09 | -- | 0.20 |
| D | 9.00 BASIC | | |
| D1 | 7.00 BASIC | | |
| D2 | 5.60 Ref. | | |
| E | 9.00 BASIC | | |
| E1 | 7.00 BASIC | | |
| E2 | 5.60 Ref. | | |
| e | 0.80 BASIC | | |
| L | 0.45 | 0.60 | 0.75 |
| θ | 0° | -- | 7° |
| ccc | -- | -- | 0.10 |

Reference Document: JEDEC Publication 95, MS-026

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### TABLE 10. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Count | Temperature |
|---|---|---|---|---|
| ICS8432CY-111 | ICS8432CY-111 | 32 Lead LQFP | 250 per tray | 0°C to 70°C |
| ICS8432CY-111T | ICS8432CY-111 | 32 Lead LQFP on Tape and Reel | 1000 | 0°C to 70°C |