



GENERAL DESCRIPTION

The ICS8431-01 is a general purpose clock frequency synthesizer for IA64/32 applications and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8431-01 consists of one independent low bandwidth PLL timing channel. A 16.666MHz crystal is used as the input to the on-chip oscillator. The M divide is configured to produce a fixed output frequency of 200MHz.

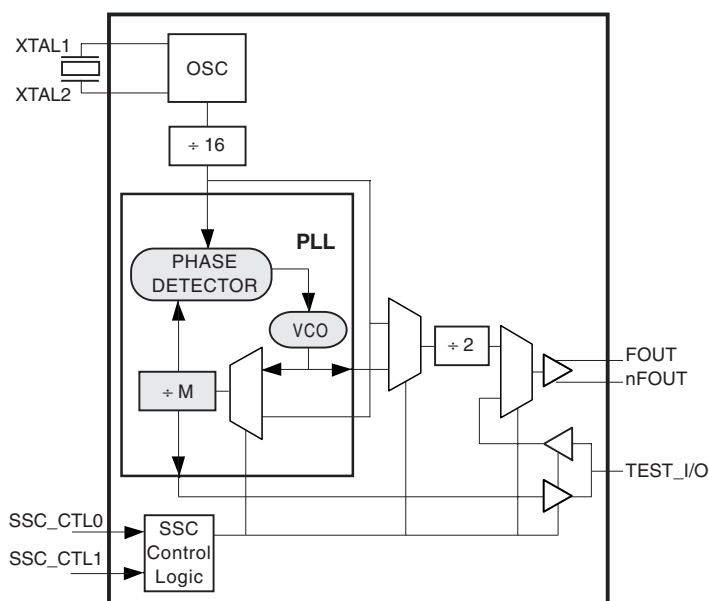
Programmable features of the ICS8431-01 support four operational modes. The four modes are spread spectrum clocking (SSC), non-spread spectrum clocking and two test modes which are controlled by the SSC_CTL[1:0] pins. Unlike other synthesizers, the ICS8431-01 can immediately change spread-spectrum operation without having to reset the device.

In SSC mode, the output clock is modulated in order to achieve a reduction in EMI. In one of the PLL bypass test modes, the PLL is disconnected as the source to the differential output allowing an external source to be connected to the TEST_I/O pin. This is useful for in-circuit testing and allows the differential output to be driven at a lower frequency throughout the system clock tree. In the other PLL bypass mode, the oscillator divider is used as the source to both the M divide and the Fout divide by 2. This is useful for characterizing the oscillator and internal dividers.

FEATURES

- Fully integrated PLL
- Differential 3.3V LVPECL output
- Crystal oscillator interface
- Output frequency of 200MHz
- 48% to 52% duty cycle
- Spread Spectrum Clocking (SSC) fixed at $1/2\%$ modulation for environments requiring ultra low EMI. Typical 10dB EMI reduction can be achieved with spread spectrum modulation
- PLL bypass modes supporting in-circuit testing and on-chip functional block characterization
- Cycle-to-cycle jitter: 30ps (maximum)
- 3.3V supply voltage
- 0° to 85°C Ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT

nc	1	28	nc
nc	2	27	Vcc
nc	3	26	XTAL2
nc	4	25	XTAL1
nc	5	24	nc
nc	6	23	nc
nc	7	22	VCCA
nc	8	21	VEE
nc	9	20	RESERVED
SSC_CTL0	10	19	nc
SSC_CTL1	11	18	VCCO
VEE	12	17	FOUT
TEST_I/O	13	16	nFOUT
Vcc	14	15	VEE

ICS8431-01 28-Lead SOIC

7.5mm x 18.05mm x 2.25mm
M Package
Top View



TABLE 1. PIN DESCRIPTIONS

Number	Name	Type	Description
1-9, 19, 23, 24, 28	nc	Unused	No connect.
10, 11	SSC_CTL0, SSC_CTL1	Input Pullup	SSC control pins. LVTTTL/LVCMOS interface levels.
12, 15, 21	V _{EE}	Power	Negative supply pins. Connect to ground.
13	TEST_ I/O	Input / Output	Programmed as defined in Table 3 Function Table.
14, 27	V _{CC}	Power	Positive supply pins. Connect to 3.3V
16, 17	nFOUT, FOUT	Output	Differential output for the synthesizer. Compatible with terminated positive reference LVPECL logic.
18	V _{CCO}	Power	Output supply pin. Connect to 3.3V.
20	RESERVED	Reserve	Reserve pin.
22	V _{CCA}	Power	Analog supply pin. Connect to 3.3V.
25, 26	XTAL1, XTAL2	Input	Crystal oscillator inputs.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

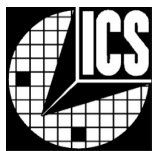
TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Pin Capacitance				4	pF
R _{PULLUP}	Input Pullup Resistor			51		KΩ
R _{PULLDOWN}	Input Pulldown Resistor			51		KΩ

TABLE 3. SSC CONTROL INPUTS FUNCTION TABLE

Inputs		TEST_I/O Source	SSC	Outputs		Operational Modes
SSC_CTL1	SSC_CTL0			FOUT, nFOUT	TEST_I/O	
0	0	Internal	Disabled	fXTAL ÷ 32	fXTAL ÷ 16 ÷ M	PLL bypass; oscillator, M and N dividers test mode. NOTE 1
0	1	PLL	Enabled	200MHz	Hi-Z	Default SSC; Modulation Factor = ½ Percent
1	0	External	Disabled	Test Clk	Input	Diagnostic Mode; NOTE 1 (1MHz ≤ Test Clk ≤ 200MHz)
1	1	PLL	Disabled	200MHz	Hi-Z	No SSC Modulation

NOTE 1: Used for in house debug and characterization.



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CCx}	4.6V
Inputs, V_I	-0.5V to $V_{CC} + 0.5V$
Outputs, V_O	-0.5V to $V_{CCO} + 0.5V$
Package Thermal Impedance, θ_{JA}	39.7°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				140	mA

TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	SSC_CTL0, SSC_CTL1, TEST_IO $V_{CC} = V_{IN} = 3.465V$			5	μA
I_{IL}	Input Low Current	SSC_CTL0, SSC_CTL1, TEST_IO $V_{CC} = V_{IN} = 3.465V$	-150			μA

TABLE 4C. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CCO} - 1.4$		$V_{CCO} - 1.0$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		600	700	850	mV

NOTE 1: Output terminated with 50 Ω to $V_{CCO} - 2V$.



TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			16.666		MHz
Equivalent Series Resistance (ESR)				70	Ω
Shunt Capacitance		3		7	pF
Series Pin Inductance		3		7	nH

TABLE 6. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
t_{PERIOD}	Average Output Period; NOTE 2	$F_{\text{OUT}} = 200\text{MHz}$	4995		5005	ps
$t_{\text{jitter(cc)}}$	Cycle-to-Cycle Jitter; NOTE 2, 3	$F_{\text{OUT}} = 200\text{MHz}$		18	30	ps
odc	Output Duty Cycle; NOTE 2	$F_{\text{OUT}} = 200\text{MHz}$	48		52	%
t_R	Output Rise Time; NOTE 1, 2	20% to 80%	300	450	600	ps
t_F	Output Fall Time; NOTE 1, 2	20% to 80%	300	450	600	ps
F_{xtal}	Crystal Input Range		14	16.666	18	MHz
Fm	SSC Modulation Frequency; NOTE 1, 2		30		33.33	KHz
Fmf	SSC Modulation Factor; NOTE 1, 2			0.4	0.6	%
SS_{Cred}	Spectral Reduction; NOTE 1, 2		7	10		dB
t_{STABLE}	Power-up to Stable Clock Output				10	ms

NOTE 1: Spread Spectrum clocking enabled.

NOTE 2: Outputs terminated with 50Ω to $V_{CCO} - 2V$.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.



PARAMETER MEASUREMENT INFORMATION

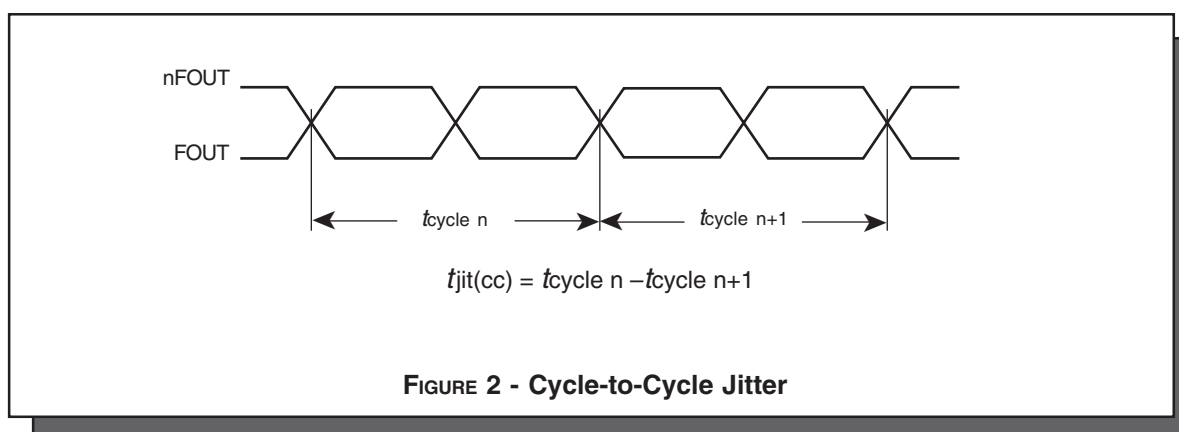
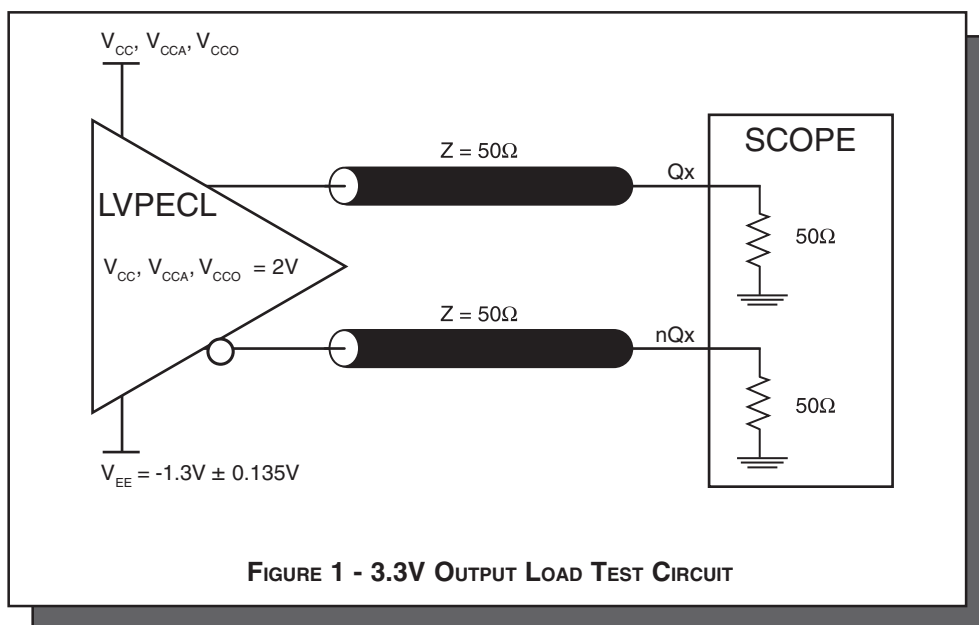




FIGURE 3 - INPUT AND OUTPUT RISE AND FALL TIME

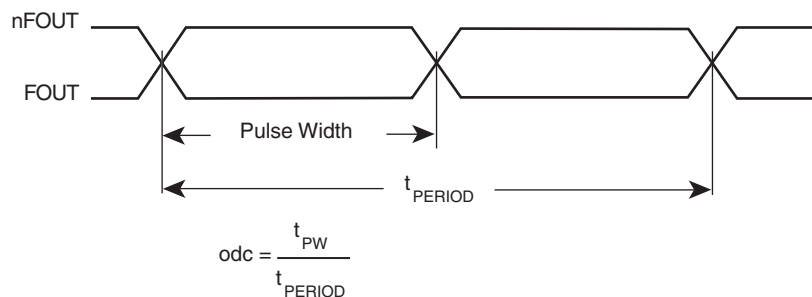


FIGURE 4 - odc & t_{PERIOD}

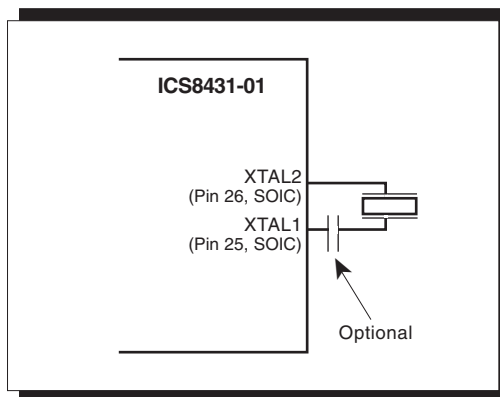


APPLICATIONS

CRYSTAL INPUT AND OSCILLATOR INTERFACE

The ICS8431-01 features an internal oscillator that uses an external quartz crystal as the source of its reference frequency. A 16.666MHz crystal divided by 16 before being sent to the phase detector provides the reference frequency. The oscillator is a series resonant, multi-vibrator type design. This design provides better stability and eliminates the need for large on chip capacitors. Though a series resonant crystal is preferred, a parallel resonant crystal can be used. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified. A few hundred ppm translates to KHz inaccuracy. In general computing applications this level of inaccuracy is irrelevant. If better ppm accuracy is required, an external capacitor can be added to a parallel resonant crystal in series to pin 25. *Figure 5A* shows how to interface with a crystal.

Figures 5A, 5B, and 5C show various crystal parameters which are recommended only as guidelines. *Figure 5A* shows how to interface a capacitor with a parallel resonant crystal. *Figure 5B* shows the capacitor value needed for the optimum ppm performance over various parallel resonant crystals. *Figure 5C* shows the recommended tuning capacitance for a 16.666MHz parallel resonant crystals.



Quartz Crystal Selection:

- (1) Raltron Series Resonant: AS-16.66-S-SMD-T-MI
- (2) Raltron Parallel Resonant: AS-16.66-18-SMD-T-MI

FIGURE 5A - CRYSTAL INTERFACE

FIGURE 5B. Recommended tuning capacitance for various parallel resonant crystals.

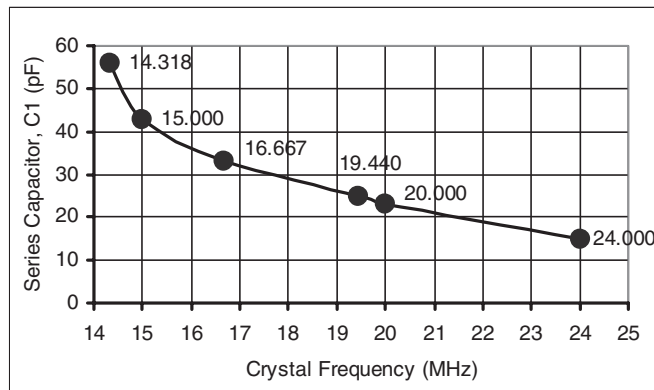
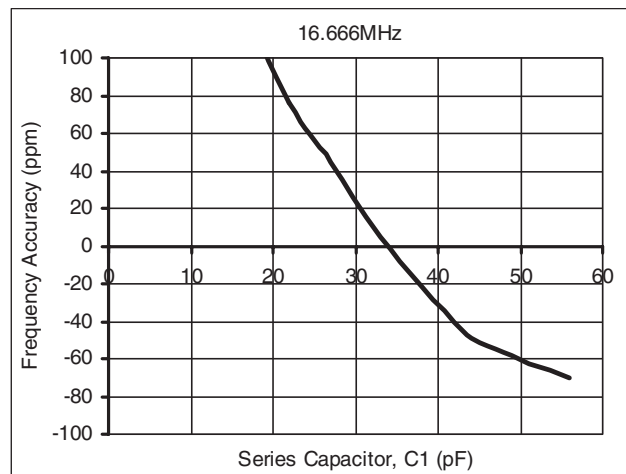


FIGURE 5C. Recommended tuning capacitance for 16.666MHz parallel resonant crystal.





SPREAD SPECTRUM

Spread-spectrum clocking is a frequency modulation technique for EMI reduction. When spread-spectrum is enabled, a 30KHz triangle waveform is used with 0.5% down-spread (+0.0%/-0.5%) from the nominal 200MHz clock frequency. An example of a triangle frequency modulation profile is shown in Figure 2 below. The ramp profile can be expressed as:

- F_{nom} = Nominal Clock Frequency in Spread OFF mode (200MHz with 16.666MHz IN)
- F_m = Nominal Modulation Frequency (30KHz)
- δ = Modulation Factor (0.5% down spread)

$$(1 - \delta) F_{nom} + 2 F_m \times \delta \times F_{nom} \times t \text{ when } 0 < t < \frac{1}{2 F_m},$$

$$(1 - \delta) F_{nom} - 2 F_m \times \delta \times F_{nom} \times t \text{ when } \frac{1}{2 F_m} < t < \frac{1}{F_m}$$

The ICS8431-01 triangle modulation frequency deviation will not exceed 0.6% down-spread from the nominal clock frequency (+0.0%/-0.5%). An example of the amount of down spread relative to the nominal clock frequency can be seen in the frequency domain, as shown in Figure 6A. The ratio of this width to the fundamental frequency is typically 0.4%, and will not exceed 0.6%. The resulting spectral reduction will be greater than 7dB, as shown in Figure 6B. It is important to note the ICS8431-01 7dB minimum spectral reduction is the component-specific EMI reduction, and will not necessarily be the same as the system EMI reduction.

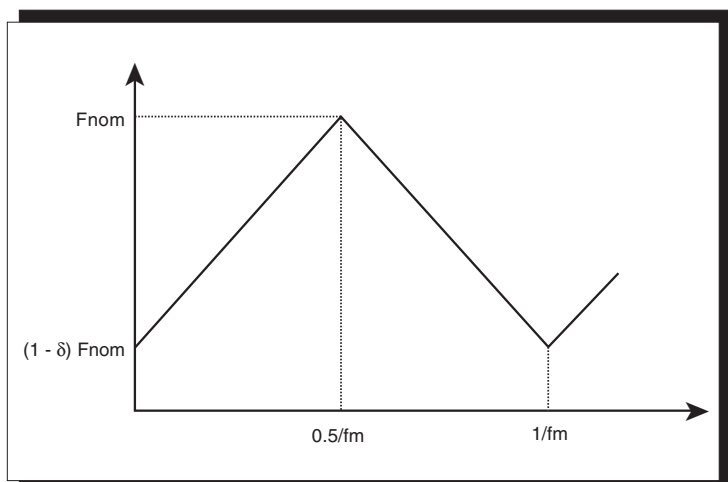


FIGURE 6A - TRIANGLE FREQUENCY MODULATION

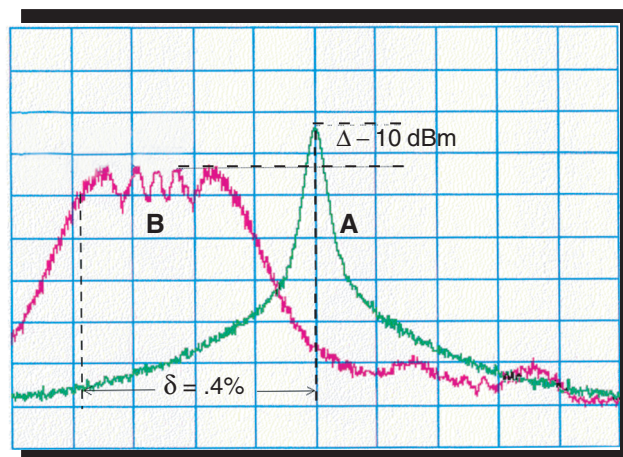


FIGURE 6B - 200MHz CLOCK OUTPUT IN FREQUENCY DOMAIN
(A) SPREAD-SPECTRUM OFF
(B) SPREAD-SPECTRUM ON

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8431-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} , V_{CCA} , and V_{CCO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, better power supply isolation is required. Figure 7 illustrates how a 10Ω along with a 10μF and a .01μF bypass capacitor should be connected to each V_{CCA} pin.

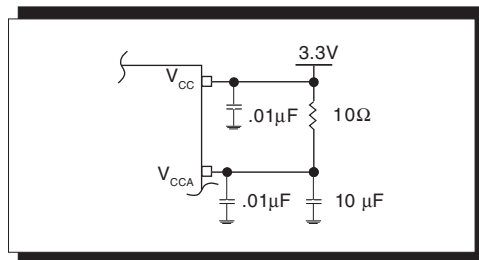


FIGURE 7 - POWER SUPPLY FILTERING



TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is typical for IA64/32 platforms. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to

drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. There are a few simple termination schemes. *Figures 8A and 8B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

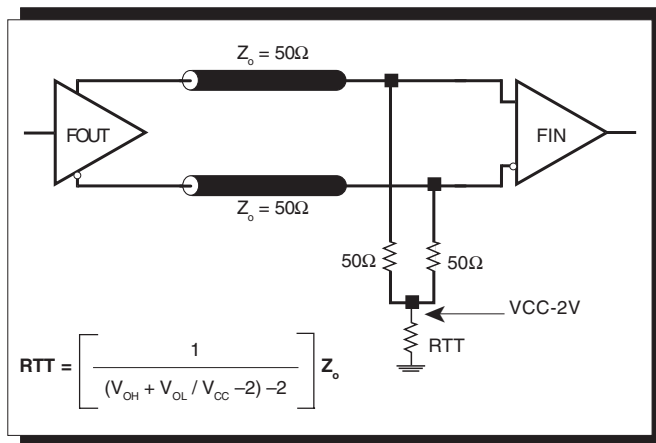


FIGURE 8A - LVPECL OUTPUT TERMINATION

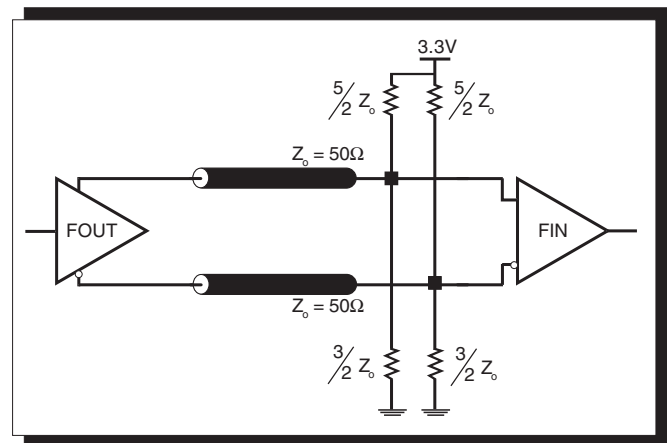


FIGURE 8B - LVPECL OUTPUT TERMINATION

LAYOUT GUIDELINE

The schematic of the ICS8431-01 layout example used in this layout guideline is shown in *Figure 9A*. The ICS8431-01 recommended PCB board layout for this example is shown in *Figure 9B*. This layout example is used as a general guideline. The layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stacking of the P.C. board.

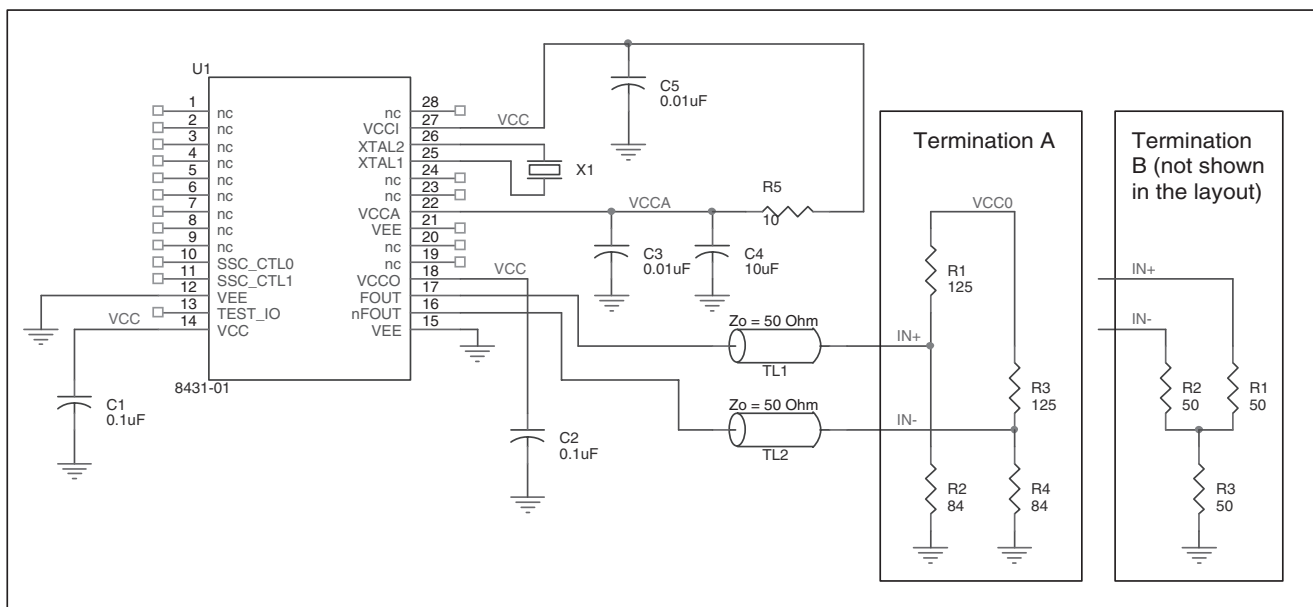


FIGURE 9A - RECOMMENDED SCHEMATIC LAYOUT



The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.
The Crystal X1 is Raltron Part # AS-16.666-18-SMD.

POWER AND GROUNDING

Place the decoupling capacitors C1, C2, C3, C4, and C5, as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin generated by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R5, C3, and C4 should be placed as close to the V_{CCA} pin as possible.

CLOCK TRACES AND TERMINATION

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The matching termination resistors should be located as close to the receiver input pins as possible.

The matching termination resistors R1, R2, R3 and R4 should be located as close to the receiver input pins as possible. Other termination scheme can also be used but is not shown in the example.

CRYSTAL

The crystal X1 should be located as close as possible to the pins 25 (XTAL1) and 26 (XTAL2). The trace length between the X1 and U1 should be kept to a minimum to avoid unwanted parasitic inductance and capacitance. Other signal traces should not be routed near the crystal traces.

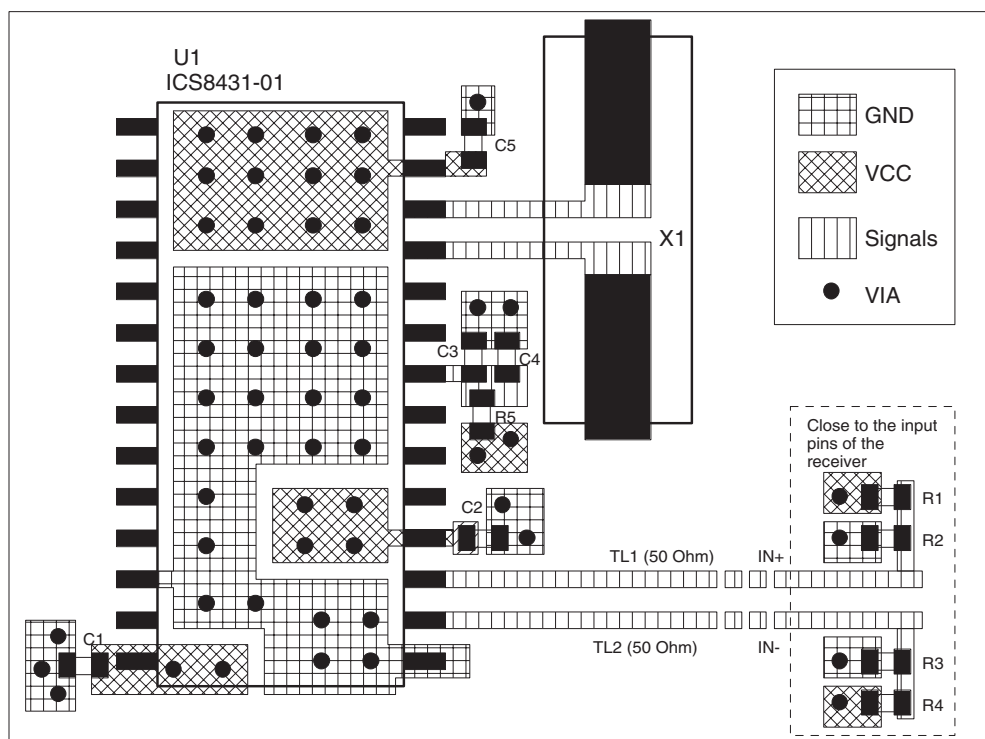
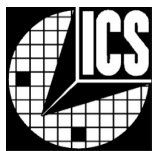


FIGURE 9B - PCB BOARD LAYOUT FOR ICS8431-01



POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8431-01. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8431-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.465V * 140mA = 485.1mW$
- Power (outputs)_{MAX} = **30.2mW/Loaded Output pair**
If all outputs are loaded, the total power is $1 * 30.2mW = 30.2mW$

Total Power_{MAX} (3.465V, with all outputs switching) = $485.1mW + 30.2mW = 515.3mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 39.7°C/W per Table 7 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:
 $85^\circ C + 0.515W * 39.7^\circ C/W = 105.4^\circ C$. This is well below the limit of 125°C

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 7. THERMAL RESISTANCE θ_{JA} FOR 28-PIN SOIC, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	76.2°C/W	60.8°C/W	53.2°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			



3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in Figure 10.

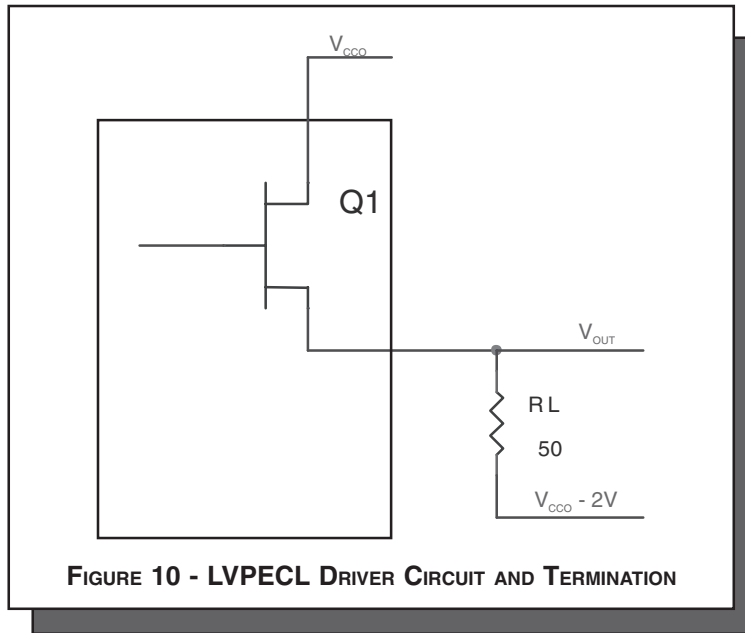


FIGURE 10 - LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CCO_MAX} - 1.0V$

$$(V_{CCO_MAX} - V_{OH_MAX}) = 1.0V$$

- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CCO_MAX} - 1.7V$

$$(V_{CCO_MAX} - V_{OL_MAX}) = 1.7V$$

Pd_H is power dissipation when the output drives high.
 Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - (V_{CCO_MAX} - V_{OH_MAX}))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - 1V)/50\Omega] * 1V = 20.0mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - (V_{CCO_MAX} - V_{OL_MAX}))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

Total Power Dissipation per output pair = $Pd_H + Pd_L = 30.2mW$



RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	76.2°C/W	60.8°C/W	53.2°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

TRANSISTOR COUNT

The transistor count for ICS8431-01 is: 5323



PACKAGE OUTLINE - M SUFFIX

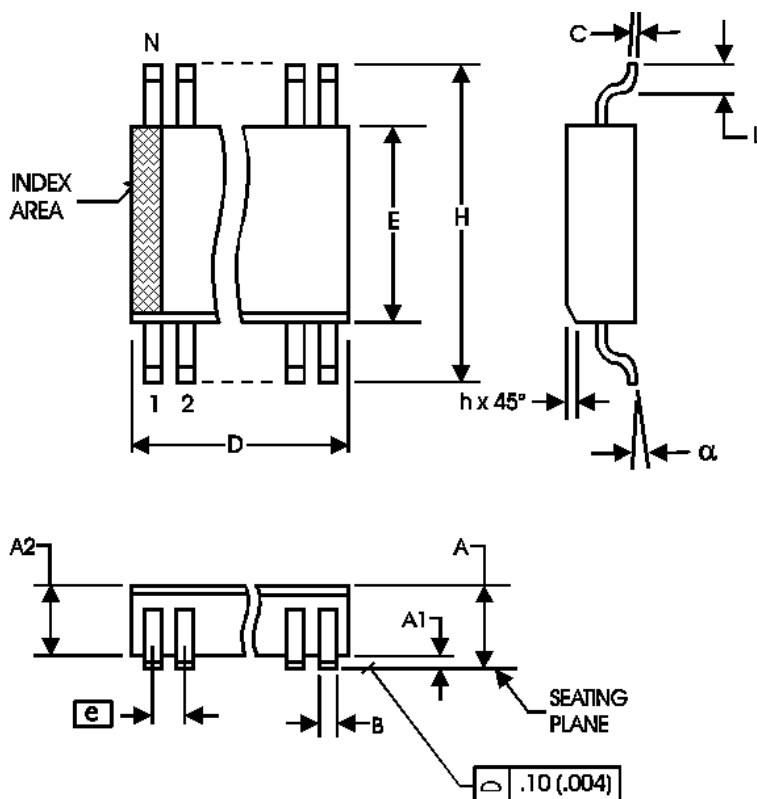


TABLE 9. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MINIMUM	MAXIMUM
N	28	
A	--	2.65
A1	0.10	--
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	17.70	18.40
E	7.40	7.60
e	1.27 BASIC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	8°

REFERENCE DOCUMENT: JEDEC PUBLICATION 95, MS-013, MO-119



Integrated
Circuit
Systems, Inc.

ICS8431-01

200MHz, LOW JITTER,
CRYSTAL OSCILLATOR-TO-3.3V LVPECL FREQUENCY SYNTHESIZER

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8431CM-01	ICS8431CM-01	28 Lead SOIC	26 Per Tube	0°C to 85°C
ICS8431CM-01T	ICS8431CM-01	28 Lead SOIC on Tape and Reel	1000	0°C to 85°C

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Integrated
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ICS8431-01

200MHz, LOW JITTER, CRYSTAL OSCILLATOR-TO-3.3V LVPECL FREQUENCY SYNTHESIZER

REVISION HISTORY SHEET

Rev	Table	Page	Description of Change	Date
B	6	4 9	Updated tjit(cc) row from 13ps Typical to 18ps Typical; 25ps Max. to 30ps Max. Updated Figures 8A and 8B, LVPECL Output Termination.	12/7/01
B	5	4	Crystal Characteristics table, ESR row value updated from 50Ω Max. to 70Ω Max.	1/10/02