PRELIMINARY

Integrated Circuit Systems, Inc.

ICS85210-21

LOW SKEW, DUAL, 1-TO-5 DIFFERENTIAL-TO-LVHSTL FANOUT BUFFER

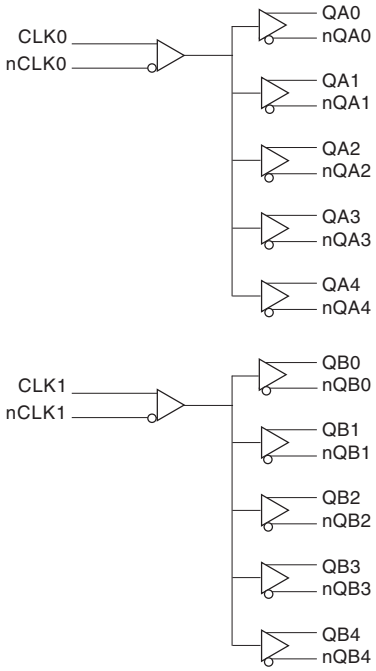
GENERAL DESCRIPTION

The ICS85210-21 is a low skew, high performance dual 1-to-5 Differential-to-LVHSTL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The CLKx, nCLKx pairs can accept most standard differential input levels. The ICS85210-21 is characterized to operate from a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the ICS85210-21 ideal for those clock distribution applications demanding well defined performance and repeatability.

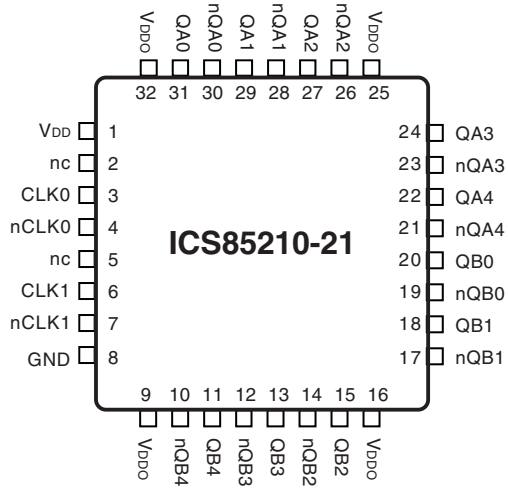
FEATURES

- Dual 1-5 LVHSTL bank outputs
- 2 selectable differential clock input pairs
- CLKx, nCLKx pairs can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: 650MHz
- Translates any single ended input signal to 3.3V LVHSTL levels with resistor bias on nCLKx input
- Output skew: 30ps (typical)
- Part-to-part skew: TBD
- Propagation delay: 1.8ns (typical)
- 3.3V core, 1.8V output operating supply
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{DD}	Power		Positive supply pin.
2, 5	nc	Unused		No connect.
3	CLK0	Input	Pulldown	Non-inverting differential clock input.
4	nCLK0	Input	Pullup	Inverting differential clock input.
6	CLK1	Input	Pulldown	Non-inverting differential clock input.
7	nCLK1	Input	Pullup	Inverting differential clock input.
8	GND	Power		Power supply ground.
9, 16, 25, 32	V_{DDO}	Power		Output supply pins.
10, 11	nQB4, QB4	Output		Differential output pair. LVHSTL interface levels.
12, 13	nQB3, QB3	Output		Differential output pair. LVHSTL interface levels.
14, 15	nQB2, QB2	Output		Differential output pair. LVHSTL interface levels.
17, 18	nQB1, QB1	Output		Differential output pair. LVHSTL interface levels.
19, 20	nQB0, QB0	Output		Differential output pair. LVHSTL interface levels.
21, 22	nQA4, QA4	Output		Differential output pair. LVHSTL interface levels.
23, 24	nQA3, QA3	Output		Differential output pair. LVHSTL interface levels.
26, 27	nQA2, QA2	Output		Differential output pair. LVHSTL interface levels.
28, 29	nQA1, QA1	Output		Differential output pair. LVHSTL interface levels.
30, 31	nQA0, QA0	Output		Differential output pair. LVHSTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DDx}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±0.2V, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Input Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Power Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current			90		mA
I_{DDO}	Output Supply Current			300		mA

TABLE 3B. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±0.2V, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK0, nCLK1	$V_{DD} = V_{IN}$ = 3.465V			5	µA
		CLK0, CLK1	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	nCLK0, nCLK1	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		CLK0, CLK1	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			0.5		V_{DD} - 0.85	V

NOTE 1: For single ended applications the maximum input voltage for CLKx and nCLKx is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 3C. LVHSTL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±0.2V, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		1		1.2	V
V_{OL}	Output Low Voltage; NOTE 1		0		0.4	V
V_{OX}	Output Crossover Voltage		40% x (V_{OH} - V_{OL}) + V_{OL}		60% x (V_{OH} - V_{OL}) + V_{OL}	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.1	V

NOTE 1: Outputs terminated with 50Ω to ground.

TABLE 4. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±0.2V, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency				650	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 650MHz		1.8		ns
*t*sk(o)	Output Skew; NOTE 2, 4			TBD		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			30		ps
t_R	Output Rise Time	20% to 80% @ 50MHz	300		700	ps
t_F	Output Fall Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		45		55	%

All parameters measured at 400MHz unless noted otherwise.
The cycle to cycle jitter on the input will equal the jitter on the output. The part does not add jitter.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

PARAMETER MEASUREMENT INFORMATION

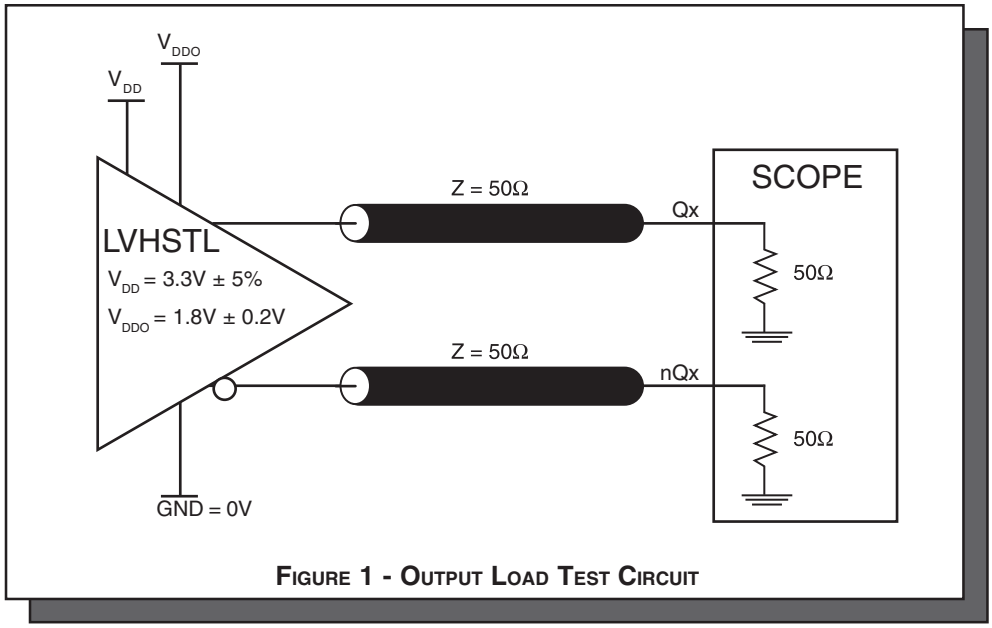


FIGURE 1 - OUTPUT LOAD TEST CIRCUIT

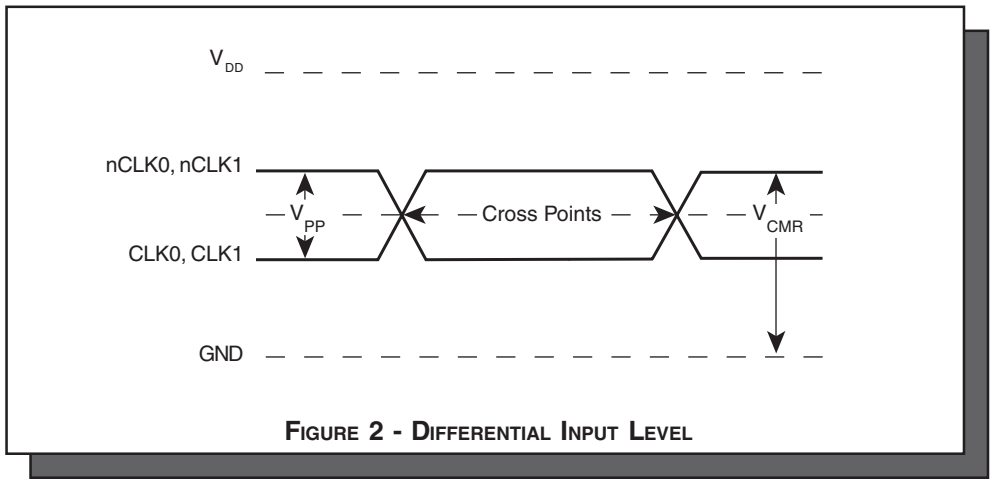


FIGURE 2 - DIFFERENTIAL INPUT LEVEL

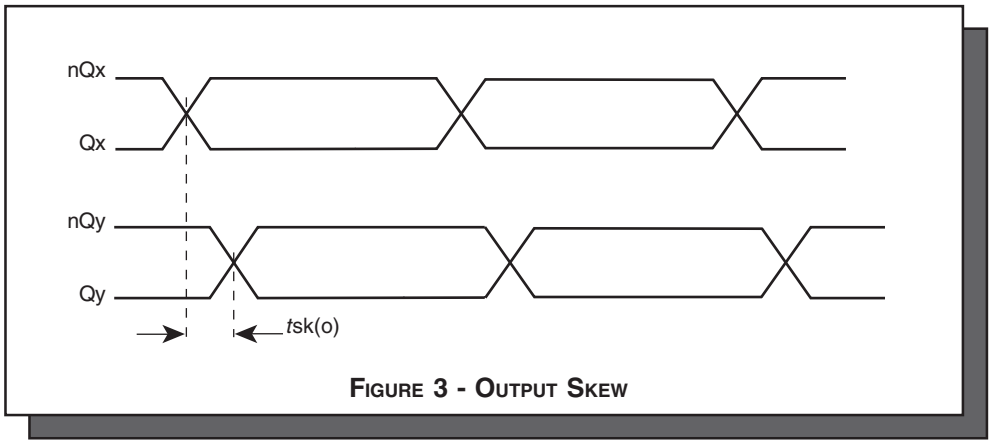


FIGURE 3 - OUTPUT SKEW

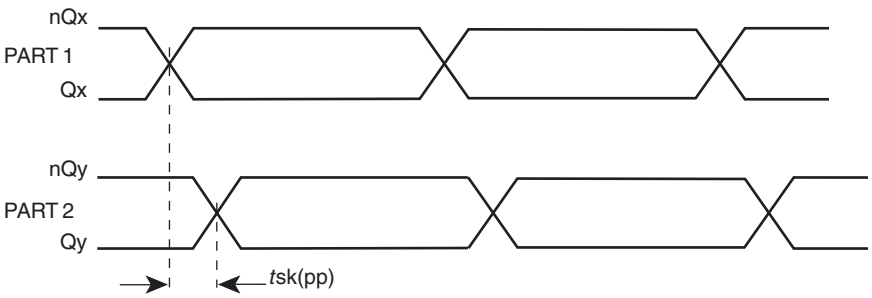


FIGURE 4 - PART-TO-PART SKEW

FIGURE 5 - INPUT AND OUTPUT RISE AND FALL TIME

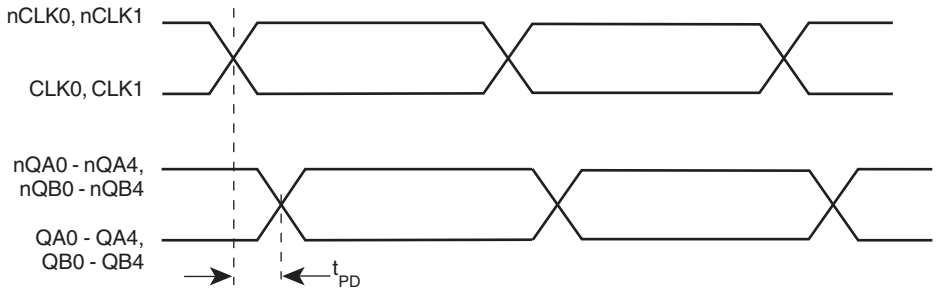


FIGURE 6 - PROPAGATION DELAY

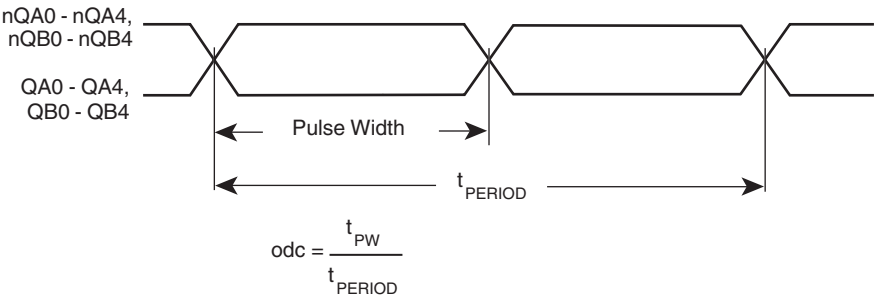


FIGURE 7 - odc & t_{PERIOD}

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 8 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

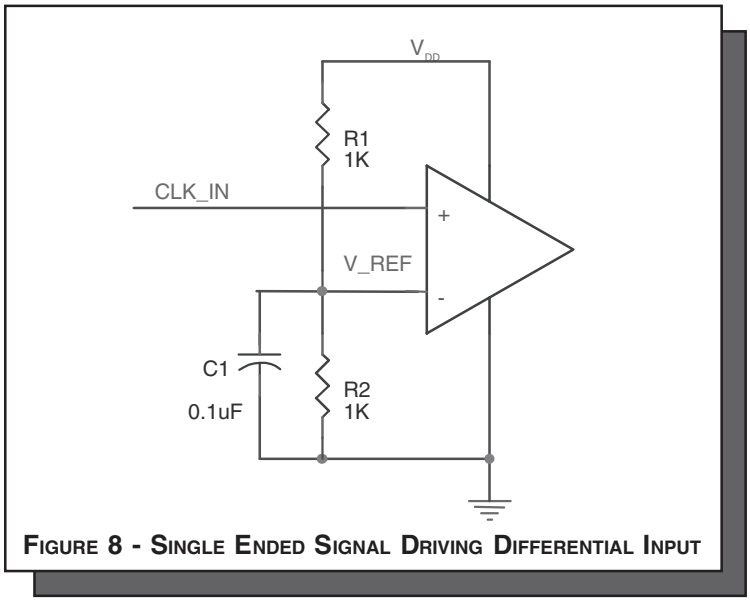


FIGURE 8 - SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS85210-21.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS85210-21 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 3.465V * 90mA = **312mW**
- Power (outputs)$_{MAX}$ = **32.8mW/Loaded Output pair**
  If all outputs are loaded, the total power is 10 * 32.8mW = **328mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 312mW + 328mW = **640mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 5 below.
Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.640W * 42.1°C/W = 97°C. This is well below the limit of 125°C

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 5. Thermal Resistance θ_{JA} for 32-pin LQFP, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVHSTL output driver circuit and termination are shown in *Figure 9.*

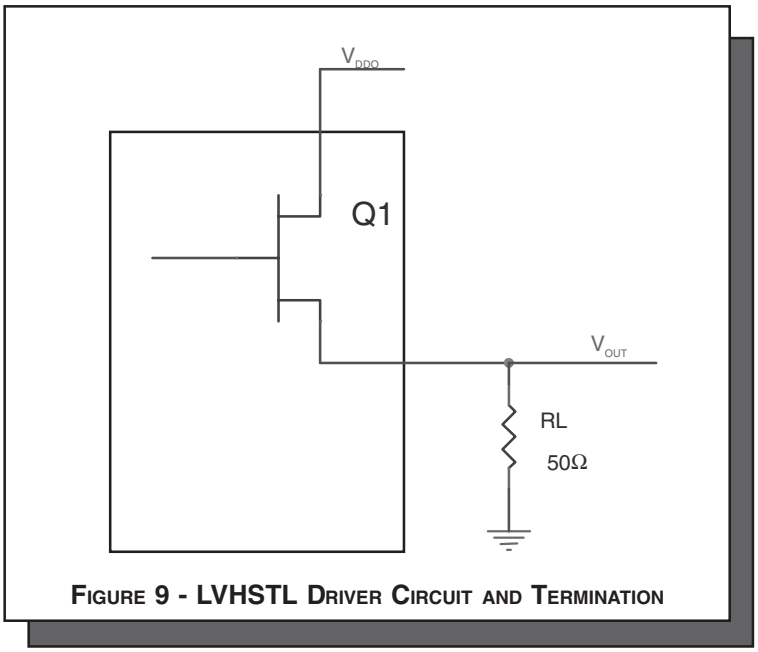


FIGURE 9 - LVHSTL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = (V_{OH\_MIN}/R_L) * (V_{DDO\_MAX} - V_{OH\_MIN})$

$Pd\_L = (V_{OL\_MAX}/R_L) * (V_{DDO\_MAX} - V_{OL\_MAX})$

Pd_H = (1.0V/50Ω) * (2V - 1.0V) = **20mW**
Pd_L = (0.4V/50Ω) * (2V - 0.4V) = **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32.8mW**

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS85210-21 is: 1216

PACKAGE OUTLINE - Y SUFFIX

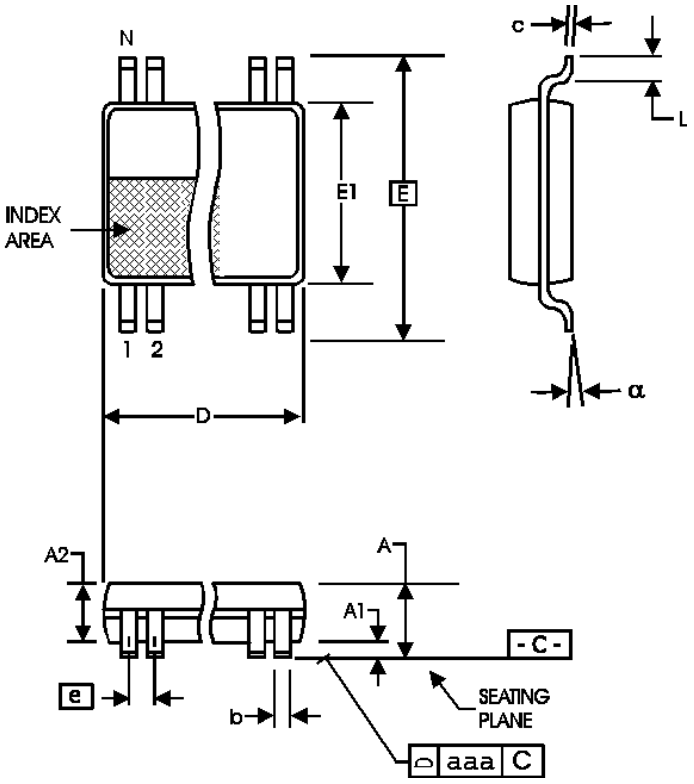


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS85210AY-21	ICS85210AY-21	32 lead LQFP	250 per tray	0°C to 70°C
ICS85210AY-21T	ICS85210AY-21	32 lead LQFP on Tape and Reel	1000	0°C to70°C