ISP1521

Hi-Speed Universal Serial Bus hub controller

Rev. 01 — 25 June 2003 **Preliminary data**

1. General description

The ISP1521 is a stand-alone Universal Serial Bus (USB) hub controller IC that complies with *Universal Serial Bus Specification Rev. 2.0*. It supports data transfer at high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s).

The upstream facing port can be connected to a Hi-Speed USB host or hub or to an Original USB host or hub. If the upstream facing port is connected to a Hi-Speed USB host or hub, then the ISP1521 will operate as a Hi-Speed USB hub. That is, it will support high-speed, full-speed and low-speed devices connected to its downstream facing ports. If the upstream facing port is connected to an Original USB host or hub, then the ISP1521 will operate as an Original USB hub. That is, high-speed devices that are connected to its downstream facing ports will operate in full-speed mode instead.

The ISP1521 is a full hardware USB hub controller. All Original USB devices connected to the downstream facing ports are handled using a single Transaction Translator (TT), when operating in a cross-version environment. This allows the whole 480 Mbit/s upstream bandwidth to be shared by all the Original USB devices on its downstream facing ports.

The ISP1521 has seven downstream facing ports. If not used, ports 3 to 7 can be disabled. The vendor ID, product ID and string descriptors on the hub are supplied by the internal ROM; they can also be supplied by an external I^{2}C-bus™ EEPROM or a microcontroller.

The ISP1521 IC is suitable for self-powered, bus-powered or hybrid-powered hub designs.

An analog overcurrent detection circuitry is built into the ISP1521, which can also accept digital overcurrent signals from external circuits; for example, Micrel MOSFET switch MIC2026. The circuitry can be configured to trip on a global or an individual overcurrent condition.

Each port comes with two status indicator LEDs.

Target applications of the ISP1521 are monitor hubs, docking stations for notebooks, internal USB hub for motherboards, hub for extending Intel® Easy PCs, hub boxes, and so on.

PHILIPS

2. Features

- Complies with:
  - *Universal Serial Bus Specification Rev. 2.0*
  - Advanced Configuration and Power Interface (ACPI™), OnNow™ and USB power management requirements
- Supports data transfer at high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s)
- Bus-powered or self-powered capability
- USB suspend mode support
- Configurable number of ports
- Internal power-on reset and low voltage reset circuit
- Port status indicators
- Integrates high performance USB interface device with hub handler, Philips Serial Interface Engine (SIE) and transceivers
- Built-in overcurrent detection circuit
- Individual or ganged power switching, individual or global overcurrent protection, and non-removable port support by I/O pins configuration
- Simple I^2C-bus (master/slave) interface to read device descriptor parameters, language ID, manufacturer ID, product ID, serial number ID and string descriptors from a dedicated external EEPROM, or to allow the microcontroller to set up hub descriptors
- Visual USB traffic monitoring (GoodLink™) for the upstream facing port
- Uses 12 MHz crystal oscillator with on-chip Phase-Locked Loop (PLL) for low ElectroMagnetic Interference (EMI)
- Full industrial operating temperature range from −40 to +85 °C
- Available in LQFP80 package.

3. Applications

- Monitor hubs
- Docking stations for notebooks
- Internal hub for USB motherboards
- Hub for extending Easy PCs
- Hub boxes.

4. Abbreviations

ACPI — Advanced Configuration and Power Interface

EMI — ElectroMagnetic Interference

ESD — ElectroStatic Discharge

NAK — Not AcKnowledge

PID — Packet Identifier

PLL — Phase-Locked Loop

SIE — Serial Interface Engine

TT — Transaction Translator

USB — Universal Serial Bus.

5. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
ISP1521BE	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1

6. Block diagram

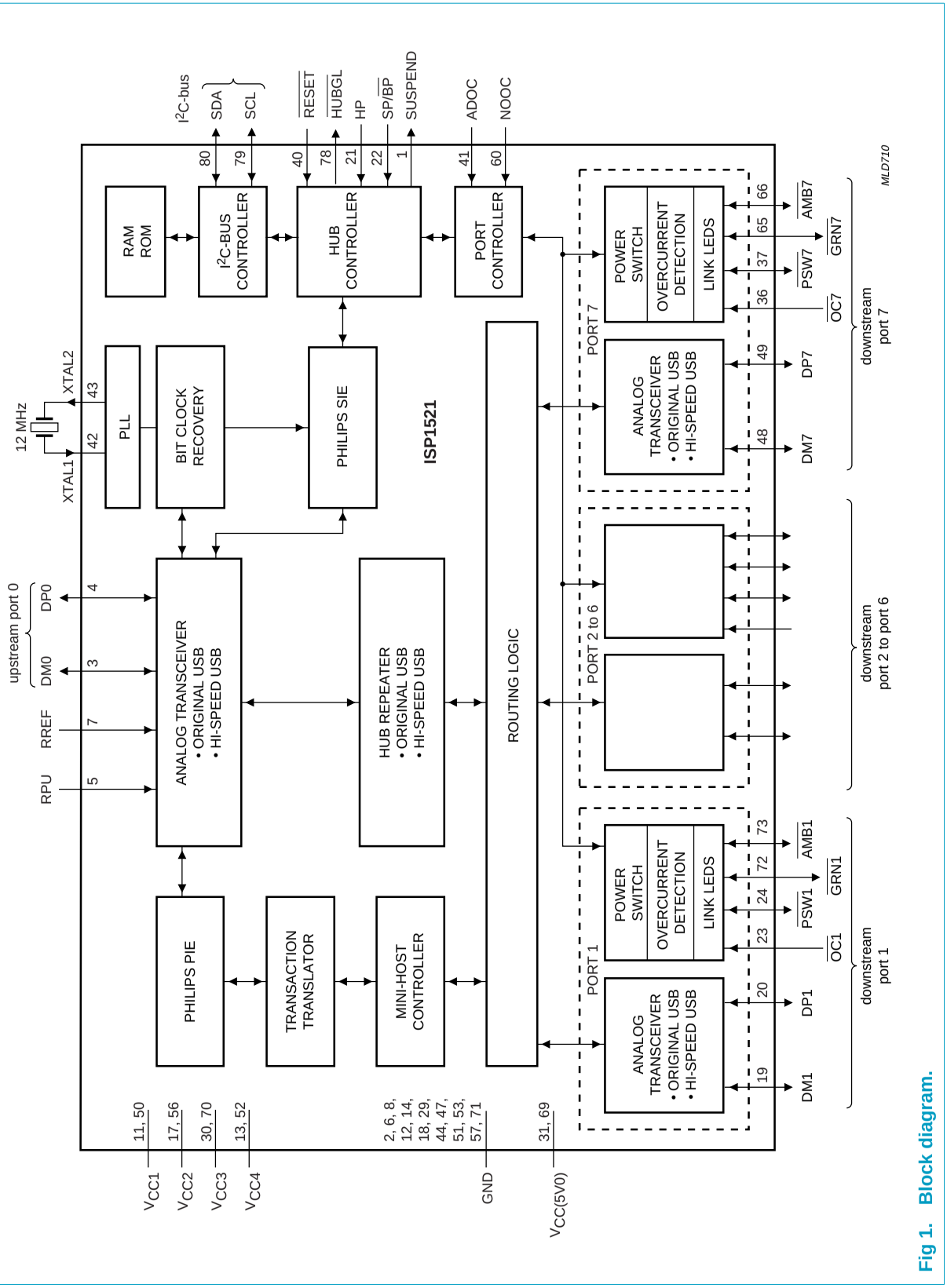


Fig 1. Block diagram.

7. Pinning information

7.1 Pinning

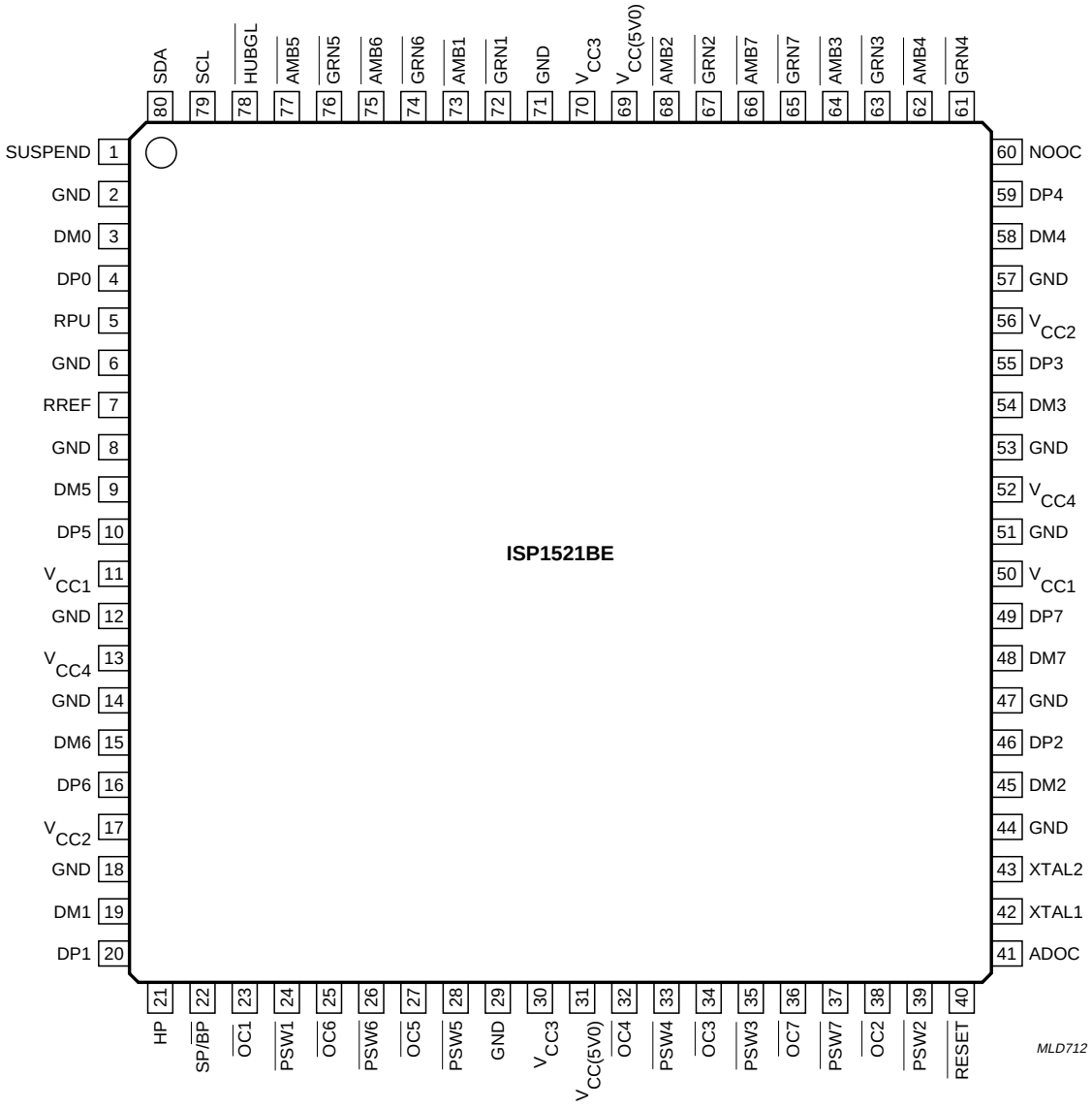


Fig 2. Pin configuration.

7.2 Pin description

Table 2: Pin description

Symbol[1]	Pin	Type	Description
SUSPEND	1	O	suspend indicator output; a HIGH level indicates that the hub is in the suspend mode
GND	2	-	ground supply
DM0	3	AI/O	upstream facing port 0 D- connection (analog)

Table 2: Pin description *...continued*

Symbol[1]	Pin	Type	Description
DP0	4	AI/O	upstream facing port 0 D+ connection (analog)
RPU	5	AI	pull-up resistor connection; connect this pin through a resistor of 1.5 kΩ ± 5% to 3.3 V
GND	6	-	ground supply
RREF	7	AI	reference resistor connection; connect this pin through a resistor of 12 kΩ ± 1% to an analog band gap ground reference
GND	8	-	ground supply
DM5	9	AI/O	downstream facing port 5 D- connection (analog)[2]
DP5	10	AI/O	downstream facing port 5 D+ connection (analog)[2]
V_{CC1}	11	-	analog supply voltage 1 (3.3 V)
GND	12	-	ground supply
V_{CC4}	13	-	crystal and PLL supply voltage 4 (3.3 V)
GND	14	-	ground supply
DM6	15	AI/O	downstream facing port 6 D- connection (analog)[2]
DP6	16	AI/O	downstream facing port 6 D+ connection (analog)[2]
V_{CC2}	17	-	transceiver supply voltage 2 (3.3 V)
GND	18	-	ground supply
DM1	19	AI/O	downstream facing port 1 D- connection (analog)[3]
DP1	20	AI/O	downstream facing port 1 D+ connection (analog)[3]
HP	21	I	hybrid-powered operation selection input; connect this pin to upstream facing V_{BUS} for the hybrid-powered operation; for pure self-powered or bus-powered operation, connect this pin to GND; see Table 4
SP/$\overline{BP}$	22	I	self-powered or bus-powered operation selection input: **self-powered (or hybrid-powered) operation —** connect this pin to the 5 V local power supply (HIGH); in the hybrid-powered operation, this pin acts as a local power supply good or loss indication **bus-powered operation —** connect this pin to GND; downstream facing ports 3 to 7 are automatically disabled
$\overline{OC1}$	23	AI/I	overcurrent sense input for downstream facing port 1 (analog/digital)
$\overline{PSW1}$	24	I/O	**output —** power switch control output (open-drain) with an internal pull-up resistor for downstream facing port 1 **input —** function of the pin when used as an input is given in Table 6
$\overline{OC6}$	25	AI/I	overcurrent sense input for downstream facing port 6 (analog/digital)
$\overline{PSW6}$	26	I/O	**output —** power switch control output (open-drain) with an internal pull-up resistor for downstream facing port 6 **input —** function of the pin when used as an input is given in Table 6
$\overline{OC5}$	27	AI/I	overcurrent sense input for downstream facing port 5 (analog/digital)

Table 2: Pin description *...continued*

Symbol[1]	Pin	Type	Description
$\overline{PSW5}$	28	I/O	**output —** power switch control output (open-drain) with an internal pull-up resistor for downstream facing port 5 **input —** function of the pin when used as an input is given in Table 6
GND	29	-	ground supply
V_{CC3}	30	-	digital supply voltage 3 (3.3 V)
$V_{CC(5V0)}$	31	-	downstream facing ports supply voltage (5 V ± 5%); used to power internal pull-up resistors of $\overline{PSWn}$ pins and as a reference voltage for the analog overcurrent detection
$\overline{OC4}$	32	AI/I	overcurrent sense input for downstream facing port 4 (analog/digital)
$\overline{PSW4}$	33	I/O	**output —** power switch control output (open-drain) with an internal pull-up resistor for downstream facing port 4 **input —** function of the pin when used as an input is given in Table 6
$\overline{OC3}$	34	AI/I	overcurrent sense input for downstream facing port 3 (analog/digital)
$\overline{PSW3}$	35	I/O	**output —** power switch control output (open-drain) with an internal pull-up resistor for downstream facing port 3 **input —** function of the pin when used as an input is given in Table 6
$\overline{OC7}$	36	AI/I	overcurrent sense input for downstream facing port 7 (analog/digital)
$\overline{PSW7}$	37	I/O	**output —** power switch control output (open-drain) with an internal pull-up resistor for downstream facing port 7 **input —** function of the pin when used as an input is given in Table 6
$\overline{OC2}$	38	AI/I	overcurrent sense input for downstream facing port 2 (analog/digital)
$\overline{PSW2}$	39	I/O	**output —** power switch control output (open-drain) with an internal pull-up resistor for downstream facing port 2 **input —** function of the pin when used as an input is given in Table 6
$\overline{RESET}$	40	I	asynchronous reset input; when reset is active, the internal switch to the 1.5 kΩ external resistor is opened, and all pins DPn and DMn are three-state; it is recommended to connect to V_{BUS} through an RC circuit; refer to the schematics in *ISP1521 Hub Demo Board User's Guide*
ADOC	41	I	analog or digital overcurrent detect selection input; a LOW selects digital mode and a HIGH (3.3 V) selects analog mode
XTAL1	42	I	crystal oscillator input (12 MHz)
XTAL2	43	O	crystal oscillator output (12 MHz)
GND	44	-	ground supply
DM2	45	AI/O	downstream facing port 2 D- connection (analog)[3]
DP2	46	AI/O	downstream facing port 2 D+ connection (analog)[3]
GND	47	-	ground supply

Table 2: Pin description *...continued*

Symbol[1]	Pin	Type	Description
DM7	48	AI/O	downstream facing port 7 D- connection (analog)[2]
DP7	49	AI/O	downstream facing port 7 D+ connection (analog)[2]
V_{CC1}	50	-	analog supply voltage 1 (3.3 V)
GND	51	-	ground supply
V_{CC4}	52	-	crystal and PLL supply voltage 4 (3.3 V)
GND	53	-	ground supply
DM3	54	AI/O	downstream facing port 3 D- connection (analog)[2]
DP3	55	AI/O	downstream facing port 3 D+ connection (analog)[2]
V_{CC2}	56	-	transceiver supply voltage 2 (3.3 V)
GND	57	-	ground supply
DM4	58	AI/O	downstream facing port 4 D- connection (analog)[2]
DP4	59	AI/O	downstream facing port 4 D+ connection (analog)[2]
NOOC	60	I	no overcurrent protection selection input; connect this pin to HIGH (3.3 V) to select no overcurrent protection; if no overcurrent is selected, all $\overline{OC}$ pins must be connected to $V_{CC(5V0)}$
$\overline{GRN4}$	61	I/O	**output —** green LED port indicator (open-drain) for downstream facing port 4 **input —** function of the pin when used as an input is given in Table 10
$\overline{AMB4}$	62	I/O	**output —** amber LED port indicator (open-drain) for downstream facing port 4 **input —** function of the pin when used as an input is given in Table 9
$\overline{GRN3}$	63	I/O	**output —** green LED port indicator (open-drain) for downstream facing port 3 **input —** function of the pin when used as an input is given in Table 10
$\overline{AMB3}$	64	I/O	**output —** amber LED port indicator (open-drain) for downstream facing port 3 **input —** function of the pin when used as an input is given in Table 9
$\overline{GRN7}$	65	I/O	**output —** green LED port indicator (open-drain) for downstream facing port 7 **input —** function of the pin when used as an input is given in Table 10
$\overline{AMB7}$	66	I/O	**output —** amber LED port indicator (open-drain) for downstream facing port 7 **input —** function of the pin when used as an input is given in Table 9
$\overline{GRN2}$	67	I/O	**output —** green LED port indicator (open-drain) for downstream facing port 2 **input —** function of the pin when used as an input is given in Table 10

Table 2: Pin description *...continued*

Symbol[1]	Pin	Type	Description
$\overline{AMB2}$	68	I/O	**output —** amber LED port indicator (open-drain) for downstream facing port 2 **input —** function of the pin when used as an input is given in Table 9
$V_{CC(5V0)}$	69	-	downstream facing ports supply voltage (5 V ± 5%); used to power internal pull-up resistors of $\overline{PSWn}$ pins and as a reference voltage for the analog overcurrent detection
V_{CC3}	70	-	digital supply voltage 3 (3.3 V)
GND	71	-	ground supply
$\overline{GRN1}$	72	I/O	**output —** green LED port indicator (open-drain) for downstream facing port 1 **input —** function of the pin when used as an input is given in Table 10
$\overline{AMB1}$	73	I/O	**output —** amber LED port indicator (open-drain) for downstream facing port 1 **input —** function of the pin when used as an input is given in Table 9
$\overline{GRN6}$	74	I/O	**output —** green LED port indicator (open-drain) for downstream facing port 6 **input —** function of the pin when used as an input is given in Table 10
$\overline{AMB6}$	75	I/O	**output —** amber LED port indicator (open-drain) for downstream facing port 6 **input —** function of the pin when used as an input is given in Table 9
$\overline{GRN5}$	76	I/O	**output —** green LED port indicator (open-drain) for downstream facing port 5 **input —** function of the pin when used as an input is given in Table 10
$\overline{AMB5}$	77	I/O	**output —** amber LED port indicator (open-drain) for downstream facing port 5 **input —** function of the pin when used as an input is given in Table 9
$\overline{HUBGL}$	78	O	hub GoodLink LED indicator output; the LED is off until the hub is configured; a transaction between the host and the hub will blink the LED off for 100 ms; this LED is off in the suspend mode (open-drain)
SCL	79	I/O	I^2C-bus clock (open-drain); see Table 12
SDA	80	I/O	I^2C-bus data (open-drain); see Table 12

[1] Symbol names with an overscore (for example, $\overline{NAME}$) represent active LOW signals.

[2] To disable a downstream port n, connect both pins DPn and DMn to V_{CC} (3.3 V); unused ports must be disabled in reverse order starting from port 7.

[3] Downstream ports 1 and 2 cannot be disabled.

8. Functional description

8.1 Analog transceivers

The integrated transceivers directly interface to USB lines. They are capable of transmitting and receiving serial data at high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s).

8.2 Hub controller core

The main components of the hub core are:

- Philips Serial Interface Engine (SIE)
- Routing logic
- Transaction Translator (TT)
- Mini-host controller
- Hub repeater
- Hub controller
- Port controller
- Bit clock recovery.

8.2.1 Philips serial interface engine

The Philips SIE implements the full USB protocol layer. It is completely hardwired for speed and needs no firmware intervention. The functions of this block include: synchronization, pattern recognition, parallel or serial conversion, bit (de-)stuffing, CRC checking and generation, Packet IDentifier verification and generation, address recognition, and handshake evaluation and generation.

8.2.2 Routing logic

The routing logic directs signaling to the appropriate modules (mini-host controller, Original USB repeater and Hi-Speed USB repeater, according to the topology in which the hub is placed.

8.2.3 Transaction translator

The TT acts as a go-between mechanism that links devices operating in the Original USB mode and the Hi-Speed USB upstream mode. For the ‘in’ direction, data is concatenated in TT buffers till the proper length is reached, before the host takes the transaction. In the reverse direction (out), the mini-host dispenses the data contained in TT buffers over a period that fits into the Original USB bandwidth. This continues until all outgoing data is emptied. TT buffers are used only on split transactions.

8.2.4 Mini-host controller

The internal mini-host generates all the Original USB IN, OUT or SETUP tokens for the downstream facing ports, while the upstream facing port is in the high-speed mode. The responses from the Original USB devices are collected in TT buffers, until the end of the complete split transaction clears the TT buffers.

8.2.5 Hub repeater

A hub repeater is responsible for managing connectivity on a per packet basis. It implements packet signaling connectivity and resume connectivity. There are two repeaters in the ISP1521: a Hi-Speed USB repeater and a Original USB repeater. The only major difference between these two repeaters is the speed at which they operate. When the hub is connected to an Original USB system, it automatically switches itself to function as a pure Original USB hub.

8.2.6 Hub and port controller

The hub controller provides status report. The port controller provides control for individual downstream facing port; it controls the port routing module. Any port status change will be reported to the host via the hub status change (interrupt) endpoint.

8.2.7 Bit clock recovery

The bit clock recovery circuit extracts the clock from the incoming USB data stream.

8.3 Phase-locked loop clock multiplier

A 12 to 480 MHz clock multiplier PLL is integrated on-chip. This allows the use of low-cost 12 MHz crystals. The low crystal frequency also minimizes ElectroMagnetic Interference (EMI). No external components are required for the operation of the PLL.

8.4 I^2C-bus controller

A simple serial I^2C-bus interface is provided to transfer vendor ID, product ID and string descriptor from an external I^2C-bus EEPROM (for example, Philips PCF8582 or equivalent) or microcontroller. A master/slave I^2C-bus protocol is implemented according to the timing requirements as mentioned in the I^2C-bus standard specifications. The maximum data count during I^2C-bus transfers for the ISP1521 is 256 bytes.

8.5 Overcurrent detection circuit

An overcurrent detection circuit is integrated on-chip. The main features of this circuit are: self reporting, automatic resetting, low-trip time and low cost. This circuit offers an easy solution at no extra hardware cost on the board.

8.6 GoodLink

Indication of a good USB connection is provided through GoodLink technology. An LED can be directly connected to pin $\overline{\text{HUBGL}}$ via an external 330 Ω resistor.

During enumeration, the LED blinks on momentarily. After successful configuration, the LED blinks off for 100 ms upon each transaction.

This feature provides a user-friendly indication of the status of the hub, the connected downstream devices and the USB traffic. It is a useful diagnostics tool to isolate faulty USB equipment and helps to reduce field support and hotline costs.

8.7 Power switch and hub power modes

USB hubs can either be self-powered or bus-powered.

Self-powered — Self-powered hubs have a 5 V local power supply on board that provides power to the hub and the downstream ports. The *Universal Serial Bus Specification Rev. 2.0* requires that these hubs limit current to 500 mA per downstream port and report overcurrent conditions to the host.

Bus-powered — Bus-powered hubs obtain all power from the host or an upstream self-powered hub. The maximum current is 100 mA per downstream port. Current limiting and reporting of overcurrent conditions are both optional.

Hybrid powered — As an option, the hub may draw current from the USB supply (V_{BUS}) to power the interface functions.

Power switching of downstream ports can be done **individually** or **ganged**, where all ports are simultaneously switched with one power switch. The ISP1521 supports both modes, which can be selected using input $\overline{PSWn}$; see Table 6.

8.7.1 Voltage drop requirements

Self-powered: Self-powered hubs are required to provide a minimum of 4.75 V to its output port connectors at all legal load conditions. To comply with Underwriters Laboratory Inc. (UL) safety requirements, the power from any port must be limited to 25 W (5 A at 5 V). Overcurrent protection may be implemented on a global or individual basis.

Assuming a 5 V ± 3% power supply, the worst-case supply voltage is 4.85 V. This only allows a voltage drop of 100 mV across the hub Printed-Circuit Board (PCB) to each downstream connector. This includes a voltage drop across the:

- Power supply connector
- Hub PCB (power and ground traces, ferrite beads)
- Power switch (FET on-resistance)
- Overcurrent sense device.

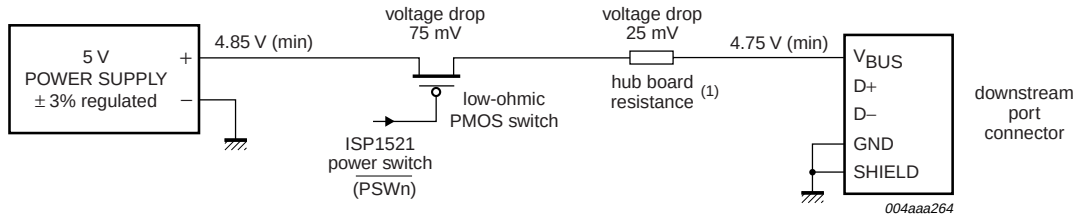
The PCB resistance and power supply connector resistance may cause a drop of 25 mV, leaving only 75 mV as the voltage drop allowed across the power switch and overcurrent sense device. The individual voltage drop components are shown in Figure 3.

For global overcurrent detection, an increased voltage drop is needed for the overcurrent sense device (in this case, a low-ohmic resistor). This can be realized by using a special power supply of 5.1 V ± 3%, as shown in Figure 4.

Bus-powered: Bus-powered hubs are guaranteed to receive a supply voltage of 4.5 V at the upstream port connector and must provide a minimum of 4.4 V to the downstream port connectors. The voltage drop of 100 mV across bus-powered hubs include:

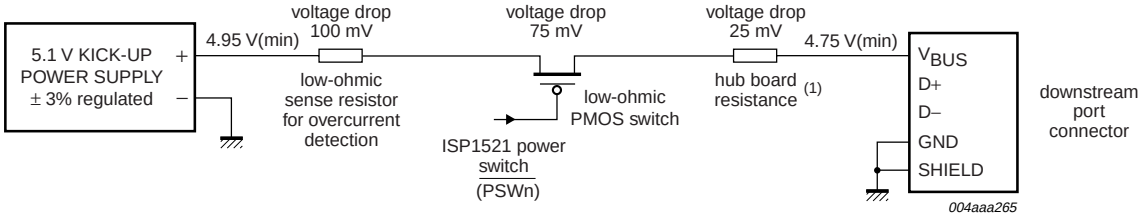
- Hub PCB (power and ground traces, ferrite beads)
- Power switch (FET on-resistance)
- Overcurrent sense device.

The PCB resistance may cause a drop of 25 mV, which leaves 75 mV for the power switch and overcurrent sense device. The voltage drop components are shown in Figure 5. For bus-powered hubs, overcurrent protection is optional. It may be implemented for all downstream ports on a global or an individual basis.



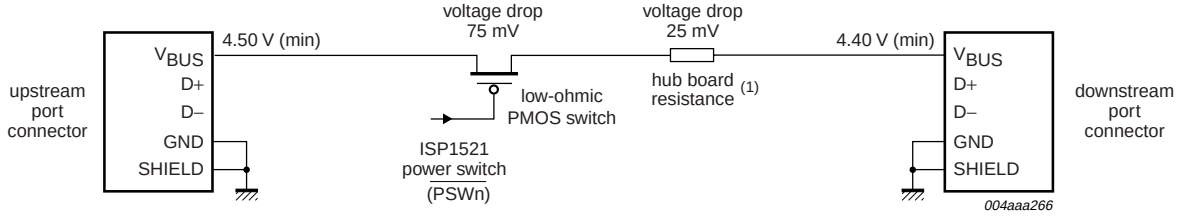
(1) Includes PCB traces, ferrite beads, and so on.

Fig 3. Typical voltage drop components in the self-powered mode using individual overcurrent detection.



(1) Includes PCB traces, ferrite beads, and so on.

Fig 4. Typical voltage drop components in the self-powered mode using global overcurrent detection.



(1) Includes PCB traces, ferrite beads, and so on.

Fig 5. Typical voltage drop components in the bus-powered mode (no overcurrent detection).

9. Configuration selections

The ISP1521 is configured through I/O pins and, optionally, through an external I^2C-bus, in which case the hub can update its configuration descriptors as a master or as a slave.

Table 3 shows the configuration parameters.

Table 3: Configuration parameters

Mode and selection	Option	Configuration method			
		Pin control		Software control	
		Control pin	Reference	Affected field	Reference
Hub power operating mode	self-powered hybrid-powered bus-powered	HP and SP/$\overline{BP}$	see Section 9.1.1	bmAttributes	see Table 19
				MaxPower: maximum bus power	see Table 19
Number of downstream facing ports	2 ports 3 ports 4 ports 5 ports 6 ports 7 ports	DM1/DP1 to DM7/DP7	see Section 9.1.2	bNbrPorts0: in bus-powered mode only 2 ports	see Table 23
Power switching mode	none ganged multiple ganged[1] individual	$\overline{PSW1}$ to $\overline{PSW7}$	see Section 9.1.3	wHubCharacteristics: bits D1 and D0	see Table 23
				bPwrOn2PwrGood: time interval	
Overcurrent protection mode	none global[2] multiple ganged individual	NOOC and $\overline{OC1}$ to $\overline{OC7}$	see Section 9.1.4	wHubCharacteristics: bits D4 and D3	see Table 23
Non-removable ports	any port can be non-removable	$\overline{AMBn}$	see Section 9.1.5	wHubCharacteristics: bit D2 (compound hub)	see Table 23
				DeviceRemovable: bit map	
Port indicator support	no yes	all $\overline{GRNn}$	see Section 9.1.6	wHubCharacteristics: bit D7	see Table 23

[1] Multiple ganged power mode is reported as individual power mode; refer to the USB 2.0 specification.

[2] When the hub uses the global overcurrent protection mode, the overcurrent indication is through the wHubStatus field bit 1 (overcurrent) and the corresponding change bit (overcurrent change).

9.1 Configuration through I/O pins

9.1.1 Hub power operating modes

Table 4 lists all possible combinations of the hub power operating mode.

Bus-powered operation — connect pins HP and SP/$\overline{BP}$ to ground; downstream facing ports 3 to 7 are automatically disabled.

Self-powered operation — connect pin HP to ground and pin SP/$\overline{BP}$ to 5 V.

Hybrid powered operation — connect pin HP to upstream facing V_{BUS}; pin SP/$\overline{BP}$ acts as a local power supply good (HIGH) or loss (LOW) indication.

Table 4: Hub power operating mode pin configuration

HP	SP/$\overline{BP}$	Hub power operating mode
LOW	LOW	bus-powered
LOW	HIGH	self-powered
HIGH	LOW	hybrid-powered (local power loss)
HIGH	HIGH	hybrid-powered (local power good)

9.1.2 Number of downstream facing ports

To discount a physical downstream facing port, connect pins DP and DM of that downstream facing port to V_{CC} (3.3 V) starting from the highest port number (7); see Table 5.

The sum of physical ports configured is reflected in the bNbrPorts field.

In the bus-powered mode, the ISP1521 has only two enabled downstream facing ports because of USB power considerations.

Table 5: Downstream facing port number pin configuration

Number of physical downstream facing port	DM1/DP1	DM2/DP2	DM3/DP3	DM4/DP4	DM5/DP5	DM6/DP6	DM7/DP7
7	15 kΩ pull-down	15 kΩ pull-down	15 kΩ pull-down	15 kΩ pull-down	15 kΩ pull-down	15 kΩ pull-down	15 kΩ pull-down
6	15 kΩ pull-down	15 kΩ pull-down	15 kΩ pull-down	15 kΩ pull-down	15 kΩ pull-down	15 kΩ pull-down	V_{CC}
5	15 kΩ pull-down	15 kΩ pull-down	15 kΩ pull-down	15 kΩ pull-down	15 kΩ pull-down	V_{CC}	V_{CC}
4	15 kΩ pull-down	15 kΩ pull-down	15 kΩ pull-down	15 kΩ pull-down	V_{CC}	V_{CC}	V_{CC}
3	15 kΩ pull-down	15 kΩ pull-down	15 kΩ pull-down	V_{CC}	V_{CC}	V_{CC}	V_{CC}
2	15 kΩ pull-down	15 kΩ pull-down	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}

9.1.3 Power switching modes

Table 6 lists the power switching mode configuration.

$\overline{PSWn}$ pins have integrated weak pull-up resistors inside the chip.

Table 6: Power switching mode: pin configuration

Power switching mode	$\overline{PSW1}$	$\overline{PSW2}$	$\overline{PSW3}$	$\overline{PSW4}$	$\overline{PSW5}$	$\overline{PSW6}$	$\overline{PSW7}$
None	ground	ground	ground	ground	ground	ground	ground
Ganged	internal pull-up	ground	ground	ground	ground	ground	ground
Individual	internal pull-up	internal pull-up	internal pull-up	internal pull-up	internal pull-up	internal pull-up	internal pull-up

9.1.4 Overcurrent protection mode

The ISP1521 supports all overcurrent protection modes: none, global, individual and multiple ganged.

No overcurrent protection mode reporting is selected when pin NOOC = HIGH. Global, individual and multiple ganged overcurrent protection modes are selected using pins $\overline{PSWn}$, following the power switching modes selection scheme; seeTable 7.

For the ganged overcurrent protection mode, the descriptor reports global overcurrent protection. Only $\overline{PSW1}$ and $\overline{OC1}$ are active; i.e. in the ganged mode, the remaining power switch pins and the overcurrent indicator pins are disabled. To inhibit the analog overcurrent detection, the $\overline{OC}$ pins must be connected to $V_{CC(5V0)}$.

Table 7: Overcurrent protection mode pin configuration

Power switching mode	NOOC	$\overline{PSW1}$	$\overline{PSW2}$	$\overline{PSW3}$	$\overline{PSW4}$	$\overline{PSW5}$	$\overline{PSW6}$	$\overline{PSW7}$
None	HIGH	ground	ground	ground	ground	ground	ground	ground
Ganged	LOW	internal pull-up	ground	ground	ground	ground	ground	ground
Individual	LOW	internal pull-up	internal pull-up	internal pull-up	internal pull-up	internal pull-up	internal pull-up	internal pull-up

Both analog and digital overcurrent modes are supported; see Table 8.

For digital overcurrent detection, the normal digital TTL level is accepted on the overcurrent input pins. For analog overcurrent detection, the threshold is given in the DC characteristics. In this mode, to filter out false overcurrent conditions because of in rush and spikes, a dead time of 15 ms is built into the IC, that is, overcurrent must persist for 15 ms before it is reported to the host.

Table 8: Overcurrent detection mode selection pin configuration

Pin ADOC	Mode selection	Description
5 V	analog	threshold ΔV_{trip}
Ground	digital	normal digital TTL level

9.1.5 Non-removable port

A non-removable port, by definition, is a port that is embedded inside the hub application box and is not accessible externally. The LED port indicators (pins $\overline{\text{AMBn}}$) of such a port are not used. Therefore, the corresponding amber LED port indicators are disabled to signify that the port is non-removable; see Table 9.

More than one non-removable port can be specified by appropriately connecting the corresponding amber LED indicators. However, at least one port should be left as a removable port.

The detection of any non-removable port sets the hub descriptor into a compound hub.

Table 9: Non-removable port pin configuration

$\overline{\text{AMBn}}$ (n = 1 to 7)	Non-removable port
Ground	non-removable
Pull-up with amber LED	removable

9.1.6 Port indicator support

The port indicator support can be disabled by grounding all green port indicators (all pins $\overline{\text{GRNn}}$); see Table 10. This is a global feature. It is not possible to disable port indicators for only one port.

Table 10: Port indicator support: pin configuration

$\overline{\text{GRN1}}$ to $\overline{\text{GRN7}}$	Port indicator support
Ground	not supported
LED pull-up green LED for at least one port	supported

9.2 Device descriptors and string descriptors settings using I²C-bus

9.2.1 Background information on I²C-bus

The I²C-bus is suitable for bi-directional communication between ICs or modules. It consists of two bi-directional lines: SDA for data signals and SCL for clock signals. Both these lines must be connected to a positive supply voltage through a pull-up resistor.

The basic I²C-bus protocol is defined as:

- Data transfer is initiated only when the bus is not busy.
- Changes in the data line occur when the clock is LOW and must be stable when the clock is HIGH. Any changes in data lines when the clock is HIGH will be interpreted as control signals.

Different conditions on I²C-bus: The I²C-bus protocol defines the following conditions:

Not busy — both SDA and SCL remain HIGH

START — a HIGH-to-LOW transition on SDA, while SCL is HIGH

STOP — a LOW-to-HIGH transition on SDA, while SCL is HIGH

Data valid — after a START condition, data on SDA must be stable for the duration of the HIGH period of SCL.

Data transfer: The master initiates each data transfer using a START condition and terminates it by generating a STOP condition. To facilitate the next byte transfer, each byte of data must be acknowledged by the receiver. The acknowledgement is done by pulling the SDA line LOW on the ninth bit of the data. An extra clock pulse needs to be generated by the master to accommodate this bit.

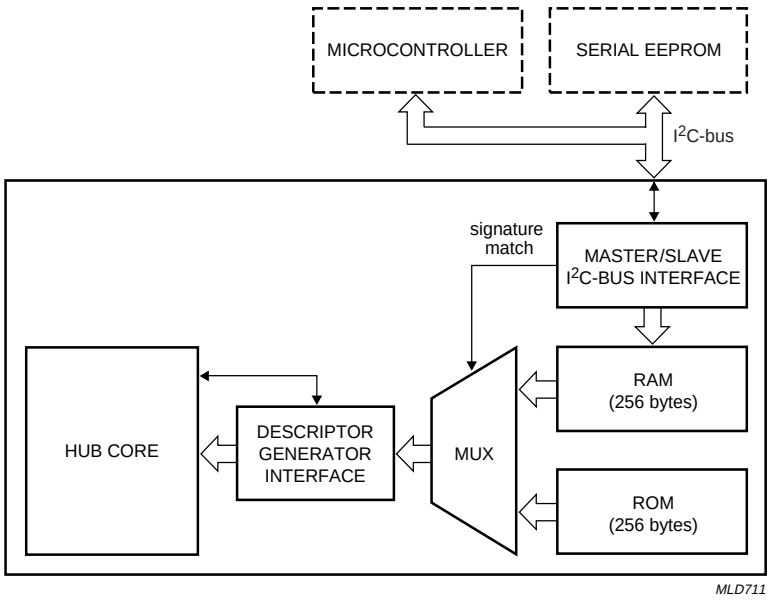
For more detailed information on the operation of the bus, refer to *The I²C-bus specification*.

I²C-bus address: The address of the ISP1521 is given in Table 11.

Table 11: I²C-bus slave address

	MSB			Slave address			LSB	
Bit	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**R/$\overline{W}$**
Value	0	0	1	1	0	1	0	0/1

9.2.2 Architecture of configurable hub descriptors



The I²C-bus cannot be shared between the EEPROM and the external microcontroller.

Fig 6. Configurable hub descriptors.

The configurable hub descriptors can be masked in the internal ROM memory; see Figure 6. These descriptors can also be supplied from an external EEPROM or a microcontroller. The ISP1521 implements both the master and slave I²C-bus controllers. The information from the external EEPROM or the microcontroller is transferred into the internal RAM during the power-on reset. A signature word is used to identify correct descriptors. If the signature matches, the content of the RAM is chosen instead of the ROM.

When the external microcontroller mode is selected and while the external microcontroller is writing to the internal RAM, any request to configurable descriptors will be responded to with a NAK (Not AcKnowledge). There is no specified time-out period for the NAK signal. This data is then passed to the host during the enumeration process.

The three configuration methods are selected by connecting pins SCL and SDA in the manner given in Table 12.

Table 12: Configuration method

Configuration method	SCL	SDA
Internal ROM	ground	ground
External EEPROM	2.2 to 4.7 kΩ pull-up	2.2 to 4.7 kΩ pull-up
External microcontroller	driven LOW by the microcontroller during reset	2.2 to 4.7 kΩ pull-up

9.2.3 ROM or EEPROM map

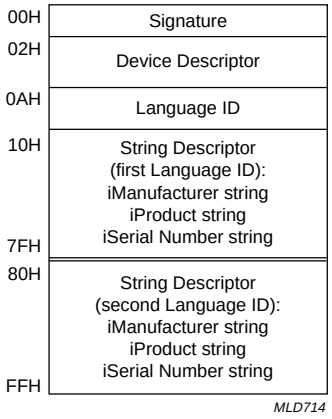


Fig 7. ROM or EEPROM map.

Remark: A 128-byte EEPROM supports one language ID only, and a 256-byte EEPROM supports two language IDs.

9.2.4 ROM or EEPROM detailed map

Table 13: ROM or EEPROM detailed map

Address (Hex)	Content	Default (Hex)	Example (Hex)	Comment
Signature descriptor				
00	signature (low	55	-	signature to signify valid data comment
01	signature (high)	AA	-	
Device descriptor				
02	idVendor (low)	CC	-	Philips Semiconductors vendor ID
03	idVendor (high)	04	-	
04	idProduct (low)	21	-	ISP1521 product ID
05	idProduct (high)	15	-	

Table 13: ROM or EEPROM detailed map*…continued*

Address (Hex)	Content	Default (Hex)	Example (Hex)	Comment
06	bcdDevice (low)	00	-	device release; silicon revision increments this value
07	bcdDevice (high)	02	-	
08	RSV, iSN, iP, iM	-	00	if all the three strings are supported, the value of this byte is 39H
09	reserved	-	FF	-
String descriptor Index 0 (language ID)				
0A	bLength[1]	-	06	two language ID support
0B	bDescriptorType	-	03[2]	STRING
0C	wLANGID[0]	-	09	LANGID code zero (first language ID) (English—USA in this example)
0D		-	04	
0E	wLANGID[1]	-	09	LANGID code one (second language ID) (English—UK in this example)
0F		-	08	
String descriptor Index 1 (iManufacturer)[3]				
10	bLength	-	2E	string descriptor length (manufacturer ID)
11	bDescriptorType	-	03[2]	STRING
12 13	bString	-	50 00	P of Philips
14 15		-	68 00	h
16 17		-	69 00	i
18 19		-	6C 00	l
1A 1B		-	69 00	i
1C 1D		-	70 00	p
1E 1F		-	73 00	s
20 21		-	20 00	
22 23		-	53 00	S of Semiconductors
24 25		-	65 00	e
26 27		-	6D 00	m
28 29		-	69 00	i
2A 2B		-	63 00	c
2C 2D		-	6F 00	o
2E 2F		-	6E 00	n
30 31		-	64 00	d
32 33		-	75 00	u
34 35		-	63 00	c
36 37		-	74 00	t
38 39		-	6F 00	o
3A 3B		-	72 00	r
3C 3D		-	73 00	s

Table 13: ROM or EEPROM detailed map…*continued*

Address (Hex)	Content	Default (Hex)	Example (Hex)	Comment
String descriptor Index 2 (iProduct)				
3E	bLength	-	10	string descriptor length (product ID)
3F	bDescriptorType	-	03[2]	STRING
40 41	bString	-	49 00	I of ISP1521
42 43		-	53 00	S
44 45		-	50 00	P
46 47		-	31 00	1
48 49		-	35 00	5
4A 4B		-	32 00	2
4C 4D		-	31 00	1
String descriptor Index 3 (iSerialNumber) **Remark: If supported, this string must be unique.**				
4E	bLength	-	3A	string descriptor length (serial number)
4F	bDescriptorType	-	03[2]	STRING
50 51	bString	-	39 00	9 of 947337877678 = wired support
52 53		-	34 00	4
54 55		-	37 00	7
56 57		-	33 00	3
58 59		-	33 00	3
5A 5B		-	37 00	7
5C 5D		-	38 00	8
5E 5F		-	37 00	7
60 61		-	37 00	7
62 63		-	36 00	6
64 65		-	37 00	7
66 67		-	38 00	8
68 69		-	20 00	
6A 6B		-	3D 00	=
6C 6D		-	20 00	
6E 6F		-	77 00	w
70 71		-	69 00	i
72 73		-	72 00	r
74 75		-	65 00	e
76 77		-	64 00	d
78 79		-	20 00	
7A 7B		-	73 00	s
7C 7D		-	75 00	u
7E 7F		-	70 00	p
80 81		-	70 00	p
82 83		-	6F 00	o

Table 13: ROM or EEPROM detailed map…*continued*

Address (Hex)	Content	Default (Hex)	Example (Hex)	Comment
84 85		-	72 00	r
86 87		-	74 00	t
String descriptor Index 1 (iManufacturer) second language				
88	bLength	-	2E	string descriptor length (manufacturer ID)
89	bDescriptorType	-	03[2]	STRING
8A 8B	bString	-	50 00	P of Philips
8C 8D		-	68 00	h
8E 8F		-	69 00	i
90 91		-	6C 00	l
92 93		-	69 00	i
94 95		-	70 00	p
96 97		-	73 00	s
98 99		-	20 00	
9A 9B		-	53 00	S of Semiconductors
9C 9D		-	65 00	e
9E 9F		-	6D 00	m
A0 A1		-	69 00	i
A2 A3		-	63 00	c
A4 A5		-	6F 00	o
A6 A7		-	6E 00	n
A8 A9		-	64 00	d
AA AB		-	75 00	u
AC AD		-	63 00	c
AE AF		-	74 00	t
B0 B1		-	6F 00	o
B2 B3		-	72 00	r
B4 B5		-	73 00	s
String descriptor Index 2 (iProduct)				
B6	bLength	-	10[1]	string descriptors (product ID)
B7	bDescriptorType	-	03[2]	STRING
B8 B9	bString	-	49 00	I of ISP1521
BA BB		-	53 00	S
BC BD		-	50 00	P
BE BF		-	31 00	1
C0 C1		-	35 00	5
C2 C3		-	32 00	2
C4 C5		-	31 00	1

Table 13: ROM or EEPROM detailed map *…continued*

Address (Hex)	Content	Default (Hex)	Example (Hex)	Comment
String descriptor Index 3 (iSerialNumber)				
C6	bLength	-	16[1]	string descriptors (serial number)
C7	bDescriptorType	-	03[2]	STRING
C8 C9	bString	-	36 00	6 of 6568824022
CA CB		-	35 00	5
CC CD		-	36 00	6
CE CF		-	38 00	8
D0 D1		-	38 00	8
D2 D3		-	32 00	2
D4 D5		-	34 00	4
D6 D7		-	30 00	0
D8 D9		-	32 00	2
DA DB		-	32 00	2
DC DD		-	FF FF	
DE DF		-	FF FF	
E0 E1		-	FF FF	
E2 E3		-	FF FF	
E4 E5		-	FF FF	
E6 E7		-	FF FF	
E8 E9		-	FF FF	
EA EB		-	FF FF	
EC ED		-	FF FF	
EE EF		-	FF FF	
F0 F1		-	FF FF	
F2 F3		-	FF FF	
F4 F5		-	FF FF	
F6 F7		-	FF FF	
F8 F9		-	FF FF	
FA FB		-	FF FF	
FC FD		-	FF FF	
FE		-	FF	
FF		-	FF	upper boundary of all string descriptors

[1] If this string descriptor is not supported, this bLength field must be programmed with the value 02H.

[2] If this string descriptor is not supported, this bDescriptorType field must be used (programmed with any value, for example, 03H).

[3] String descriptor index (iManufacturer) starts from the address 0EH for one language ID support and 10H for two languages ID support.

10. Hub controller description

Each USB device is composed of several independent logic endpoints. An endpoint acts as a terminus of communication flow between the host and the device. At design time, each endpoint is assigned a unique number (endpoint identifier; see Table 14). The combination of the device address (given by the host during enumeration), the endpoint number and the transfer direction allows each endpoint to be uniquely referenced.

The ISP1521 has two endpoints: endpoint 0 (control) and endpoint 1 (interrupt).

Table 14: Hub endpoints

Function	Endpoint identifier	Transfer type	Direction [1]	Maximum packet size (bytes)
Hub ports 0 to 7	0	control	OUT	64
			IN	64
	1	interrupt	IN	1

[1] IN: input for the USB host; OUT: output from the USB host.

10.1 Endpoint 0

According to the USB specification, all devices must implement a default control endpoint. This endpoint is used by the host to configure the USB device. It provides access to the device configuration and allows generic USB status and control access.

The ISP1521 supports the following descriptor information through its control endpoint 0:

- Device descriptor
- Device_qualifier descriptor
- Configuration descriptor
- Interface descriptor
- Endpoint descriptor
- Hub descriptor
- Other_speed_configuration descriptor.

The maximum packet size of this endpoint is 64 bytes.

10.2 Endpoint 1

Endpoint 1 can be accessed only after the hub has been configured by the host (by sending the Set Configuration command). It is used by the ISP1521 to send the status change information to the host.

Endpoint 1 is an interrupt endpoint. The host polls this endpoint once every 255 ms. After the hub is configured, an IN token is sent by the host to request the port change status. If the hub detects no change in the port status, it returns a NAK to this request, otherwise the Status Change byte is sent. Table 15 shows the content of the change byte.

Table 15: Status Change byte: bit allocation

Bit	Name	Value	Description
0	Hub Status Change	0	no change in the hub status
		1	change in the hub status detected
1 to 7	Port n Status Change	0	no change in the status of port n (n = 1 to 7)
		1	change in the status of port n (n = 1 to 7)

11. Descriptors

The ISP1521 hub controller supports the following standard USB descriptors:

- Device
- Device_qualifier
- Other_speed_configuration
- Configuration
- Interface
- Endpoint
- Hub.

The hub returns different descriptors based on the mode of operation: full-speed or high-speed.

Table 16: Device descriptor

Offset (bytes)	Field name	Value (Hex)		Comments
		Full-speed	High-speed	
0	bLength	12	12	descriptor length = 18 bytes
1	bDescriptorType	01	01	type = DEVICE
2	bcdUSB	00	00	see USB specification Rev. 2.0
3		02	02	
4	bDeviceClass	09	09	HUB_CLASSCODE
5	bDeviceSubClass	00	00	HubSubClassCode
6	bDeviceProtocol	00	01	HubProtocolHSpeedOneTT
7	bMaxPacketSize0	40	40	packet size = 64 bytes
8	idVendor	CC	CC	Philips Semiconductors vendor ID (04CC); can be customized
9		04	04	
10	idProduct	21	21	the ISP1521 product ID; can be customized
11		15	15	
12	bcdDevice	00	00	device ID; can be customized
13		02	02	
14	iManufacturer	01	01	can be customized
15	iProduct	02	02	can be customized
16	iSerialNumber	03	03	can be customized; this value must be unique
17	bNumConfigurations	01	01	one configuration

Table 17: Device_qualifier descriptor

Offset (bytes)	Field name	Value (Hex)		Comments
		Full-speed	High-speed	
0	bLength	0A	0A	descriptor length = 10 bytes
1	bDescriptorType	06	06	type = DeviceQualifierType
2	bcdUSB	00	00	see USB specification Rev. 2.0
3		02	02	
4	bDeviceClass	09	09	HUB_CLASSCODE
5	bDeviceSubClass	00	00	HubSubClassCode
6	bDeviceProtocol	00	01	HubProtocolHSpeedOneTT
7	bMaxPacketSize0	40	40	packet size = 64 bytes
8	bNumConfigurations	01	01	number of configurations

Table 18: Other_speed_configuration descriptor

Offset (bytes)	Field name	Value (Hex)		Comments
		Full-speed	High-speed	
0	bLength	09	09	descriptor length = 9 bytes
1	bDescriptorType	07	07	type = OtherSpeedConfigurationType
2	wTotalLength	19	19	TotalConfBtye
3		00	00	
4	bNumInterfaces	01	01	-
5	bConfigurationValue	01	01	-
6	iConfiguration	00	00	no string supported
7	bmAttributes	E0	E0	self-powered or hybrid-powered
		A0	A0	others
8	bMaxPower	00	00	self-powered
		32	32	bus-powered and hybrid-powered

Table 19: Configuration descriptor

Offset (bytes)	Field name	Value (Hex)		Comments
		Full-speed	High-speed	
0	bLength	09	09	descriptor length = 9 bytes
1	bDescriptorType	02	02	type = CONFIGURATION
2	wTotalLength	19	19	total length of configuration, interface and endpoint descriptors = 25 bytes
3		00	00	
4	bNumInterfaces	01	01	one interface
5	bConfigurationValue	01	01	configuration value = 1
6	iConfiguration	00	00	no configuration string descriptor
7	bmAttributes	E0	E0	self-powered or hybrid-powered[1]
		A0	A0	bus-powered[1]
8	bMaxPower[2]	00	00	self-powered
		32	32	bus-powered and hybrid-powered

[1] Selected by input pin SP/$\overline{BP}$.

[2] Value in units of 2 mA.

Table 20: Interface descriptor

Offset (bytes)	Field name	Value (Hex)		Comments
		Full-speed	High-speed	
0	bLength	09	09	descriptor length = 9 bytes
1	bDescriptorType	04	04	type = INTERFACE
2	bInterfaceNumber	00	00	-
3	bAlternateSetting	00	00	no alternate setting
4	bNumEndpoints	01	01	status change (interrupt) endpoint
5	bInterfaceClass	09	09	HUB_CLASSCODE
6	bInterfaceSubClass	00	00	HubSubClassCode
7	bInterfaceProtocol	00	00	-
8	bInterface	00	00	no interface string descriptor

Table 21: Endpoint descriptor

Offset (bytes)	Field name	Value (Hex)		Comments
		Full-speed	High-speed	
0	bLength	07	07	descriptor length = 7 bytes
1	bDescriptorType	05	05	type = ENDPOINT
2	bEndpointAddress	81	81	endpoint 1 at the address number 1
3	bmAttributes	03	03	interrupt endpoint
4	wMaxPacketSize	01	01	packet size = 1 byte
5		00	00	
6	bInterval	FF	0C	polling interval

Table 22: Hub descriptor

Offset (bytes)	Field name	Value (Hex)		Comments
		Full-speed	High-speed	
0	bDescLength	09	09	descriptor length = 9 bytes
1	bDescriptorType	29	29	type = HUB
2	bNbrPorts	07	07	number of enabled downstream facing ports; selectable by DP/DM strapping
		06	06	
		05	05	
		04	04	
		03	03	
		02	02	
3	wHubCharacteristics	A9	A9	see Table 23
4		00	00	
5	bPwrOn2PwrGood[1]	32	32	ganged or individual mode = 100 ms
		00	00	no power switching mode = 0 ms
6	bHubContrCurrent	64	64	-
7	DeviceRemovable	00	00	seven downstream facing ports, no embedded port
8	PortPwrCtrlMask	FF	FF	-

[1] Value in units of 2 ms.

Table 23: WHubCharacteristics bit description

Bit	Function	Value	Description
D0, D1	logical power switching mode	00	ganged
		01	individual and multiple ganged
		10	none
		11	-
D2	compound hub selection	0	non-compound
		1	compound
D3, D4	overcurrent protection mode	00	global
		01	individual and multiple ganged
		10	none
		11	-
D5	-		
D6	-		
D7	port indicator	0	global feature
		1	-

12. Hub requests

The hub must react to a variety of requests initiated by the host. Some requests are standard and are implemented by any USB device whereas others are hub-class specific requests.

12.1 Standard USB requests

Table 24 shows the supported standard USB requests.

Table 24: Standard USB requests

Request	bmRequestType byte 0 (bits 7 to 0)	bRequest byte 1 (hex)	wValue byte 2, 3 (hex)	wIndex byte 4, 5 (hex)	wLength byte 6, 7 (hex)	Data response
Address						
Set Address	0000 0000	05	device address[1]	00, 00	00, 00	none
Configuration						
Get Configuration	1000 0000	08	00, 00	00, 00	01, 00	configuration value
Set Configuration (0)	0000 0000	09	00, 00	00, 00	00, 00	none
Set Configuration (1)	0000 0000	09	01, 00	00, 00	00, 00	none
Descriptors						
Get Configuration Descriptor	1000 0000	06	00, 02	00, 00	length[2]	configuration interface and endpoint descriptors
Get Device Descriptor	1000 0000	06	00, 01	00, 00	length[2]	device descriptor
Get String Descriptor (0)	1000 0000	06	03, 00	00, 00	length[2]	language ID descriptor
Get String Descriptor (1)	1000 0000	06	03, 01	00, 00	length[2]	manufacturer string
Get String Descriptor (2)	1000 0000	06	03, 02	00, 00	length[2]	product string
Get String Descriptor (3)	1000 0000	06	03, 03	00, 00	length[2]	serial number string
Feature						
Clear Device Feature (Remote_ Wakeup)	0000 0000	01	01, 00	00, 00	00, 00	none
Clear Endpoint (1) Feature (Halt/Stall)	0000 0010	01	00, 00	81, 00	00, 00	none
Set Device Feature (Remote_ Wakeup)	0000 0000	03	01, 00	00, 00	00, 00	none
Set Endpoint (1) Feature (Halt/Stall)	0000 0010	03	00, 00	81, 00	00, 00	none
Status						
Get Device Status	1000 0000	00	00, 00	00, 00	02, 00	device status
Get Interface Status	1000 0001	00	00, 00	00, 00	02, 00	zero
Get Endpoint (0) Status	1000 0010	00	00, 00	00/80, 00[3]	02, 00	endpoint 0 status
Get Endpoint (1) Status	1000 0010	00	00, 00	81, 00	02, 00	endpoint 1 status

[1] Device address: 0 to 127.

[2] Returned value in bytes.

[3] MSB specifies endpoint direction: 0 = OUT, 1 = IN. The ISP1521 accepts either value.

12.2 Hub class requests

Table 25 shows the hub class requests.

Table 25: Hub class requests

Request	bmRequestType byte 0 (bits 7 to 0)	bRequest byte 1 (hex)	wValue byte 2, 3 (hex)	wIndex byte 4, 5 (hex)	wLength byte 6, 7 (hex)	Data
Descriptor						
Get Hub Descriptor	1010 0000	06	descriptor type and index	00, 00	length[2]	descriptor
Feature						
Clear Hub Feature (C_LOCAL_POWER)	0010 0000	01	00, 00	00, 00	00, 00	none
Clear Port Feature	0010 0011	01	feature[3], 00	port[4], 00	00, 00	none
Set Port Feature	0010 0011	03	feature[3], 00	port[4], 00	00, 00	none
Status						
Get Hub Status	1010 0000	00	00, 00	00, 00	04, 00	hub status and change status
Get Port Status	1010 0011	00	00, 00	port[4], 00	04, 00	port status and change status
TT						
ClearTTBuffer	0010 0011	08	Dev_Addr, EP_nr	01, 00	00, 00	none
ResetTT	0010 0000	09	00, 00	01, 00	00, 00	none
GetTTState	1010 0011	10	TT-flags	01, 00	-[1]	TT state
StopTT	0010 0011	11	00, 00	01, 00	00, 00	none
Test modes						
Test_J	0010 0011	03	15, 00	port[4], 01	00, 00	none
Test_K	0010 0011	03	15, 00	port[4], 02	00, 00	none
Test_SE0_NAK	0010 0011	03	15, 00	port[4], 03	00, 00	none
Test_Packet	0010 0011	03	15, 00	port[4], 04	00, 00	none
Test_Force_Enable	0010 0011	03	15, 00	port[4], 05	00, 00	none

[1] Returns vendor-specific data.

[2] Returned value in bytes.

[3] Feature selector value; see Table 26.

[4] Downstream port identifier: 1 to N with N is number of enabled ports (2 to 7).

Table 26: Hub class feature selector

Feature selector name	Recipient	Value
C_HUB_LOCAL_POWER	hub	00
C_HUB_OVER_CURRENT	hub	01
PORT_CONNECTION	port	00
PORT_ENABLE	port	01
PORT_SUSPEND	port	02
PORT_OVER_CURRENT	port	03
PORT_RESET	port	04
PORT_POWER	port	08
PORT_LOW_SPEED	port	09
C_PORT_CONNECTION	port	16
C_PORT_ENABLE	port	17
C_PORT_SUSPEND	port	18
C_PORT_OVER_CURRENT	port	19
C_PORT_RESET	port	20
PORT_TEST	port	21
PORT_INDICATOR	port	22

12.3 Detailed responses to hub requests

12.3.1 Get configuration

This request returns the configuration value of the device. This request returns one byte of data; see Table 27.

Table 27: Get hub configuration response

Bit	Function	Value	Description
0	configuration value	0	device is not configured
		1	device is configured
1 to 7	reserved	0	-

12.3.2 Get device status

This request returns two bytes of data; see Table 28.

Table 28: Get device status response

Bit	Function	Value	Description
0	self-powered	0	bus-powered
		1	self-powered
1	remote wake-up	0	disabled
		1	enabled
2 to 15	reserved	0	-

12.3.3 Get interface status

The request returns two bytes of data; see Table 29.

Table 29: Get interface status response

Bit	Function	Value	Description
0 to 15	reserved	0	-

12.3.4 Get endpoint status

The request returns two bytes of data; see Table 30.

Table 30: Get endpoint status response

Bit	Function	Value	Description
0	halt	0	endpoint is not halted
		1	endpoint is halted
1 to 15	reserved	0	-

12.3.5 Get hub status

The request returns four bytes of data; see Table 31.

Table 31: Get hub status response

Bit	Function	Value	Description
0	local power source	0	local power supply good
		1	local power supply lost (inactive)
1	overcurrent indicator	0	no overcurrent condition currently exists
		1	a hub overcurrent condition exists
2 to 15	reserved	0	-
16	local power status change	0	no change in the local power status
		1	local power status has changed
17	overcurrent indicator change	0	no change in overcurrent
		1	overcurrent status has changed
18 to 31	reserved	0	-

12.3.6 Get port status

This request returns four bytes of data. The first word contains the port status bits (wPortStatus), and the next word contains the port status change bits (wPortChange). The contents of wPortStatus is given in Table 32, and the contents of wPortChange is given in Table 33.

Table 32: Get port status response (wPortStatus)

Bit	Function	Value	Description
0	current connect status	0	no device is present
		1	a device is present on this port
1	port enabled or disabled	0	port is disabled
		1	port is enabled
2	suspend	0	port is not suspended
		1	port is suspended

Table 32: Get port status response (wPortStatus) *...continued*

Bit	Function	Value	Description
3	overcurrent indicator	0	no overcurrent condition exists
		1	an overcurrent condition exists
4	reset	0	reset signaling is not asserted
		1	reset signaling is asserted
5 to 7	reserved	0	-
8	port power	0	port is in the powered-off state
		1	port is not in the powered-off state
9	low-speed device attached	0	full-speed or high-speed device is attached
		1	low-speed device is attached
10	high-speed device attached	0	full-speed device is attached
		1	high-speed device is attached
11	port test mode	0	not in the port test mode
		1	in the port test mode
12	port indicator control	0	displays default colors
		1	displays software controlled color
13 to 15	reserved	0	-

Table 33: Get port status change response (wPortChange)

Bit	Function	Value	Description
0	connect status change	0	no change in the current connect status
		1	change in the current connect status
1	port enable or disable change	0	port is enabled
		1	port is disabled
2	suspend change	0	no change
		1	resume complete
3	overcurrent indicator change	0	no change in the overcurrent indicator
		1	change in the overcurrent indicator
4	reset change	0	no change
		1	reset complete
5 to 15	reserved	0	-

12.4 Various get descriptors

bmRequestType — 10000000B

bmRequest — GET_DESCRIPTOR = 6

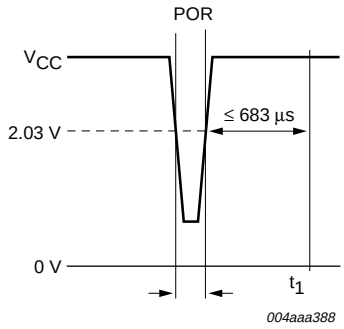
Table 34: Get descriptor request

Request name	wValue		wIndex	Data
	Descriptor index	Descriptor type	Zero/Language ID	
Get device descriptor	00	01	0	device descriptor
Get configuration descriptor	00	02	0	configuration interface and endpoint descriptors
Get language ID string descriptor	00	03	0	language ID support string
Get manufacturer string descriptor	01	03	n	manufacturer string in LANGID n
Get product string descriptor	02	03	n	product string in LANGID n
Get serial number string descriptor	03	03	n	serial number string in LANGID n

13. Power-on reset

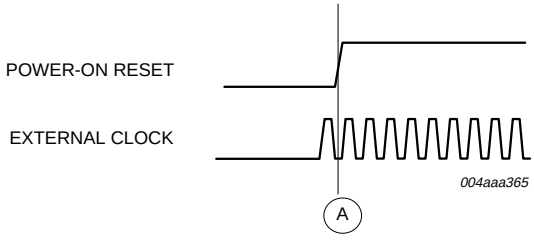
The ISP1521 has an internal Power-On Reset (POR) circuit.

The triggering voltage of the POR circuit is 2.03 V nominal. A POR is automatically generated when V_{CC} goes below the trigger voltage for a duration longer than 1 µs.



At t_1: clock is running and available.

Fig 8. Power-on reset timing.



Stable external clock is to be available at A.

Fig 9. External clock with respect to power-on reset.

14. Limiting values

Table 35: Absolute maximum ratings

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage 3.3 V			–0.5	+4.6	V
$V_{CC(5V0)}$	supply voltage 5.0 V			–0.5	+6.0	V
$V_{I(5V0)}$	input voltage on 5 V buffers	3.0 V < V_{CC} < 3.6 V	[1]	–0.5	+6.0	V
$V_{I(3V3)}$	input voltage on 3.3 V buffers	3.0 V < V_{CC} < 3.6 V		–0.5	+4.6	V
$V_{O(3V3)}$	output voltage on 3.3 V buffers			–0.5	+4.6	V
I_{lu}	latch-up current	V_I < 0 or V_I > V_{CC}		-	100	mA
V_{esd}	electrostatic discharge voltage	on pins DM1 to DM7, DP1 to DP7, $\overline{OC1}$ to $\overline{OC7}$, and all $V_{CC(5V0)}$ and GND pins; I_{LI} < 1 µA	[2][3]	–4000	+4000	V
		on all other pins; I_{LI} < 1 µA	[2][3]	–2000	+2000	V
T_{stg}	storage temperature			–40	+125	°C

[1] Valid only when supply voltage is present.

[2] Test method available on request.

[3] Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ resistor (Human Body Model).

15. Recommended operating conditions

Table 36: Recommended operating ranges

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	supply voltage 3.3 V		3.0	3.3	3.6	V
$V_{CC(5V0)}$	supply voltage 5 V	[1]	4.5	5.0	5.5	V
V_I	input voltage on 3.3 V pins		0	-	V_{CC}	V
$V_{I(5V0)}$	input voltage on 5 V tolerant pins		0	-	$V_{CC(5V0)}$	V
T_{amb}	operating temperature		–40	-	+85	°C

[1] All internal pull-up resistors are connected to this voltage.

16. Static characteristics

Table 37: Static characteristics: supply pins

V_{CC} = 3.0 to 3.6 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Full-speed							
$I_{CC(5V0)}$	supply current 5 V			-	0.5	-	mA
$I_{CC(tot)}$	total supply current 3.3 V	$I_{CC(tot)} = I_{CC1} + I_{CC2} + I_{CC3} + I_{CC4}$	[1]	-	91	-	mA
High-speed							
$I_{CC(5V0)}$	supply current 5 V			-	0.5	-	mA
$I_{CC(tot)}$	total supply current 3.3 V	suspend mode; internal clock stopped	[2][3]	-	0.5	-	mA
		no device connected; bus-powered mode; ports 3 to 7 disabled		-	120	-	mA
		no device connected		-	183	-	mA
		1 active device connected		-	231	-	mA
		2active devices connected		-	276	-	mA
		3 active devices connected		-	318	-	mA
		4 active devices connected		-	362	-	mA
		5 active devices connected		-	400	-	mA
		6 active devices connected		-	446	-	mA
		7 active devices connected		-	492	-	mA

[1] Irrespective of the number of devices connected, the value of I_{CC} is always 91 mA in full-speed.

[2] Including R_{pu} drop current.

[3] In the bus-powered mode, only two ports are active.

Table 38: Static characteristics: digital input and outputs[1]

V_{CC} = 3.0 to 3.6 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Digital input pins							
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
I_{LI}	input leakage current			−1	-	+1	µA
Schmitt-trigger input pins							
$V_{th(LH)}$	positive-going threshold voltage			1.4	-	1.9	V
$V_{th(HL)}$	negative-going threshold voltage			0.9	-	1.5	V
V_{hys}	hysteresis voltage			0.4	-	0.7	V
Overcurrent detection pins $\overline{OC1}$ to $\overline{OC7}$							
ΔV_{trip}	overcurrent detection trip voltage	$\Delta V = V_{CC} - V_{\overline{OCn}}$	[2]	-	84	-	mV
Digital output pins							
V_{OL}	LOW-level output voltage			-	-	0.4	V
V_{OH}	HIGH-level output voltage			2.4	-	-	V
Open-drain output pins							
I_{OZ}	OFF-state output current			−1	-	+1	µA

[1] All pins are 5 V tolerant.

[2] Bus-powered mode.

Table 39: Static characteristics: I²C-bus interface block

V_{CC} = 3.0 to 3.6 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input pin SCL and input/output pin SDA	[1]						
V_{IL}	LOW-level input voltage			-	-	0.9	V
V_{IH}	HIGH-level input voltage			2.1	-	-	V
V_{hys}	hysteresis voltage			0.15	-	-	V
V_{OL}	LOW-level output voltage			-	-	0.4	V
t_f	output fall time V_{IH} to V_{IL}	10 < C_b = 10 to 400 pF	[2]	-	0	250	ns

[1] All pins are 5 V tolerant.

[2] The bus capacitance (C_b) is specified in pF. To meet the specification for V_{OL} and the maximum rise time (300 ns), use an external pull-up resistor with R_{max} = 850/C_b kΩ and R_{min} = (V_{CC} − 0.4)/3 kΩ.

Table 40: Static characteristics: USB interface block (DP0 to DP7 and DM0 to DM7)

V_{CC} = 3.0 to 3.6 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input levels for high-speed							
V_{HSSQ}	squelch detection threshold (differential signal amplitude)	squelch detected		-	-	100	mV
		no squelch detected		150	-	-	mV
V_{HSCM}	data signaling common-mode voltage range			−50	-	+500	mV
Output levels for high-speed							
V_{HSOI}	idle state			−10	-	+10	mV
V_{HSOH}	data signaling HIGH			360	-	440	mV
V_{HSOL}	data signaling LOW			−10	-	+10	mV
V_{CHIRPJ}	Chirp J level (differential voltage)		[1]	700	-	1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)		[1]	−900	-	−500	mV
Input levels for full-speed and low-speed							
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{IH}	HIGH-level input voltage (drive)			2.0	-	-	V
V_{IHZ}	HIGH-level input voltage (floating)			2.7	-	3.6	V
V_{DI}	differential input sensitivity	|DP − DM|		0.2	-	-	V
V_{CM}	differential common-mode range			0.8	-	2.5	V
Output levels for full-speed and low-speed							
V_{OL}	LOW-level output voltage			0	-	0.3	V
V_{OH}	HIGH-level output voltage			2.8	-	3.6	V
V_{CRS}	output signal crossover point voltage		[2]	1.3	-	2.0	V
Leakage current							
I_{LZ}	OFF-state leakage current			−1	-	+1	µA

Table 40: Static characteristics: USB interface block (DP0 to DP7 and DM0 to DM7) *...continued*

V_{CC} = 3.0 to 3.6 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Capacitance						
C_{IN}	transceiver capacitance	pin to GND	-	-	20	pF
Resistance						
Z_{INP}	input impedance		10	-	-	MΩ
Termination						
V_{TERM}	termination voltage for pull-up resistor on pin RPU	[3]	3.0	-	3.6	V

[1] For minimum value the HS termination resistor is disabled and the pull-up resistor is connected. Only during reset, when both the hub and the device are capable of high-speed operation.

[2] Characterized only, not tested. Limits guaranteed by design.

[3] In the suspend mode, the minimum voltage is 2.7 V.

17. Dynamic characteristics

Table 41: Dynamic characteristics: system clock timing

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reset							
$t_{W(POR)}$	internal power-on reset pulse width			0.2	-	1	µs
$t_{W(\overline{RESET})}$	pulse width on pin $\overline{RESET}$			0.2	-	-	µs
Crystal oscillator							
f_{clk}	clock frequency	crystal	[1][2]	-	12	-	MHz
External clock input							
δ	clock duty cycle			-	50	-	%

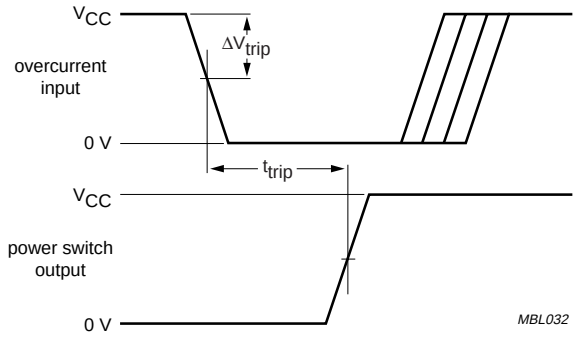
[1] Recommended accuracy of the clock frequency is 500 ppm for the crystal.

[2] Suggested values for external capacitors when using a crystal are 22 to 27 pF.

Table 42: Dynamic characteristics: overcurrent sense timing

V_{CC} = 3.0 to 3.6 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Overcurrent sense pins $\overline{OC1}$ to $\overline{OC7}$						
t_{trip}	overcurrent trip response time from $\overline{OCn}$ LOW to $\overline{PSWn}$ HIGH	see Figure 10	-	-	15	ms



Overcurrent input: pins $\overline{OCn}$; power switch output: pins $\overline{PSWn}$.

Reference voltage for overcurrent sensing: V_{CC} for bus-powered mode or $V_{SP/\overline{BP}}$ for self-powered mode.

Fig 10. Overcurrent trip response timing.

Table 43: Dynamic characteristics: digital pins[1]

V_{CC} = 3.0 to 3.6 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{t(HL)}$, $t_{t(LH)}$	output transition time		4	-	15	ns

[1] All pins are 5 V tolerant.

Table 44: Dynamic characteristics: high-speed source electrical characteristics

V_{CC} = 3.0 to 3.6 V; T_{amb} = −40 to +85 °C; test circuit Figure 25; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
t_{HSR}	rise time	10% to 90%	500	-	-	ps
t_{HSF}	fall time	90% to 10%	500	-	-	ps
Clock timing						
t_{HSDRAT}	data rate		479.76	-	480.24	Mbit/s
t_{HSFRAM}	microframe interval		124.9375	-	125.0625	µs
t_{HSRFI}	consecutive microframe interval difference		1	-	four high-speed bit times	ns

Table 45: Dynamic characteristics: full-speed source electrical characteristics

V_{CC} = 3.0 to 3.6 V; T_{amb} = −40 to +85 °C; test circuit Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Driver characteristics							
t_{FR}	rise time	C_L = 50 pF; 10% to 90% of $\|V_{OH} - V_{OL}\|$		4	-	20	ns
t_{FF}	fall time	C_L = 50 pF; 90% to 10% of $\|V_{OH} - V_{OL}\|$		4	-	20	ns
t_{FRFM}	differential rise and fall time matching		[1]	90	-	111.1	%
Z_{DRV}	driver output resistance	for the driver that is not high-speed capable		28	-	44	Ω
V_{CRS}	output signal crossover voltage		[1][2]	1.3	-	2.0	V
Data source timing[2]							
t_{DJ1}	source differential jitter for consecutive transitions	see Figure 11	[1]	−3.5	-	+3.5	ns
t_{DJ2}	source differential jitter for paired transitions	see Figure 11	[1]	−4	-	+4	ns
t_{FEOPT}	source SE0 interval of EOP	see Figure 12		160	-	175	ns
t_{FDEOP}	source differential data-to-EOP transition skew	see Figure 12		−2	-	+5	ns
Receiver timing[2]							
t_{JR1}	receiver data jitter tolerance for consecutive transitions	see Figure 13		−18.5	-	+18.5	ns
t_{JR2}	receiver data jitter tolerance for paired transitions	see Figure 13		−9	-	+9	ns
t_{FEOPR}	receiver SE0 width	accepted as EOP; see Figure 12		82	-	-	ns
t_{FST}	width of SE0 interval during differential transaction	rejected as EOP; see Figure 14		-	-	14	ns

Table 45: Dynamic characteristics: full-speed source electrical characteristics *...continued*

V_{CC} = 3.0 to 3.6 V; T_{amb} = −40 to +85 °C; test circuit Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Hub timing (downstream ports configured as full-speed)[2]						
t_{FHDD}	hub differential data delay (without cable)	see Figure 15; C_L = 0 pF	-	-	44	ns
t_{FSOP}	data bit width distortion after SOP	see Figure 15	−5	-	+5	ns
t_{FEOPD}	hub EOP delay relative to t_{HDD}	see Figure 16	0	-	15	ns
t_{FHESK}	hub EOP output width skew	see Figure 16	−15	-	+15	ns

[1] Excluding the first transition from Idle state.

[2] Characterized only, not tested. Limits guaranteed by design.

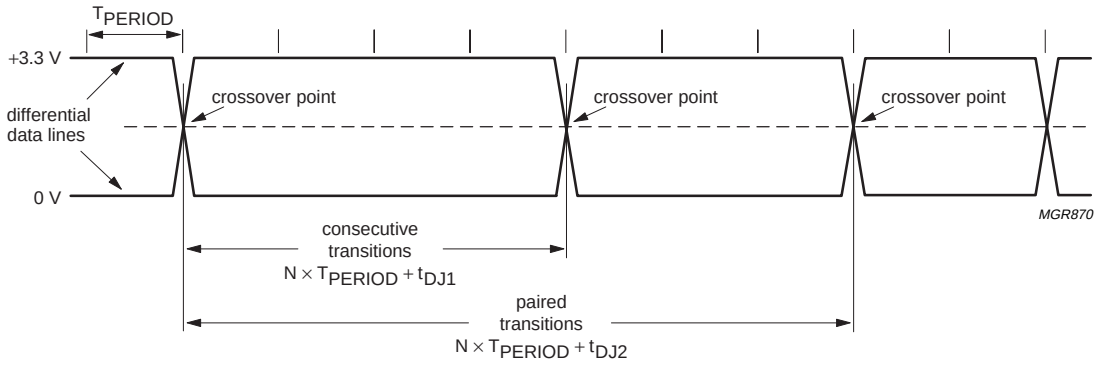
Table 46: Dynamic characteristics: low-speed source electrical characteristics

V_{CC} = 3.0 to 3.6 V; T_{amb} = −40 to +85 °C; test circuit Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
t_{LR}	rise time		75	-	300	ns
t_{LF}	fall time		75	-	300	ns
t_{LRFM}	differential rise and fall time matching	[1]	80	-	125	%
V_{CRS}	output signal crossover voltage	[1][2]	1.3	-	2.0	V
Hub timing (downstream ports configured as full-speed)						
t_{LHDD}	hub differential data delay	see Figure 15	-	-	300	ns
t_{LSOP}	data bit width distortion after SOP	see Figure 15 [2]	−60	-	+60	ns
t_{LEOPD}	hub EOP delay relative to t_{HDD}	see Figure 16 [2]	0	-	200	ns
t_{LHESK}	hub EOP output width skew	see Figure 16 [2]	−300	-	+300	ns

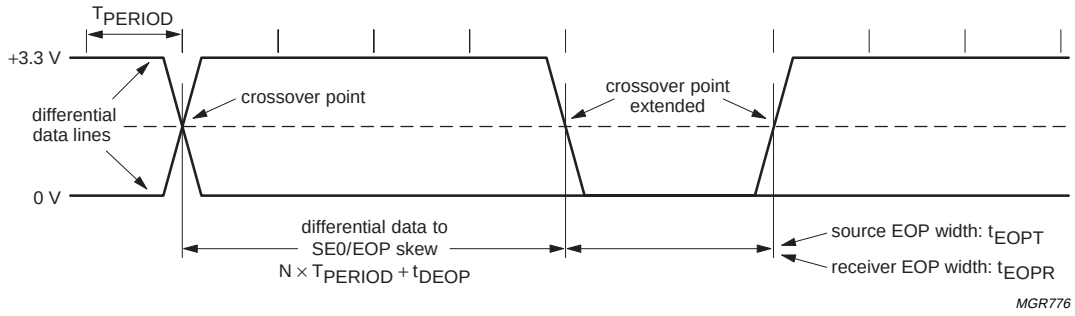
[1] Excluding the first transition from Idle state.

[2] Characterized only, not tested. Limits guaranteed by design.



T_{PERIOD} is the bit duration corresponding with the USB data rate.

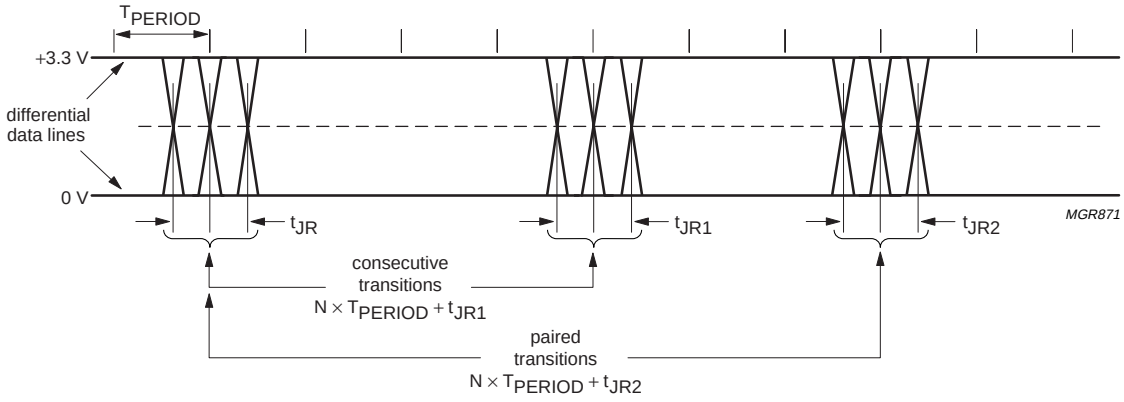
Fig 11. Source differential data jitter.



T_{PERIOD} is the bit duration corresponding with the USB data rate.

Full-speed timing symbols have a subscript prefix ‘F’, low-speed timings a prefix ‘L’.

Fig 12. Source differential data-to-EOP transition skew and EOP width.



T_{PERIOD} is the bit duration corresponding with the USB data rate.

Fig 13. Receiver differential data jitter.

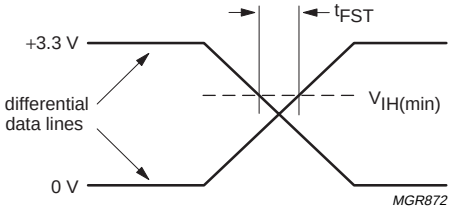
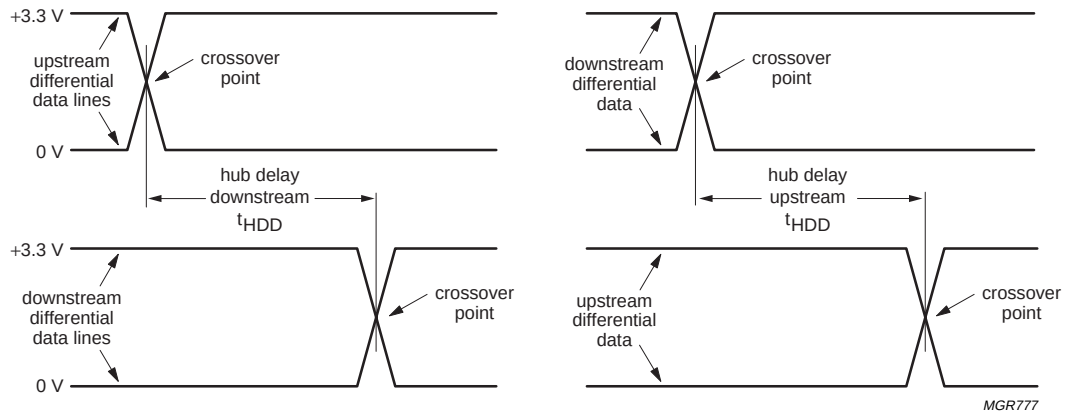


Fig 14. Receiver SE0 width tolerance.



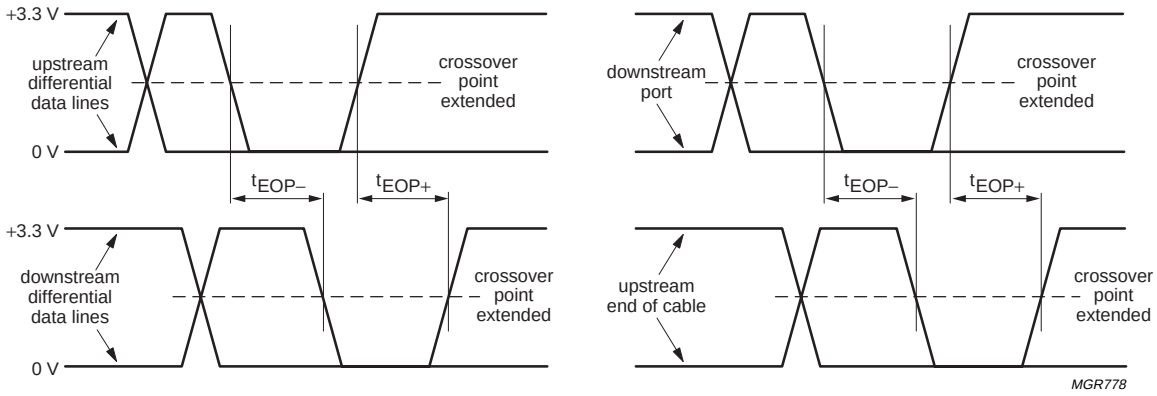
(A) downstream hub delay

(B) upstream hub delay

SOP distortion:
$t_{SOP} = t_{HDD\ (next\ J)} - t_{HDD(SOP)}$

Full-speed timing symbols have a subscript prefix 'F', low-speed timings a prefix 'L'.

Fig 15. Hub differential data delay and SOP distortion.



(A) downstream EOP delay

(B) upstream EOP delay

EOP delay:
$t_{EOP} = \max(t_{EOP-}, t_{EOP+})$

EOP delay relative to t_{HDD}:
$t_{EOPD} = t_{EOP} - t_{HDD}$

EOP skew:
$t_{HESK} = t_{EOP+} - t_{EOP-}$

Full-speed timing symbols have a subscript prefix 'F', low-speed timings a prefix 'L'.

Fig 16. Hub EOP delay and EOP skew.

Table 47: Dynamic characteristics: I²C-bus (pins SDA and SCL)

V_{CC} and T_{amb} within recommended operating range; V_{DD} = +5 V; V_{SS} = V_{GND} ; V_{IL} and V_{IH} between V_{SS} and V_{DD}.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clock frequency							
f_{SCL}	SCL clock frequency	f_{XTAL} = 12 MHz	[1]	0	93.75	100	kHz
General timing							
t_{LOW}	SCL LOW time			4.7	-	-	µs
t_{HIGH}	SCL HIGH time			4.0	-	-	µs
t_r	SCL and SDA rise time		[2]	-	-	1000	ns
t_f	SCL and SDA fall time			-	-	300	ns
C_b	capacitive load for each bus line			-	-	400	pF
SDA timing							
t_{BUF}	bus free time			4.7	-	-	µs
$t_{SU;STA}$	set-up time for (repeated) START condition			4.7	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			4.0	-	-	µs
$t_{SU;DAT}$	data set-up time			250	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition			4.0	-	-	µs
Additional I²C-bus timing							
$t_{VD;DAT}$	SCL LOW to data-out valid time			-	-	0.4	µs

[1] $f_{SCL} = {}^{1}/_{64} \times f_{XTAL}$.

[2] Rise time is determined by C_b and pull-up resistor value R_p (typical 4.7 kΩ).

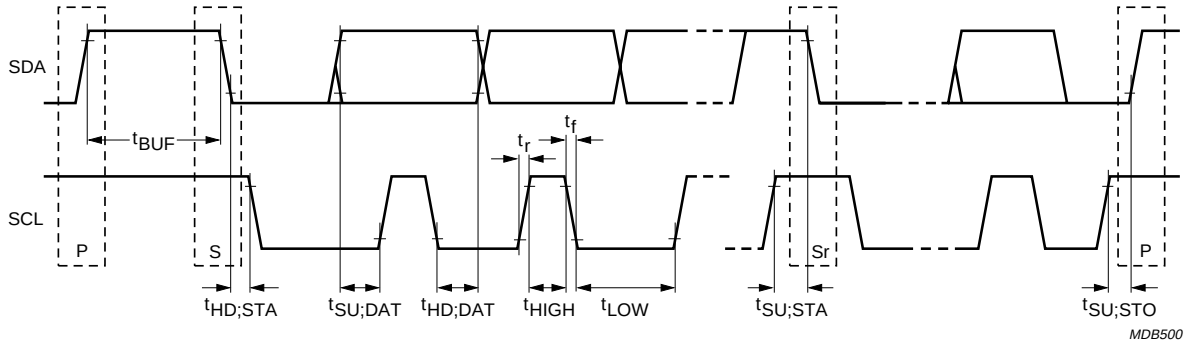
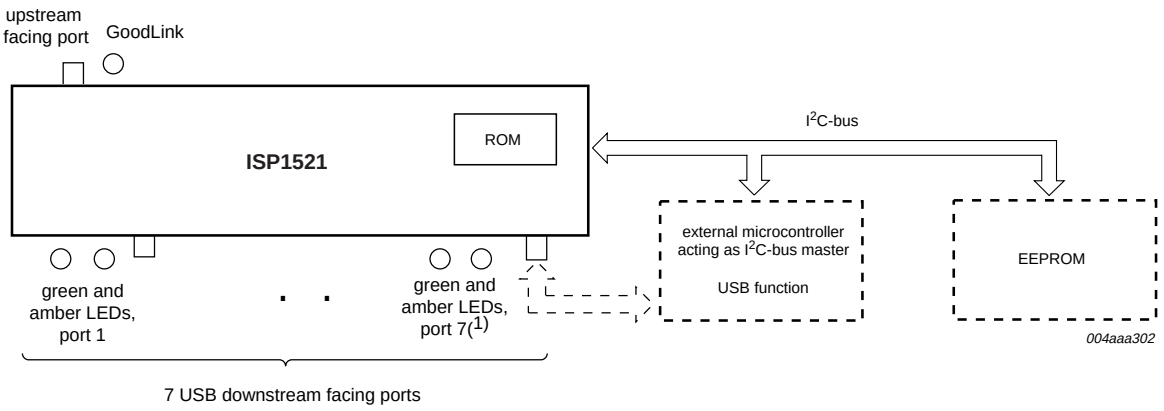


Fig 17. I²C-bus timing.

18. Application information

18.1 Descriptor configuration selection



The I^2C-bus cannot be shared between the EEPROM and the external microcontroller; see Table 12.

(1) The function on port 7, which is a non-removable port, is optional.

Fig 18. Descriptors configuration selection application diagram.

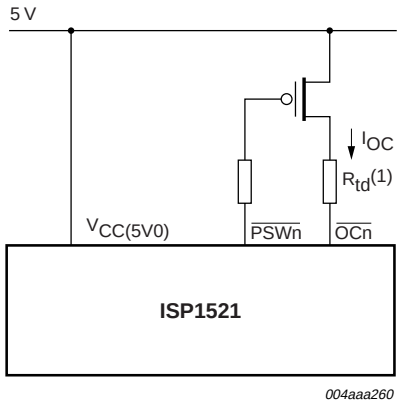
18.2 Overcurrent detection limit adjustment

For an overcurrent limit of 500 mA per port, a PMOS with R_{DSON} of approximately 100 mΩ is required. If a PMOS with a lower R_{DSON} is used, analog overcurrent detection can be adjusted by using a series resistor; see Figure 19.

$\Delta V_{PMOS} = \Delta V_{trip} = \Delta V_{trip(intrinsic)} - (I_{OC(nom)} \times R_{td})$, where:

ΔV_{PMOS} = voltage drop on PMOS

$I_{OC(nom)}$ = 0.6 µA.



(1) R_{td} is optional.

Fig 19. Adjusting analog overcurrent detection limit (optional).

18.3 Self-powered hub configurations

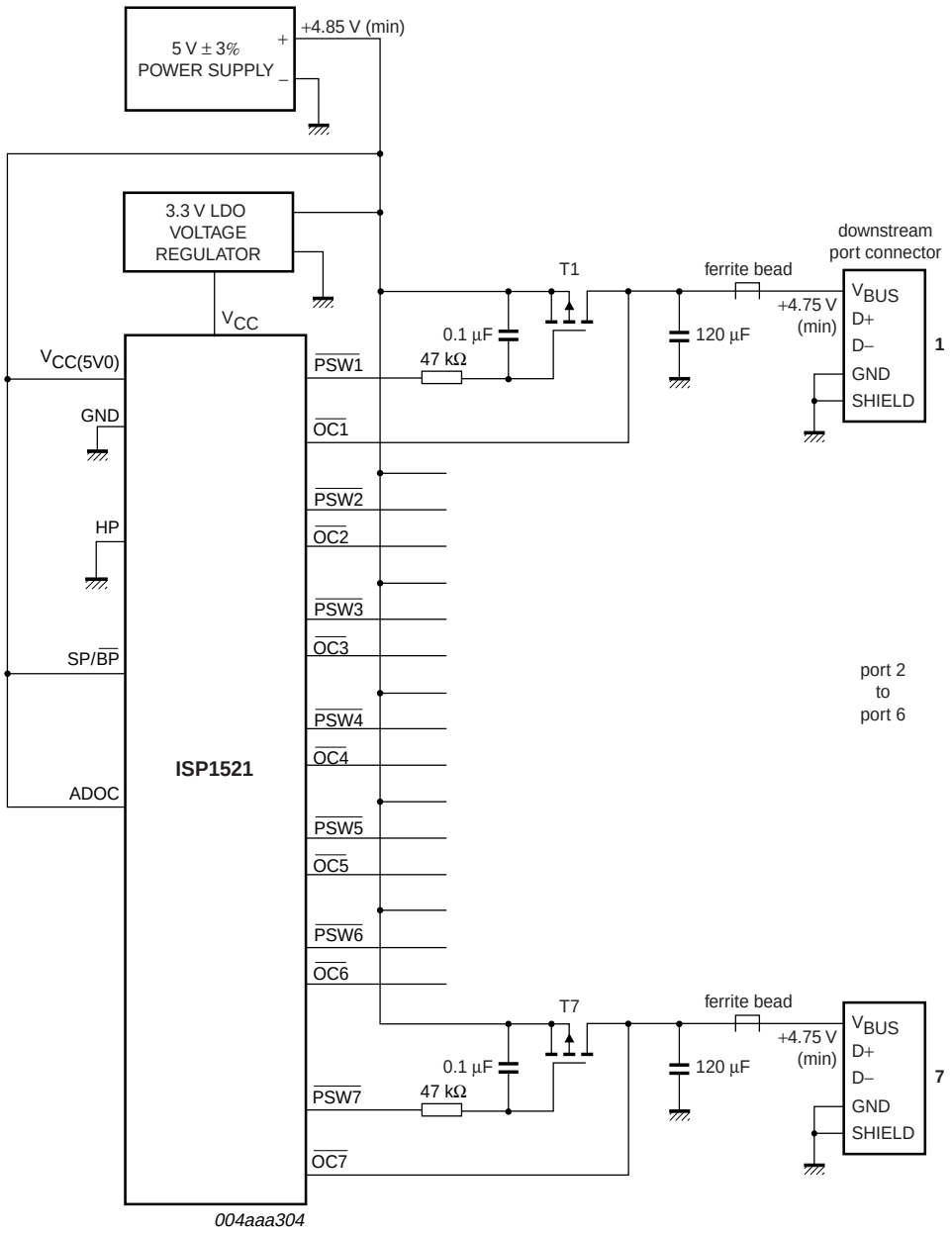


Fig 20. Self-powered hub; individual port power switching; individual overcurrent detection.

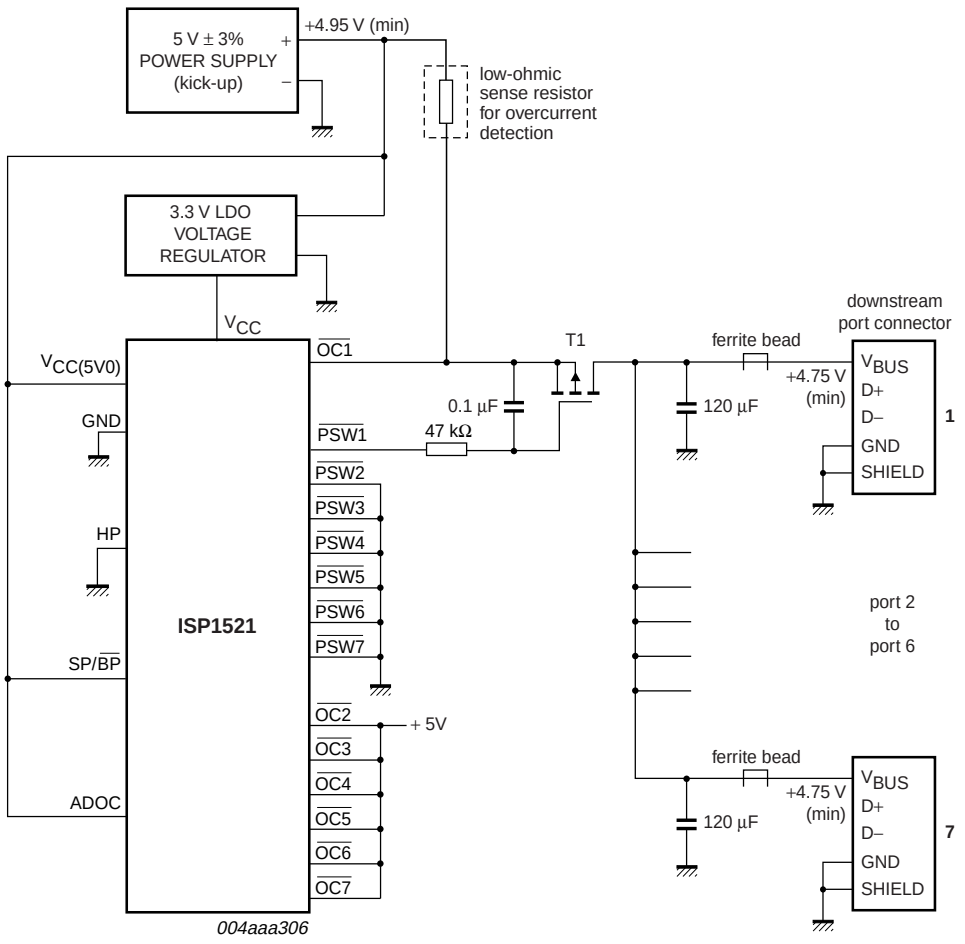


Fig 21. Self-powered hub; ganged port power switching; global overcurrent detection.

18.4 Bus-powered configurations

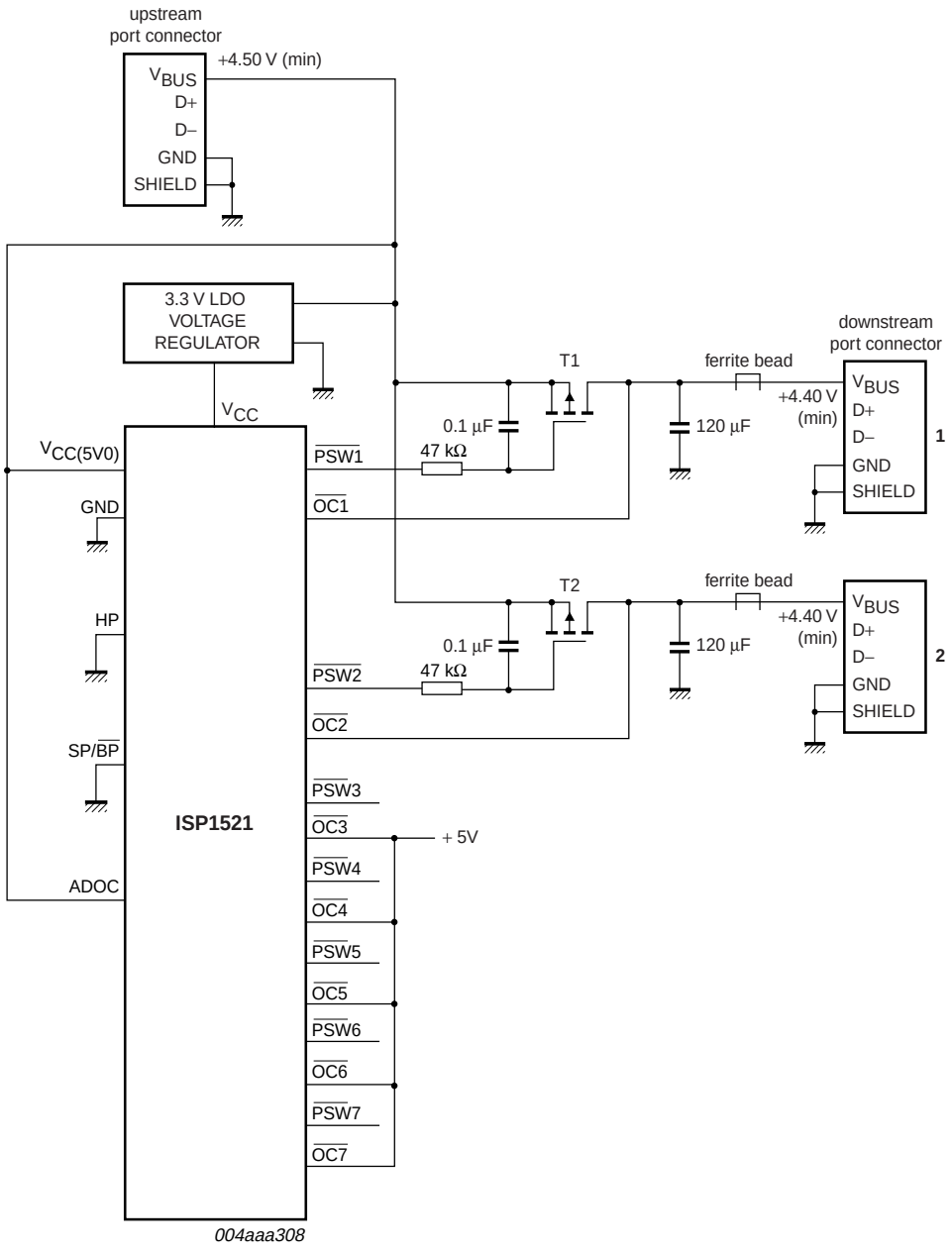


Fig 22. Bus-powered hub; individual port power switching and overcurrent detection.

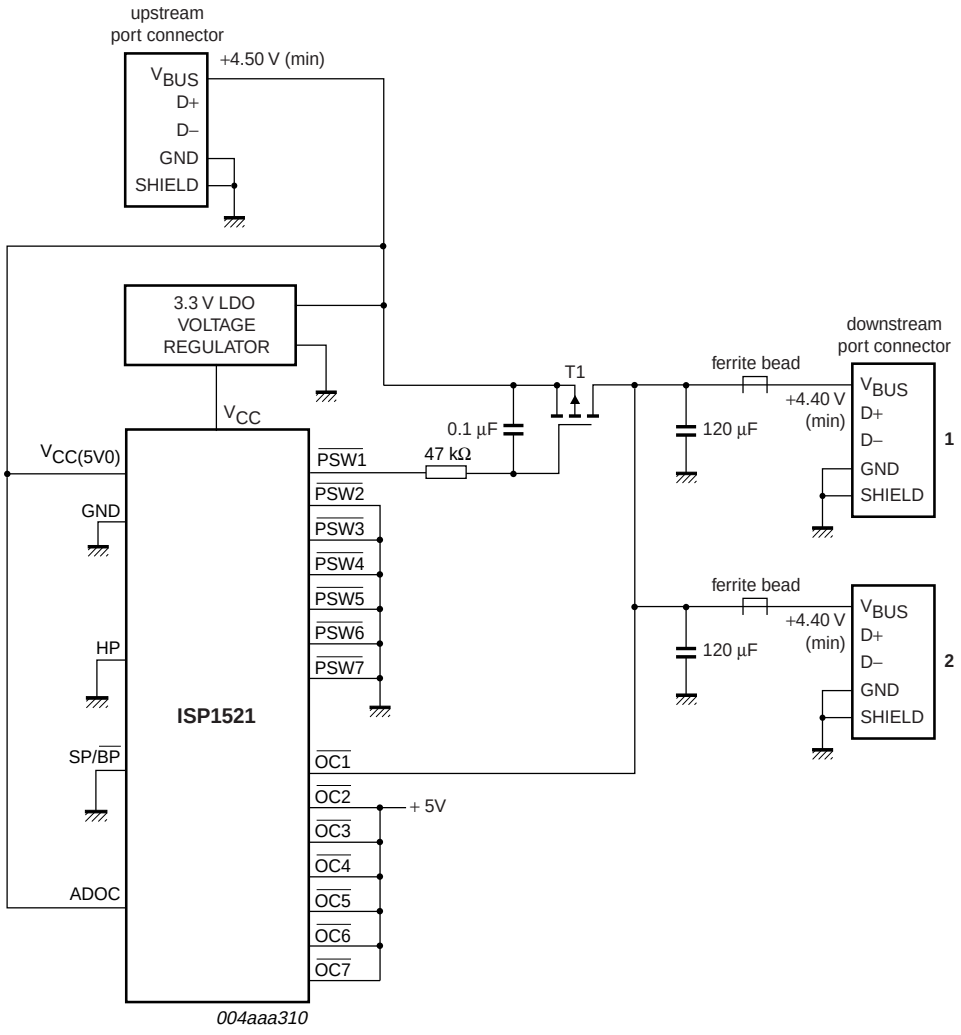


Fig 23. Bus-powered hub; ganged port power switching; global overcurrent detection.

18.5 Hybrid-powered configuration

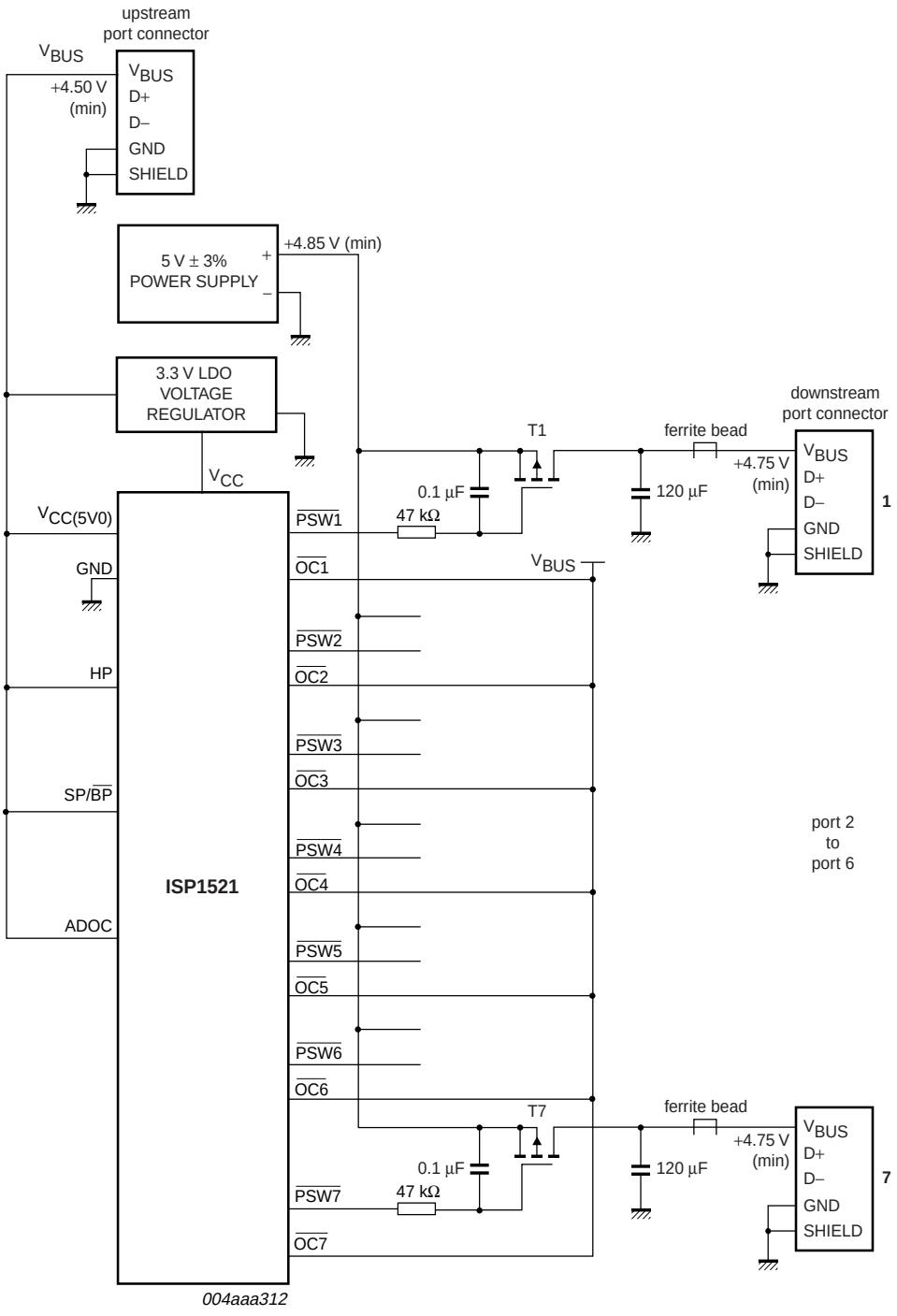
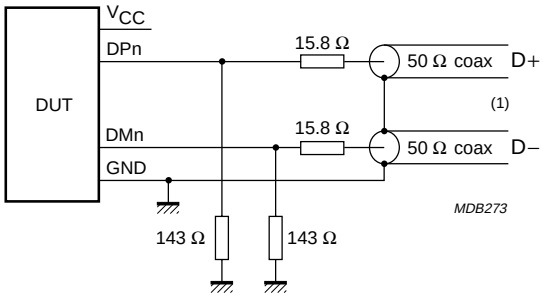


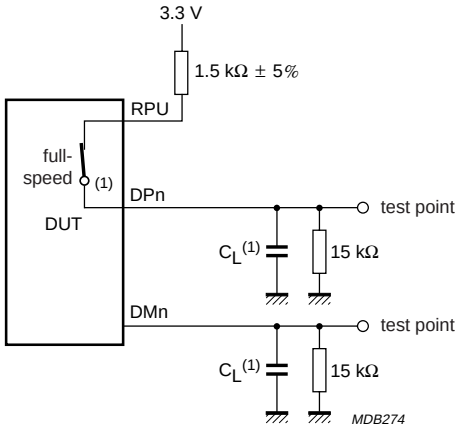
Fig 24. Hybrid powered hub; individual port switching and overcurrent detection.

19. Test information



(1) Transmitter: connected to 50 Ω inputs of a high-speed differential oscilloscope.
Receiver: connected to 50 Ω outputs of a high-speed differential data generator.

Fig 25. High-speed transmitter and receiver test circuit.

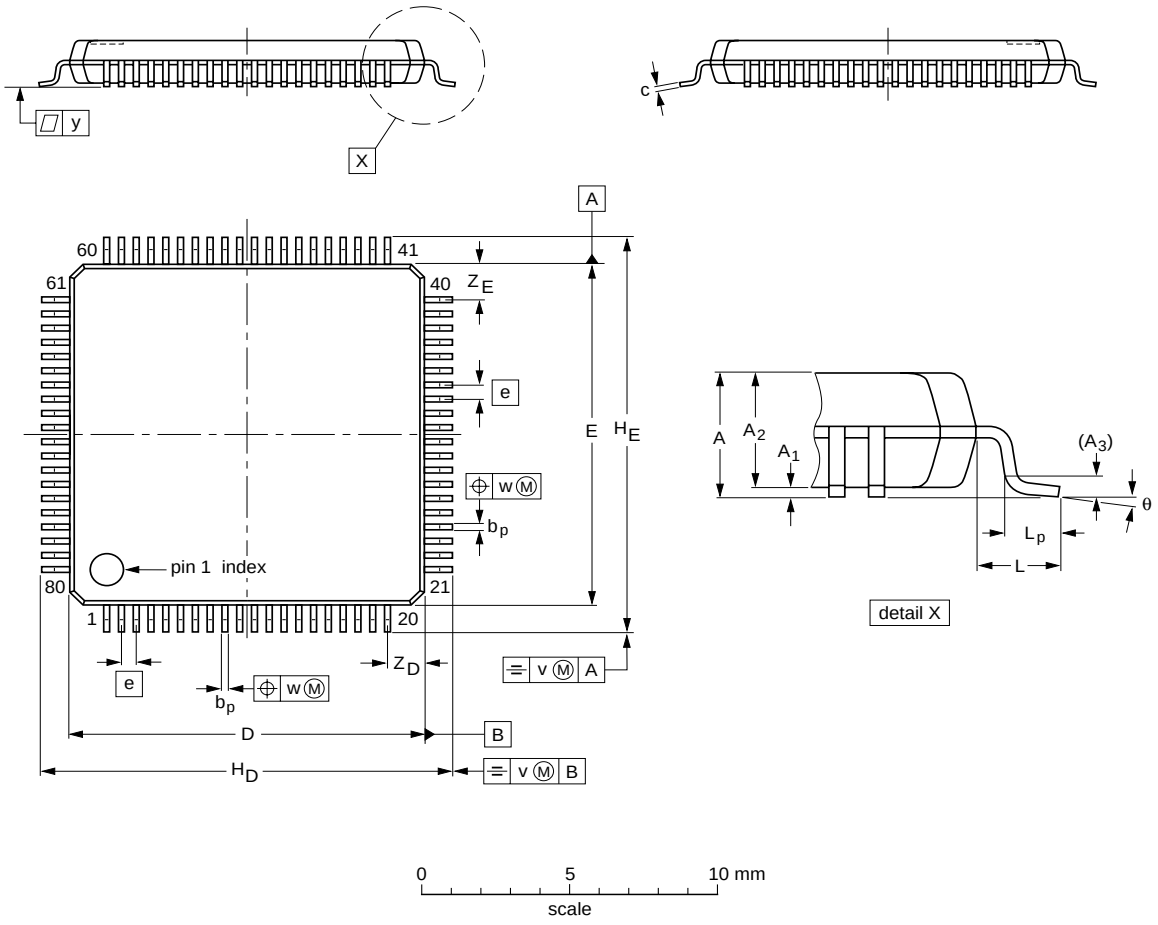


(1) C_L = 50 pF for full-speed.

Fig 26. Full-speed test circuit.

20. Package outline

LQFP80: plastic low profile quad flat package; 80 leads; body 12 x 12 x 1.4 mm **SOT315-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.16 0.04	1.5 1.3	0.25	0.27 0.13	0.18 0.12	12.1 11.9	12.1 11.9	0.5	14.15 13.85	14.15 13.85	1	0.75 0.30	0.2	0.15	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT315-1	136E15	MS-026				~~00-01-19~~ 03-02-25

Fig 27. LQFP80 package outline.

21. Soldering

21.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended. In these situations reflow soldering is recommended.

21.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA and SSOP-T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

21.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.

- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

21.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

21.5 Package related soldering information

Table 48: Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, LBGA, LFBGA, SQFP, SSOP-T[3], TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

22. Revision history

Table 49: Revision history

Rev	Date	CPCN	Description
01	20030625		Preliminary data (9397 750 10691)

23. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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